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March 2001
Revised January 2005

NC7WZ241
TinyLogic® UHS Dual Buffer with 3-STATE Outputs

General Description

The NC7WZ241 is a Dual Non-Inverting Buffer with 3-STATE outputs. The output enable circuitry is organized as active LOW for one buffer and active HIGH for the other buffer, thus facilitating transceiver operation.

The Ultra High Speed device is fabricated with advanced CMOS technology to achieve superior switching performance with high output drive while maintaining low static power dissipation over a broad V_{CC} operating range. The device is specified to operate over the 1.65V to 5.5V V_{CC} operating range. The inputs and outputs are high impedance when V_{CC} is 0V. Inputs tolerate voltages up to 5.5V independent of V_{CC} operating range. Outputs tolerate voltages above V_{CC} when in the 3-STATE condition.

Features

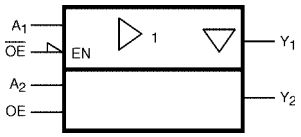
- Space saving US8 surface mount package
- MicroPak™ Pb-Free leadless package
- Ultra High Speed; t_{PD} 2.6 ns Typ into 50 pF at 5V V_{CC}
- High Output Drive; ±24 mA at 3V V_{CC}
- Broad V_{CC} Operating Range: 1.65V to 5.5V
- Matches the performance of LCX when operated at 3.3V V_{CC}
- Power down high impedance inputs/outputs
- Overvoltage tolerant inputs facilitate 5V to 3V translation
- Outputs are overvoltage tolerant in 3-STATE mode
- Patented noise/EMI reduction circuitry implemented

Ordering Code:

Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
NC7WZ241K8X	MAB08A	WZ41	8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide	3k Units on Tape and Reel
NC7WZ241L8X	MAC08A	T7	Pb-Free 8-Lead MicroPak, 1.6 mm Wide	5k Units on Tape and Reel

Pb-Free package per JEDEC J-STD-020B.

Logic Symbol



Function Table

Inputs		Output	
$\overline{OE}$ or OE	A_n	Y_1	Y_2
L	L	L	Z
L	H	H	Z
H	L	Z	L
H	H	Z	H

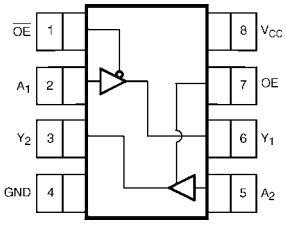
H = HIGH Logic Level
L = LOW Logic Level
Z = 3-STATE

Pin Descriptions

Pin Names	Description
$\overline{OE}$, OE	Enable Inputs for 3-STATE Outputs
A_n	Inputs
Y_n	3-STATE Outputs

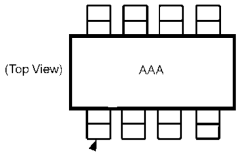
Connection Diagrams

Pin Assignments for US8



(Top View)

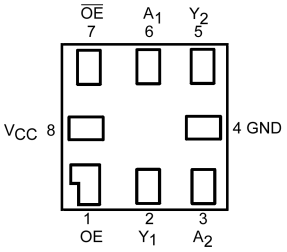
Pin One Orientation Diagram



AAA represents Product Code Top Mark - see ordering code

Note: Orientation of Top Mark determines Pin One location. Read the top product code mark left to read, Pin One is the lower left pin (see diagram).

Pad Assignments for MicroPak



(Top Thru View)

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN}) (Note 2)	−0.5V to +7.0V
DC Output Voltage (V_{OUT})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
@V_{IN} < 0V	−50 mA
DC Output Diode Current (I_{OK})	
@V_{OUT} < 0V	−50 mA
DC Output Source/Sink Current (I_{OUT})	±50 mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	±100 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Junction Temperature under Bias (T_J)	+150°C
Junction Lead Temperature (T_L)	
(Soldering, 10 seconds)	+260°C
Power Dissipation (P_D) @+85°C	250 mW

Recommended Operating Conditions (Note 3)

Supply Voltage Operating (V_{CC})	1.65V to 5.5V
Supply Voltage Data Retention (V_{CC})	1.5V to 5.5V
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	
Active State	0V to V_{CC}
3-State	0V to 5.5V
Operating Temperature (T_A)	−40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
V_{CC} = 1.8V, 0.15V, 2.5V ± 0.2V	0 ns/V to 20 ns/V
V_{CC} = 3.8V ± 0.3V	0 ns/V to 10 ns/V
V_{CC} = 5.0V ± 0.5V	0 ns/V to 5 ns/V
Thermal Resistance (θ_{JA})	250°C/W

Note 1: Absolute maximum ratings are DC values beyond which the device may be damaged or have its useful life impaired. The datasheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside datasheet specifications.

Note 2: The input and output negative voltage ratings may be exceeded is the input and output diode current ratings are observed.

Note 3: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC}	T_A = +25°C			T_A = −40°C to +85°C		Unit	Conditions	
		(V)	Min	Typ	Max	Min	Max			
V_{IH}	HIGH Level Input Voltage	1.65 to 1.95	0.75 V_{CC}			0.75 V_{CC}		V		
		2.3 to 5.5	0.7 V_{CC}			0.7 V_{CC}				
V_{IL}	LOW Level Input Voltage	1.65 to 1.95			0.25 V_{CC}		0.25 V_{CC}	V		
		2.3 to 5.5			0.3 V_{CC}		0.3 V_{CC}			
V_{OH}	HIGH Level Output Voltage	1.65	1.55	1.65		1.55		V	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −100 µA
		2.3	2.2	2.3		2.2				
		3.0	2.9	3.0		2.9				
		4.5	4.4	4.5		4.4				
		1.65	1.29	1.52		1.29		V	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −4 mA
		2.3	1.9	2.15		1.9				I_{OH} = −8 mA
		3.0	2.4	2.80		2.4				I_{OH} = −16 mA
		3.0	2.3	2.68		2.3				I_{OH} = −24 mA
		4.5	3.8	4.20		3.8				I_{OH} = −32 mA
V_{OL}	LOW Level Output Voltage	1.65		0.0	0.10		0.10	V	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100 µA
		2.3		0.0	0.10		0.10			
		3.0		0.0	0.10		0.10			
		4.5		0.0	0.10		0.10			
		1.65		0.08	0.24		0.24	V	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4 mA
		2.3		0.10	0.3		0.3			I_{OL} = 8 mA
		3.0		0.15	0.4		0.4			I_{OL} = 16 mA
		3.0		0.22	0.55		0.55			I_{OL} = 24 mA
		4.5		0.22	0.55		0.55			I_{OL} = 32 mA
I_{IN}	Input Leakage Current	0 to 5.5			±0.1		±1	µA	V_{IN} = 5.5V, GND	
I_{OZ}	3-STATE Output Leakage	1.65 to 5.5			±0.5		±5	µA	V_{IN} = V_{IH} or V_{IL}, 0 ≤ V_{OUT} ≤ 5.5V	
I_{OFF}	Power Off Leakage Current	0.0			1		10	µA	V_{IN} or V_{OUT} = 5.5V	
I_{CC}	Quiescent Supply Current	1.65 to 5.5			1		10	µA	V_{IN} = 5.5V, GND	

Noise Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$		Units	Conditions
			Typ	Max		
V_{OLP} (Note 4)	Quiet Output Maximum Dynamic V_{OL}	5.0		1.0	V	$C_L = 50$ pF
V_{OLV} (Note 4)	Quiet Output Minimum Dynamic V_{OL}	5.0		1.0	V	$C_L = 50$ pF
V_{OHV} (Note 4)	Quiet Output Minimum Dynamic V_{OH}	5.0		4.0	V	$C_L = 50$ pF
V_{IHD} (Note 4)	Minimum HIGH Level Dynamic Input Voltage	5.0		3.5	V	$C_L = 50$ pF
V_{ILD} (Note 4)	Maximum LOW Level Dynamic Input Voltage	5.0		1.5	V	$C_L = 50$ pF

Note 4: Parameter guaranteed by design.

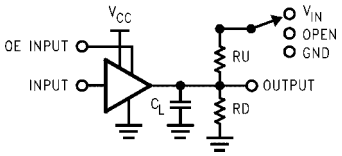
AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$			$T_A = -40°C$ to $+85°C$		Units	Conditions	Figure Number
			Min	Typ	Max	Min	Max			
t_{PLH}	Propagation Delay	1.8 ± 0.15	2.0		12.0	2.0	13.0	ns	$C_L = 15$ pF	Figures 1, 3
t_{PHL}	A_n to Y_n	2.5 ± 0.2	1.0		7.5	1.0	8.0		RD = 1 MΩ	
		3.3 ± 0.3	0.8		5.2	0.8	5.5		S_1 = OPEN	
		5.0 ± 0.5	0.5		4.5	0.5	4.8			
t_{PLH}	Propagation Delay	3.3 ± 0.3	1.2		5.7	1.2	6.0	ns	$C_L = 50$ pF	Figures 1, 3
t_{PHL}	A_n to Y_n	5.0 ± 0.5	0.8		5.0	0.8	5.3		RD = 500Ω	
									S_1 = OPEN	
t_{OSLH}	Output to Output Skew	3.3 ± 0.3			1.0		1.0	ns	$C_L = 50$ pF	Figures 1, 3
t_{OSHL}	(Note 5)	5.0 ± 0.5			0.8		0.8		RD = 500Ω	
									S_1 = OPEN	
t_{PZL}	Output Enable Time	1.8 ± 0.15	3.0		14.0	3.0	15.0	ns	$C_L = 50$ pF	Figures 1, 3
t_{PZH}		2.5 ± 0.2	1.8		8.5	1.8	9.0		RD, RU = 500Ω	
		3.3 ± 0.3	1.2		6.2	1.2	6.5		S_1 = GND for t_{PZH}	
		5.0 ± 0.5	0.8		5.5	0.8	5.8		$S_1 = V_I$ for t_{PZL}	
									$V_I = 2 \times V_{CC}$	
t_{PLZ}	Output Disable Time	1.8 ± 0.15	2.5		12.0	2.5	13.0	ns	$C_L = 50$ pF	Figures 1, 3
t_{PHZ}		2.5 ± 0.2	1.5		8.0	1.5	8.5		RD, RU = 500Ω	
		3.3 ± 0.3	0.8		5.7	0.8	6.0		S_1 = GND for t_{PHZ}	
		5.0 ± 0.5	0.3		4.7	0.3	5.0		$S_1 = V_I$ for t_{PLZ}	
									$V_I = 2 \times V_{CC}$	
C_{IN}	Input Capacitance	0		2.5				pF		
C_{OUT}	Output Capacitance	5.0		4						
C_{PD}	Power Dissipation	3.3		10				pF	$\overline{OE}$ = GND	Figure 2
	Capacitance (Note 6)	5.0		12					OE = V_{CC}	

Note 5: Parameter guaranteed by design. $t_{OSLH} = | t_{PLHmax} - t_{PLHmin} |$; $t_{OSHL} = | t_{PHLmax} - t_{PHLmin} |$.

Note 6: C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure 2.) C_{PD} is related to I_{CCD} dynamic operating current by the expression:
$I_{CCD} = (CPD)\ (V_{CC})\ (f_{IN}) + (I_{CC}$ static).

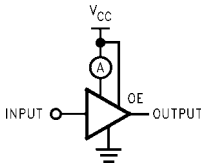
AC Loading and Waveforms



C_L includes load and stray capacitance

Input PRR = 1.0 MHz, t_w = 500 ns

FIGURE 1. AC Test Circuit



Input = AC Waveform; $t_r = t_f = 1.8$ ns;

PRR = 10 MHz; Duty Cycle = 50%

FIGURE 2. I_{CCD} Test Circuit

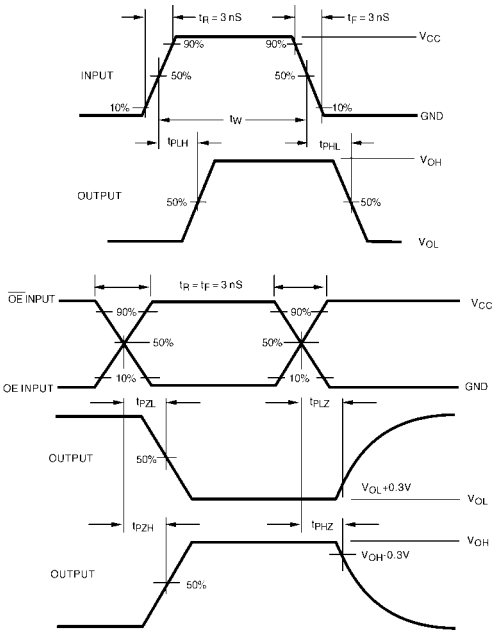


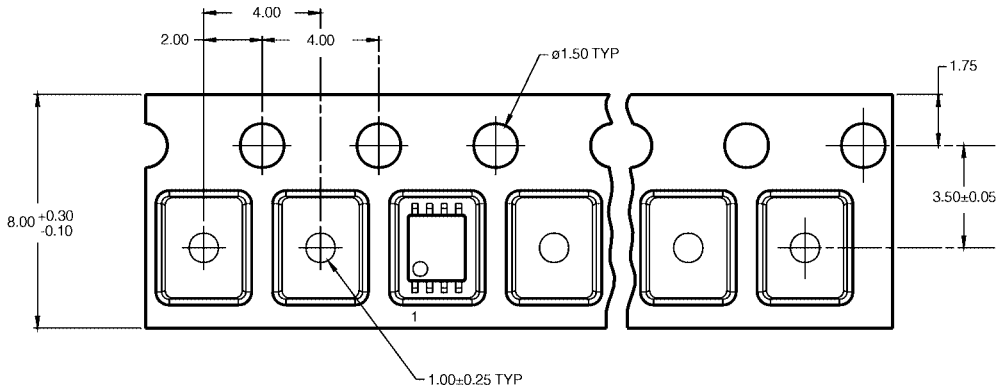
FIGURE 3. AC Waveforms

Tape and Reel Specification

TAPE FORMAT for US8

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
K8X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

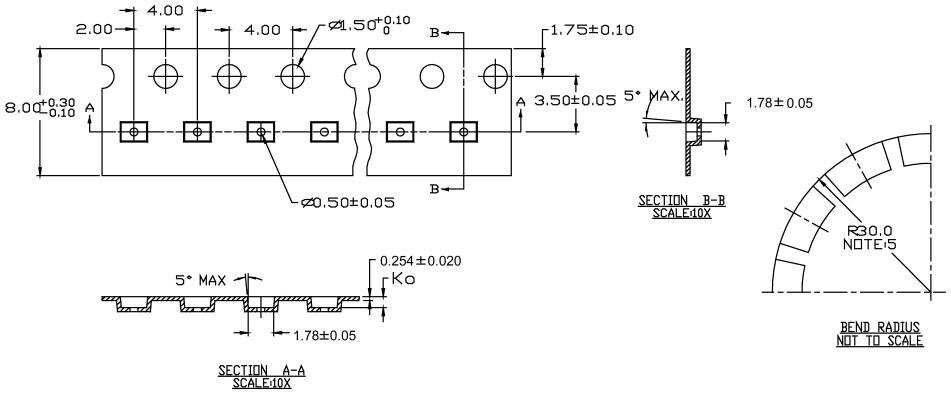
TAPE DIMENSIONS inches (millimeters)



TAPE FORMAT for MicroPak

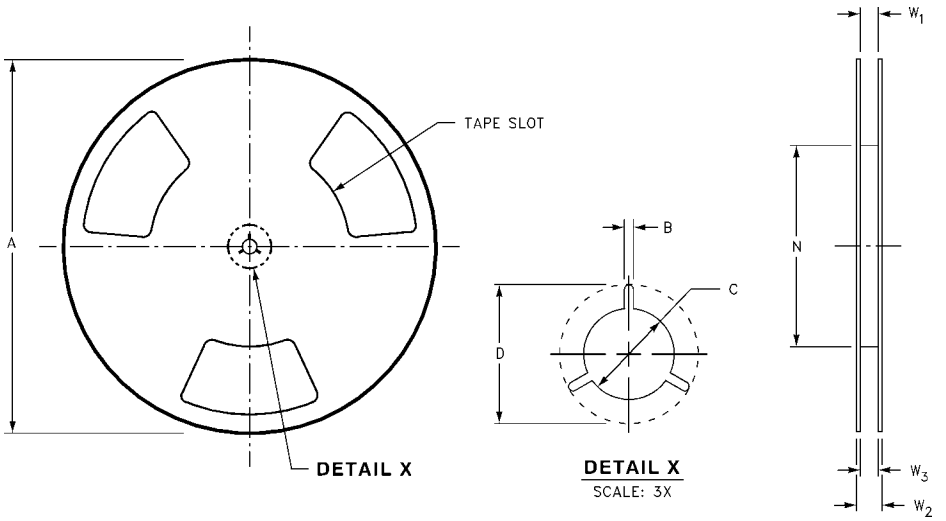
Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
L8X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

TAPE DIMENSIONS inches (millimeters)



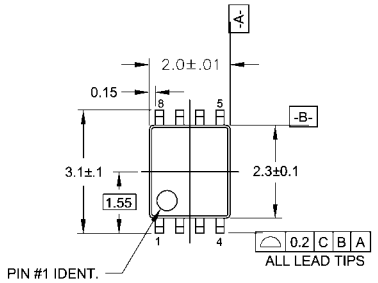
Tape and Reel Specification (Continued)

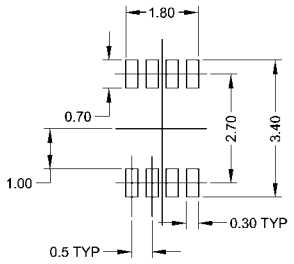
REEL DIMENSIONS inches (millimeters)



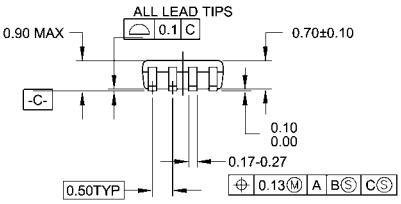
Tape Size	A	B	C	D	N	W1	W2	W3
8 mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.331 + 0.059/–0.000 (8.40 + 1.50/–0.00)	0.567 (14.40)	W1 + 0.078/–0.039 (W1 + 2.00/–1.00)

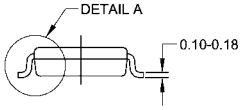
Physical Dimensions inches (millimeters) unless otherwise noted

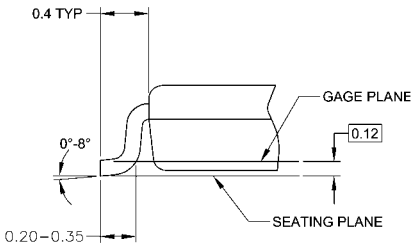




LAND PATTERN RECOMMENDATION







DETAIL A

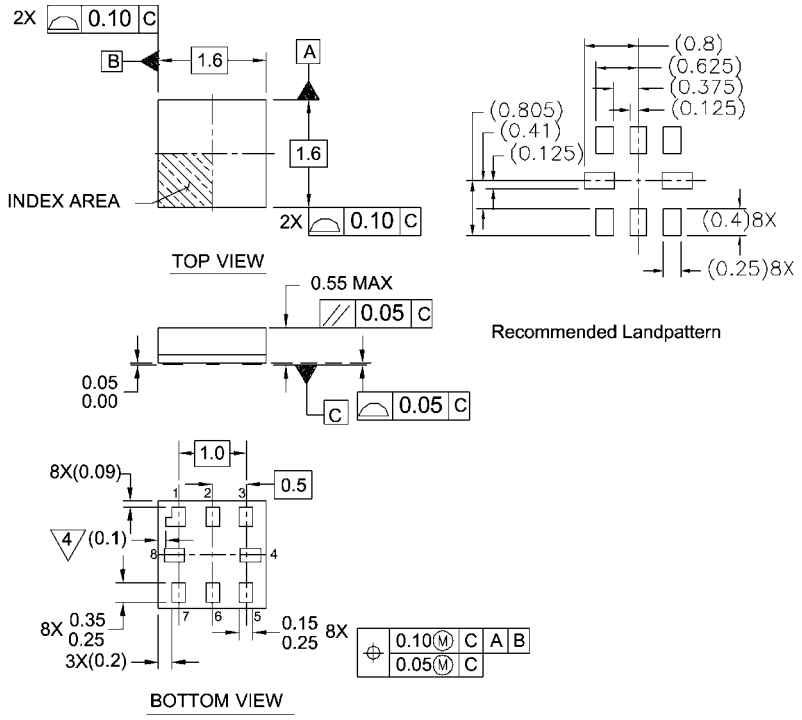
NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-187
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MAB08AREVC

8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide
Package Number MAB08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Notes:

1. PACKAGE CONFORMS TO JEDEC MO-255 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y.14M-1994
4. PIN 1 FLAG, END OF PACKAGE OFFSET.

MAC08AREVC

Pb-Free 8-Lead MicroPak, 1.6 mm Wide
Package Number MAC08A

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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