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December 2010

NC7SP126 TinyLogic[®] ULP Buffer with Three-State Output

Features

- 0.9V to 3.6V V_{CC} Supply Operation
- 3.6V Over-Voltage Tolerant I/O's at Vcc from 0.9V to 3.6V
- Extremely High Speed tpd
 - 3.0ns: Typical for 3.0V to 3.6V V_{CC}
 - 4.0ns: Typical for 2.3V to 2.7V V_{CC}
 - 5.0ns: Typical for 1.65V to 1.95V V_{CC}
 - 6.0ns: Typical for 1.4V to 1.6V V_{CC}
 - 10.0ns: Typical for 1.1V to 1.3V V_{CC}
 - 26.0ns: Typical for 0.9V V_{CC}
- Power-Off High-Impedance Inputs and Outputs
- Static Drive (I_{OH}/I_{OL})
 - ±2.6mA at 3.00V V_{CC}
 - ±2.1mA at 2.30V Vcc
 - ±1.5mA at 1.65V V_{CC}
 - $\pm 1.0 mA$ at 1.4V V_{CC}
 - $\pm 0.5 mA$ at 1.1V V_{CC}
 - $\pm 020 \mu A$ at 0.9V V_{CC}
- Uses Proprietary Quiet Series[™] Noise/EMI Reduction Circuitry
- Ultra-Small MicroPak[™] Leadfree Package
- Ultra-Low Dynamic Power

Description

The NC7SP126 is a single Buffer with 3-STATE output from Fairchild's Ultra-Low Power (ULP) series of Tiny-Logic®. Ideal for applications where battery life is critical, this product is designed for ultra-low power consumption within the V_{CC} operating range of 0.9V to 3.6V $V_{\text{CC}}.$

The internal circuit is composed of a minimum of inverter stages, including the output buffer, to enable ultra-low static and dynamic power.

The NC7SP126, for lower drive requirements, is uniquely designed for optimized power and speed, and is fabricated with an advanced CMOS technology to achieve best in class speed operation while maintaining extremely low CMOS power dissipation.

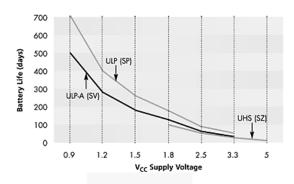
Ordering Information

Part Number	Top Mark	Package	Packing Method
NC7SP126P5X	P26	5-Lead SC70, EIAJ SC-88a, 1.25mm Wide	3000 Units on Tape & Reel
NC7SP126L6X	L6	6-Lead MicroPak™, 1.00mm Wide	5000 Units on Tape & Reel
NC7SP126FHX	L6	6-Lead, MicroPak2™, 1x1mm Body, .35mm Pitch	5000 Units on Tape & Reel

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MicroPak™ and Quiet Series™ are trademarks of Fairchild Semiconductor Corporation.

Battery Life



Notes:

- 1. TinyLogic® ULP and ULP-A with up to 50% less power consumption can extend your battery life significantly. Battery Life = (V_{battery}•l_{battery}•.9)/(P_{device})/24hrs/day
- Where, P_{device} = (I_{CC} V_{CC}) + (C_{PD}+ C_L) V_{CC2} f.

 2. Assumes ideal 3.6V Lithium Ion battery with current rating of 900mAH and derated 90% and device frequency at 10MHz, with C_L = 15pF load.

Figure 1. Battery Life vs. V_{CC} Supply Voltage

Connection Diagram



Figure 2. Logic Symbol

Pin Configurations

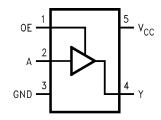


Figure 3. SC70 (Top View)

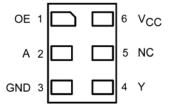


Figure 4. MicroPak™ (Top Through View)

Pin Definitions

Pin # SC70	Pin # MicroPak™	Name	Description
1	1	OE	Input
2	2	A	Input
3	3	GND	Ground
4	4	Y	Output
5	6	Vcc	Supply Voltage
	5	NC	No Connect

Function Table

Inp	outs	Output			
OE	Α	Out Y			
Н	L	L			
Н	Н	Н			
L	X	Z			

H = HIGH Logic Level

L = LOW Logic Level

X = HIGH or LOW Logic Level

Z = HIGH Impedance State

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Para	meter	Min.	Max.	Unit
V _{CC}	Supply Voltage		-0.5	4.6	V
V _{IN}	DC Input Voltage		-0.5	4.6	V
V	DC Output Voltage	HIGH or LOW State ⁽³⁾	-0.5	V _{CC} + 0.5	V
V _{OUT}	DC Output Voltage	V _{CC} =0V	-0.5	4.6	V
I _{IK}	DC Input Diode Current	$V_{IN} < 0V$		-50	mA
	DC Output Diodo Current	V _{OUT} < 0V		-50	~ Λ
I _{OK}	DC Output Diode Current	$V_{OUT} > V_{CC}$		+50	mA
I _{OH} /I _{OL}	DC Output Source/Sink Curren	t		±50	mA
I _{CC} or I _{GND}	DC V _{CC} or Ground Current per	Supply Pin		±50	mA
T _{STG}	Storage Temperature Range		-65	+150	°C
TJ	Junction Temperature under Bi	as		+150	°C
TL	Junction Lead Temperature, Sc	oldering 10 Seconds		+260	°C
		SC70-5		150	
P_{D}	Power Dissipation at +85°C	MicroPak™-6		130	mW
		MicroPak2™-6		120	
ESD	Human Body Model, JEDEC:JE		4000	V	
ESD	Charge Device Model, JEDEC:	JESD22-C101		2000	V

Note:

3. IO absolute maximum rating must be observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	Min.	Max.	Unit	
Vcc	Supply Voltage Operating		0.9	3.6	V	
V _{IN}	Input Voltage		0	3.6	V	
Vout	Output Voltage	V _{CC} =0V	0	3.6	V	
VOUT	Output voltage	HIGH or LOW State	0	V _{CC}	v	
		V _{CC} =3.0V to 3.6V		±2.6		
		V _{CC} =2.3V to 2.7V		±2.1	7	
1/1	Output Current	V _{CC} =1.65V to 1.95V		±1.5	mA	
I _{OH} /I _{OL}	Output Current	V _{CC} =1.4V to 1.6V		±1.0		
		V _{CC} =1.1V to 1.3V		±0.5	$\mathbf{K} \cup$	
		V _{CC} =0.9V		±20	μA	
T_A	Operating Temperature, Free Air		-40	+85	°C	
Δt/ΔV	Minimum Input Edge Rate	V _{IN} =0.8V to 2.0, V _{CC} =3.0V		10	ns/V	
		SC70-5		425		
θ_{JA}	Thermal Resistance	MicroPak™-6		500	°C/W	
		MicroPak2™-6		560	1	

Note:

4. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

0	D	.,	0	T _A =+2	25°C	T _A =-40	to +85°C	11!4
Symbol	Parameter	V _{CC}	Conditions	Min.	Max.	Min.	Max.	Units
		0.90		.65 x V _{CC}		.65 x V _{CC}		
		$1.10 \le V_{CC} \le 1.30$.65 x V _{CC}		.65 x V _{CC}		
	HIGH Level Input	$1.40 \le V_{CC} \le 1.60$.65 x V _{CC}		.65 x V _{CC}		\ ,,
V_{IH}	Voltage	$1.65 \le V_{CC} \le 1.95$.65 x V _{CC}		.65 x V _{CC}		V
		$2.30 \leq V_{CC} \leq 2.70$		1.6		1.6		
		$3.00 \le V_{CC} \le 3.60$		2.1		2.1		
		0.90			.35 x V _{CC}		.35 x V _{CC}	
		$1.10 \le V_{CC} \le 1.30$	1		.35 x V _{CC}		.35 x V _{CC}	
.,	LOW Level Input	$1.40 \leq V_{CC} \leq 1.60$	1		.35 x V _{CC}		.35 x V _{CC}	١,,
V_{IL}	Voltage	$1.65 \le V_{CC} \le 1.95$.35 x V _{CC}		.35 x V _{CC}	V
		$2.30 \leq V_{CC} \leq 2.70$			0.7		0.7	
		$3.00 \le V_{CC} \le 3.60$	1		0.9		0.9	
7		0.90		V _{CC} -0.1		V _{CC} -0.1		
	1.40 ≤ '	1.10 ≤ V _{CC} ≤ 1.30		V _{CC} -0.1		V _{CC} -0.1		
		1.40 ≤ V _{CC} ≤ 1.60	1.	V _{CC} -0.1		V _{CC} -0.1		
		1.65 ≤ V _{CC} ≤ 1.95	Ι _{ΟΗ} =-20μΑ	V _{CC} -0.1		V _{CC} -0.1		
VoH Voltage	$2.30 \le V_{CC} \le 2.70$	1	V _{CC} -0.1		V _{CC} -0.1			
	$3.00 \le V_{CC} \le 3.60$	1	V _{CC} -0.1		V _{CC} -0.1		V	
	Voltage	1.10 ≤ V _{CC} ≤ 1.30	I _{OH} =-0.5mA	.75 x V _{CC}		.70 x V _{CC}		
		1.40 ≤ V _{CC} ≤ 1.60	I _{OH} =-1mA	1.07		0.99		
		1.65 ≤ V _{CC} ≤ 1.95	I _{OH} =-1.5mA	1.24		1.22		
		2.30 ≤ V _{CC} ≤ 2.70	I _{OH} =-2.1mA	1.95		1.87		
		3.00 ≤ V _{CC} ≤ 3.60	I _{OH} =-2.6mA	2.61		2.55		
		0.90		7	0.1		0.1	
		1.10 ≤ V _{CC} ≤ 1.30			0.1		0.1	
		1.40 ≤ V _{CC} ≤ 1.60	1		0.1	/	0.1	
		1.65 ≤ V _{CC} ≤ 1.95	I _{OL} =20μA		0.1		0.1	
		$2.30 \le V_{CC} \le 2.70$	1		0.1		0.1	
V_{OL}	LOW Level Output	$3.00 \le V_{CC} \le 3.60$	1		0.1		0.1	V
	Voltage	1.10 ≤ V _{CC} ≤ 1.30	I _{OL} =0.5mA		.30 x V _{CC}		.30 x V _{CC}	
		1.40 ≤ V _{CC} ≤ 1.60	I _{OL} =1mA		0.31		0.37	
		1.65 ≤ V _{CC} ≤ 1.95	I _{OL} =1.5mA		0.31		0.35	
		2.30 ≤ V _{CC} ≤ 2.70	I _{OL} =2.1mA		0.31		0.33	
		3.00 ≤ V _{CC} ≤ 3.60	I _{OL} =2.6mA		0.31		0.33	$\supset \cap$
I _{IN}	Input Leakage Current	0.90 to 3.60	$0 \leq V_{IN} \leq 3.60$		±0.1		±0.5	μΑ
l _{OZ}	3-STATE Output Leakage	0.90 to 3.6	$\begin{array}{c} V_{IN} = V_{IH} \text{ or } V_{IL} \\ 0 \leq V_{IN} \leq 3.60 \end{array}$		±0.5		±0.5	μA
I _{OFF}	Power Off Leakage Current	0	$\begin{array}{l} 0 \leq \left(V_{IN}, V_{O}\right) \\ \leq 3.60 \end{array}$		0.5		0.5	μΑ
Icc	Quiescent Supply Current	0.90 to 3.60	V _{IN} =V _{CC} , or GND		0.9		0.9	μΑ

AC Electrical Characteristics

Cumbal	Doromotor	V	Conditions	Т	A=+25°	C	T _A =-40	to +85°C	Hnito	Ciaura
Symbol	Parameter	V _{cc}	Conditions	Min.	Тур.	Max.	Min.	Max.	Units	Figure
		0.90			26					
		1.10 ≤ V _{CC} ≤ 1.30		4.0	10.0	19.1	3.5	39.6		
	, , Propagation	1.40 ≤ V _{CC} ≤ 1.60	C _L =10pF,	2.0	6.0	11.2	1.5	14.5		Figure 5
t _{PHL} , t _{PLH}	Delay	1.65 ≤ V _{CC} ≤ 1.95	$R_L=1M\Omega$	1.5	5.0	8.6	1.0	11.6	ns	Figure 6
		2.30 ≤ V _{CC} ≤ 2.70		1.0	4.0	6.3	0.8	8.2		
		$3.00 \le V_{CC} \le 3.60$		1.0	3.0	5.3	0.5	7.2		
		0.90			29					
		1.10 ≤ V _{CC} ≤ 1.30		4.0	8.0	17.5	3.5	40.4		
	Output Enable	1.40 ≤ V _{CC} ≤ 1.60	C _L =10pF,	2.0	6.0	11.9	1.5	14.8		Figure 5
$t_{PZL,}t_{PZH}$	Time	1.65 ≤ V _{CC} ≤ 1.95	R_{D} =5000 Ω R_{D} =5000 Ω	1.5	5.0	9.7	1.0	12.3	ns	Figure 6
		$2.30 \leq V_{CC} \leq 2.70$		1.0	4.0	7.7	0.8	10.5		
		$3.00 \leq V_{CC} \leq 3.60$		1.0	3.0	6.9	0.5	8.6		
		0.90			28	1				
	Output $1.40 \le V_{CC} \le 1$	1.10 ≤ V _{CC} ≤ 1.30	C_L =10pF, R_U =5000 Ω R_D =5000 Ω	4.0	8.0	20.5	3.5	42.0	ns	
		1.40 ≤ V _{CC} ≤ 1.60		2.0	6.0	15.3	1.5	18.0		Figure 5 Figure 6
$t_{PHZ,}t_{PLZ}$	Disable Time	$1.65 \leq V_{CC} \leq 1.95$		1.5	5.0	14.7	1.0	17.8		
		$2.30 \leq V_{CC} \leq 2.70$		1.0	4.0	13.7	0.8	15.0		
		$3.00 \leq V_{CC} \leq 3.60$		1.0	3.0	13.5	0.5	14.8		
		0.90			28					
		$1.10 \le V_{CC} \le 1.30$		5.0	10.0	20.5	4.5	42.5		
+ +	Propagation	$1.40 \le V_{CC} \le 1.60$	C _L =15pF,	3.0	7.0	11.8	2.5	15.4	ns	Figure 5
t _{PHL} , t _{PLH}	Delay	$1.65 \leq V_{CC} \leq 1.95$	$R_L=1M\Omega$	2.0	5.0	9.1	2.0	12.2	115	Figure 6
		$2.30 \leq V_{CC} \leq 2.70$		1.5	4.0	6.6	1.0	8.6		
		$3.00 \leq V_{CC} \leq 3.60$		1.0	3.0	5.6	0.5	7.5		
		0.90			31					
		$1.10 \le V_{CC} \le 1.30$		5.0	11.0	18.2	4.5	43.3		
t _{PZL} ,t _{PZH}	Output Enable	$1.40 \leq V_{CC} \leq 1.60$	$C_L=15pF$, $R_U=5000\Omega$	3.0	7.0	12.5	2.5	15.5	ns	Figure 5
PZL, PZH	Time	$1.65 \le V_{CC} \le 1.95$	$R_D=5000\Omega$	2.0	5.0	10.2	2.0	12.9	110	Figure 6
		$2.30 \leq V_{CC} \leq 2.70$		1.5	4.0	8.0	1.0	9.9		
		$3.00 \leq V_{CC} \leq 3.60$		1.0	3.0	7.2	0.5	8.9		
		0.90			30					
		$1.10 \le V_{CC} \le 1.30$	0 15 5	5.0	11.0	21.6	4.5	44.9	ns	Figure 5 Figure 6
t _{PHZ} t _{PLZ}	Output	$1.40 \le V_{CC} \le 1.60$	C _L =15pF, R _U =5000Ω	3.0	7.0	15.9	2.5	18.8		
YFIIZ,YPLZ	Disable Time	$1.65 \le V_{CC} \le 1.95$	$R_D=5000\Omega$	2.0	5.0	15.2	2.0	18.2		
		$2.30 \leq V_{CC} \leq 2.70$		1.5	4.0	14.1	1.0	15.4		
		$3.00 \leq V_{CC} \leq 3.60$		1.0	3.0	13.9	0.5	15.1		

Continued on following page...

AC Electrical Characteristics (Continued)

		.,	0	Т	A=+25°	С	T _A =-40 to	o +85°C		
Symbol	Parameter V _{CC}		Conditions	Min.	Тур.	Min.	Тур.	Min.	Units	Figure
		0.90			34					
		$1.10 \le V_{CC} \le 1.30$		5.5	12.0	23.4	5.0	51.1		
	Propagation	$1.40 \le V_{CC} \le 1.60$	C _L =30pF,	4.0	8.0	13.8	3.0	17.7		Figure 5
t _{PHL} , t _{PLH}	Delay	$1.65 \leq V_{CC} \leq 1.95$	$R_L=1M\Omega$	2.0	6.0	10.6	2.0	14.0	ns	Figure 6
		$2.30 \leq V_{CC} \leq 2.70$		1.0	5.0	7.6	1.0	9.9		
		$3.00 \leq V_{CC} \leq 3.60$		0.8	4.0	6.4	0.5	8.9		
		0.90			37					
		$1.10 \le V_{CC} \le 1.30$		6.0	13.0	24.4	5.0	51.9		
	Output Enable	$1.40 \leq V_{CC} \leq 1.60$	C _L =30pF,	4.0	8.0	14.5	3.0	17.9]	Figure 5 Figure 6
t _{PZL} ,t _{PZH}	Time	$1.65 \le V_{CC} \le 1.95$	R _U =5000Ω R _D =5000Ω	2.0	6.0	11.7	2.0	14.7	ns	
		$2.30 \leq V_{CC} \leq 2.70$	_	1.0	5.0	9.1	1.0	11.1		
		$3.00 \leq V_{CC} \leq 3.60$		0.8	4.0	8.1	0.5	10.1		
		0.90			36					
		$1.10 \le V_{CC} \le 1.30$		6.0	13.0	24.8	5.0	53.5		
	Output	$1.40 \le V_{CC} \le 1.60$	C _L =30pF,	4.0	8.0	17.1	3.0	21.1]	Figure 5
t _{PHZ} ,t _{PLZ}	Disable Time	$1.65 \leq V_{CC} \leq 1.95$	R _U =5000Ω R _D =5000Ω	2.0	6.0	16.5	2.0	20.5	ns	Figure 6
		$2.30 \leq V_{CC} \leq 2.70$		1.0	5.0	15.2	1.0	16.7		
		$3.00 \leq V_{CC} \leq 3.60$		0.8	4.0	14.8	0.5	16.3		
C _{IN}	Input Capacitance	0.00			2				pF	
C _{OUT}	Output Capacitance	0.00			4				pF	
C _{PD}	Power Dissipation Capacitance	0.90 to 3.60	V _{IN} =0V or V _{CC} , f=10MHz		8				pF	

AC Loadings and Waveforms

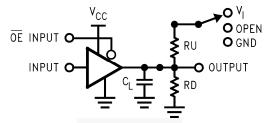


Figure 5. AC Test Circuit

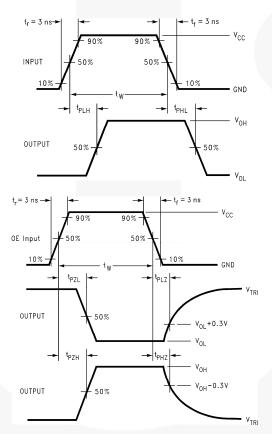


Figure 6. AC Waveforms

Symbol	V _{cc}							
Symbol	$3.3V \pm 0.3V$	2.5V ± 0.2V	1.8V ± 0.15V	1.5V ± 0.10V	1.2V ± 0.10V	0.9V		
V _{mi}	1.5V	V _{CC} /2						
V_{mo}	0.3V	0.15V	0.15V	0.10V	0.10V	0.10V		

Physical Dimensions

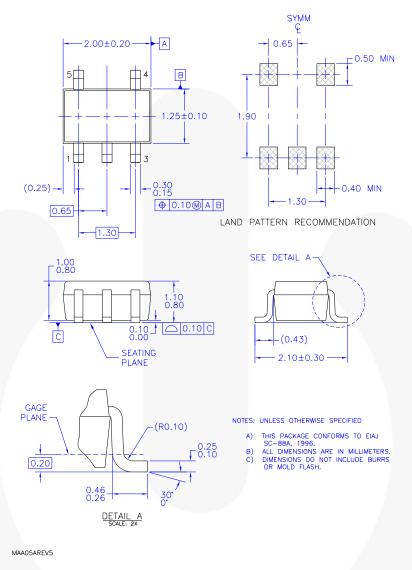


Figure 7. 5-Lead, SC70, EIAJ SC-88a, 1.25mm Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

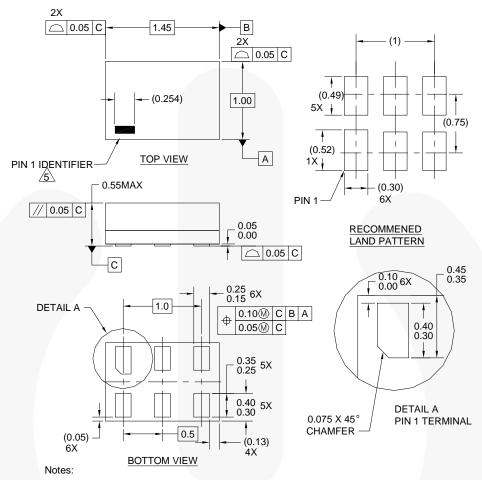
Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings: http://www.fairchildsemi.com/packaging/.

Tape and Reel Specification

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications: http://www.fairchildsemi.com/products/analog/pdf/sc70-5_tr.pdf.

Package Designator Tape Section		Cavity Number	Cavity Status	Cover Type Status
	Leader (Start End)	125 (Typical)	Empty	Sealed
P5X	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

Physical Dimensions



- 1. CONFORMS TO JEDEC STANDARD M0-252 VARIATION UAAD
- 2. DIMENSIONS ARE IN MILLIMETERS
- 3. DRAWING CONFORMS TO ASME Y14.5M-1994
- 4. FILENAME AND REVISION: MAC06AREV4
- 5. PIN ONE IDENTIFIER IS 2X LENGTH OF ANY
 - OTHER LINE IN THE MARK CODE LAYOUT.

Figure 8. 6-Lead, MicroPak™, 1.0mm Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings: http://www.fairchildsemi.com/packaging/.

Tape and Reel Specification

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications: http://www.fairchildsemi.com/products/logic/pdf/micropak_tr.pdf.

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
	Leader (Start End)	125 (Typical)	Empty	Sealed
L6X	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

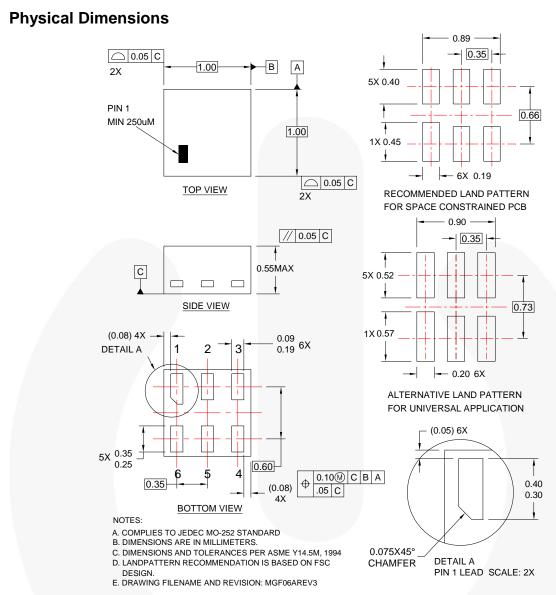


Figure 9. 6-Lead, MicroPak2™, 1x1mm Body, .35mm Pitch

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Tape and Reel Specifications

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications: http://www.fairchildsemi.com/packaging/MicroPAK2 6L tr.pdf.

Package Designator Tape Section		Cavity Number	Cavity Status	Cover Type Status
	Leader (Start End)	125 (Typical)	Empty	Sealed
FHX	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed





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