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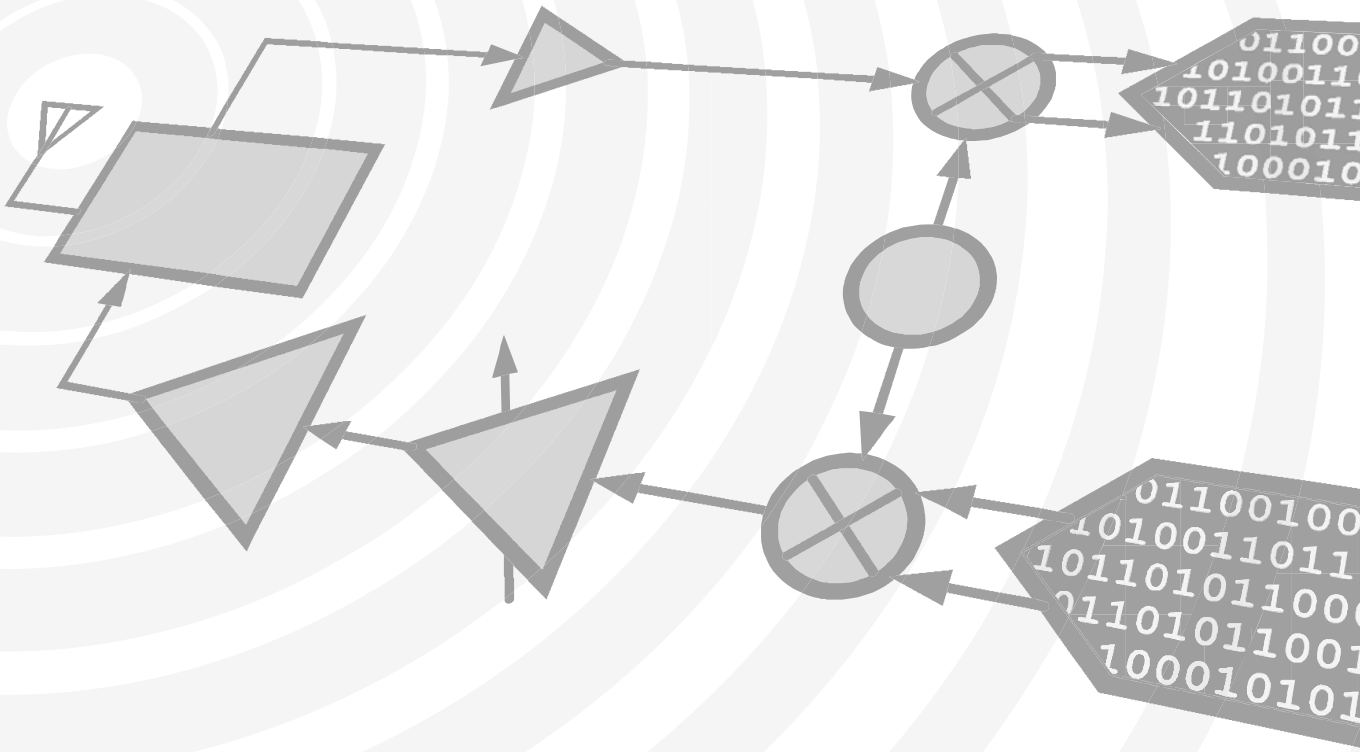

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HMC685* Product Page Quick Links

Last Content Update: 08/30/2016

Comparable Parts

View a parametric search of comparable parts

Evaluation Kits

- HMC685LP4 Evaluation Board

Documentation

Data Sheet

- HMC685 Data Sheet

Reference Materials

Quality Documentation

- Package/Assembly Qualification Test Report: LP4, LP4B, LP4C, LP4K (QTR: 2013-00487 REV: 04)
- Semiconductor Qualification Test Report: BiCMOS-A (QTR: 2013-00235)

Design Resources

- HMC685 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

Discussions

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HMC685LP4 / 685LP4E

v04.0110

BiCMOS MMIC MIXER W/ INTEGRATED LO AMPLIFIER, 1.7 - 2.2 GHz

Typical Applications

The HMC685LP4(E) is Ideal for:

- Cellular/3G & LTE/WiMAX/4G
- Basestations & Repeaters
- GSM, CDMA & OFDM
- Transmitters and Receivers

Features

High Input IP3: +35 dBm

8 dB Conversion Loss @ 0 dBm LO

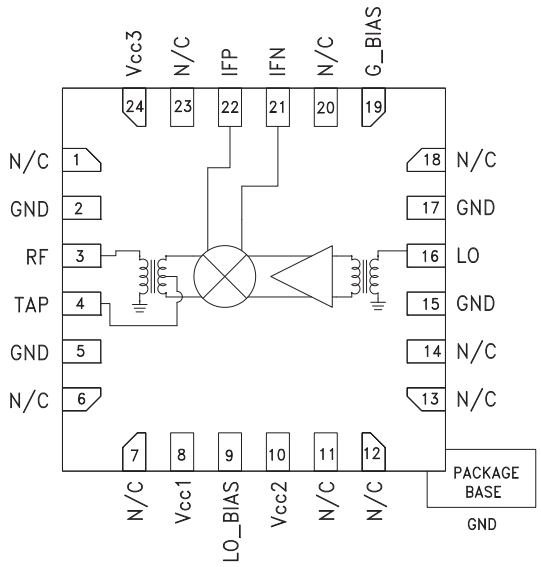
Optimized for Low Side LO Input

Upconversion & Downconversion Applications

Adjustable Supply Current

24 Lead 4x4mm SMT Package: $16mm^2$

Functional Diagram



General Description

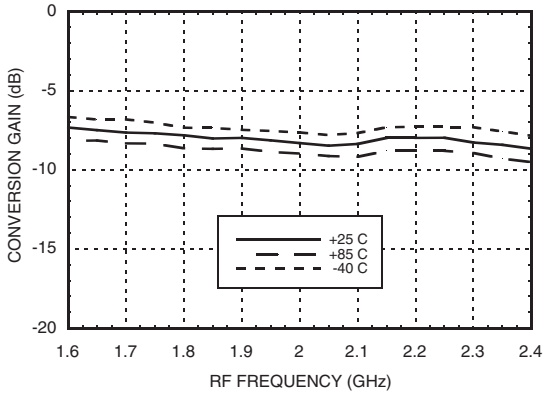
The HMC685LP4(E) is a high dynamic range passive MMIC mixer with integrated LO amplifier in a 4x4 SMT QFN package covering 1.7 to 2.2 GHz. Excellent input IP3 performance of +35 dBm for down conversion is provided for 3G & 4G GSM/CDMA applications at an LO drive of 0 dBm. With an input 1 dB compression of +27 dBm, the RF port will accept a wide range of input signal levels. Conversion loss is 8 dB typical. The DC to 500 MHz IF frequency response will satisfy GSM/CDMA transmit or receive frequency plans. The HMC685LP4(E) is pin for pin compatible with the HMC684LP4(E) which is a 700 - 1000 MHz mixer with LO amplifier.

Electrical Specifications, T_A = +25° C, IF = 200 MHz, LO = 0 dBm, Vcc = Vcc1, 2, 3 = +5V, G_Bias = +2.5V*

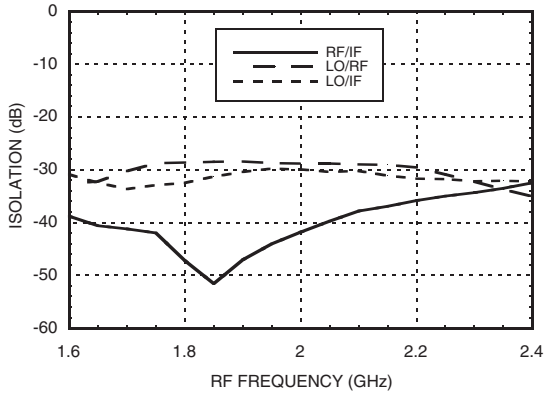
Nominal Supply	Icc = 120 mA			Icc = 90 mA	Icc = 70 mA	Units
Parameter	Min.	Typ.	Max.	Typ.	Typ.	
Frequency Range, RF	1.7 - 2.2					GHz
Frequency Range, LO	1.5 - 2.2					GHz
Frequency Range, IF	DC - 500					MHz
Conversion Loss		8	10	8	8	dB
Noise Figure (SSB)		8		8	8	dB
LO to RF Isolation	22	30		33	34	dB
LO to IF Isolation	24	30		31	32	dB
RF to IF Isolation	30	42		42	43	dB
IP3 (Input)		35		34	32	dBm
1 dB Compression (Input)		25		24	23	dBm
LO Drive Input Level (Typical)	-6 to +3			-6 to +3	-6 to +3	dBm
Supply Current Icc total		120	140	90	70	mA

** Unless otherwise noted all measurements performed as downconverter with low side LO & IF = 200 MHz.*

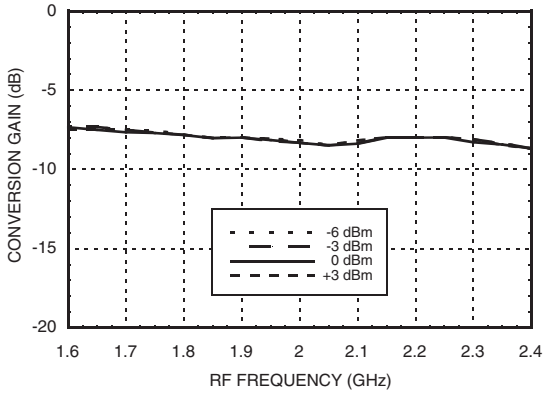
Conversion Gain vs. Temperature



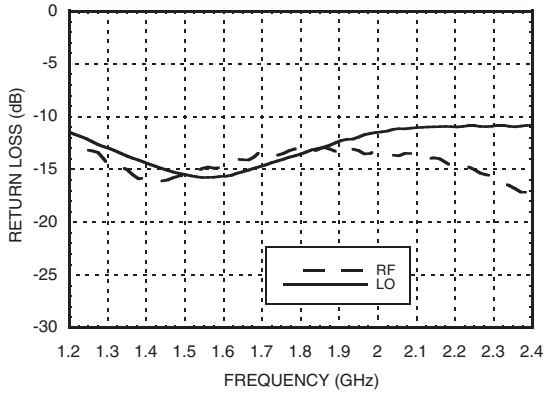
Isolation



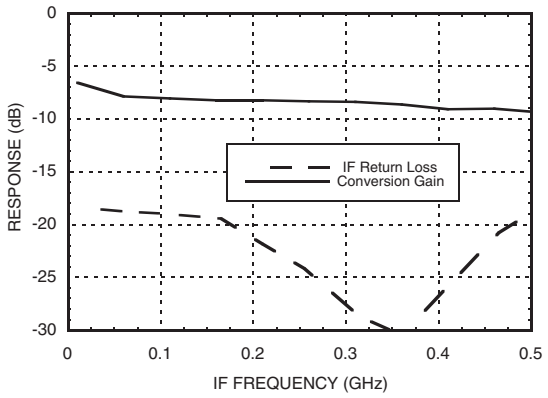
Conversion Gain vs. LO Drive



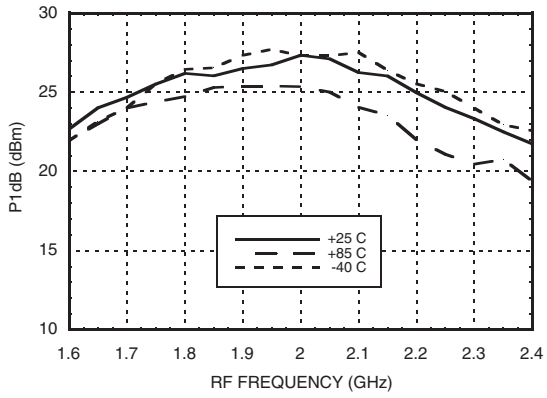
Return Loss



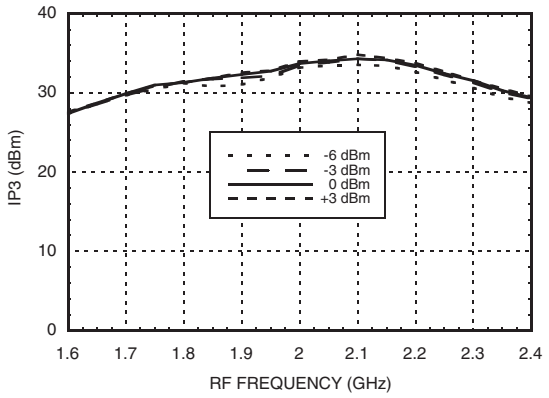
IF Bandwidth (LO= 1.7 GHz)



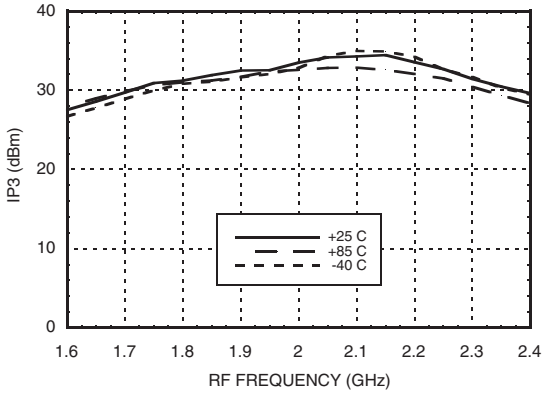
Input P1dB vs. Temperature



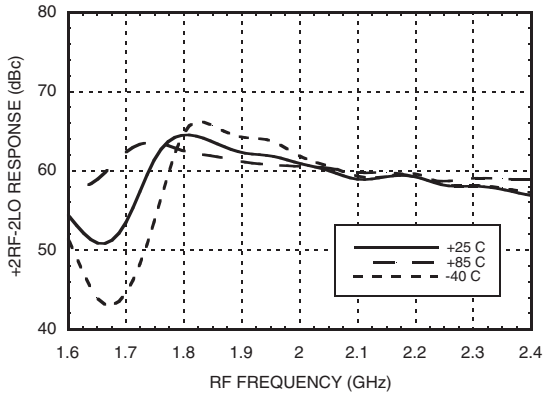
Input IP3 vs. LO Drive [1]



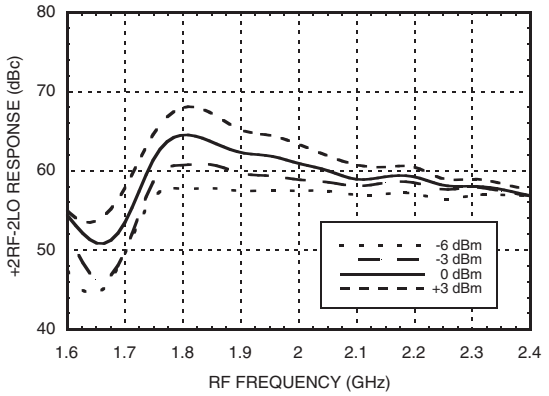
Input IP3 vs. Temperature[1]



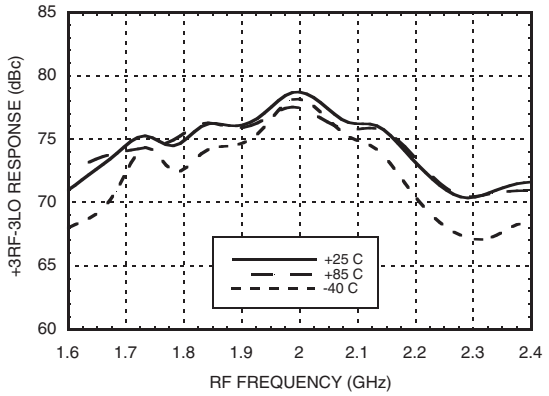
+2RF -2LO Response vs. Temperature [2]



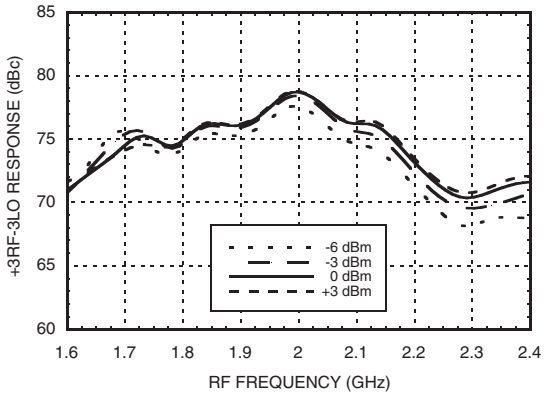
+2RF -2LO Response vs. LO Drive [2]



+3RF -3LO Response vs. Temperature [2]



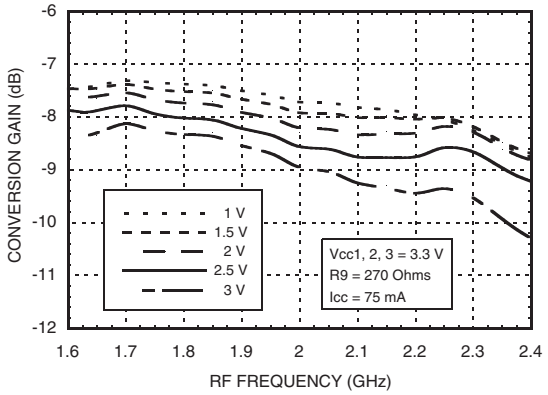
+3RF -3LO Response vs. LO Drive [2]



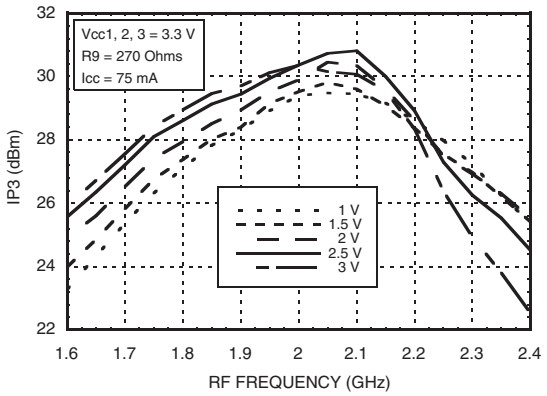
[1] Two-tone input power = +9 dBm each tone, 1 MHz spacing [2] Referenced to RF input power at 0 dBm

Low Power Consumption Performance

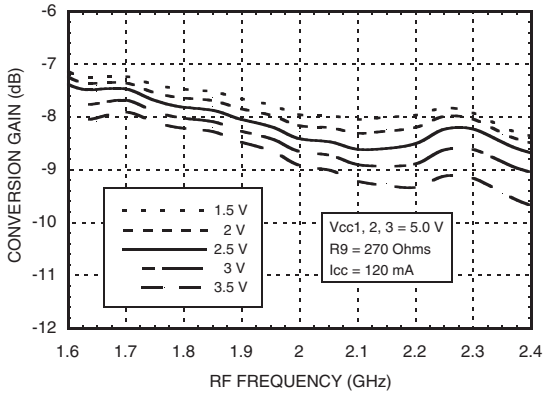
Conversion Gain vs. G_Bias Voltage



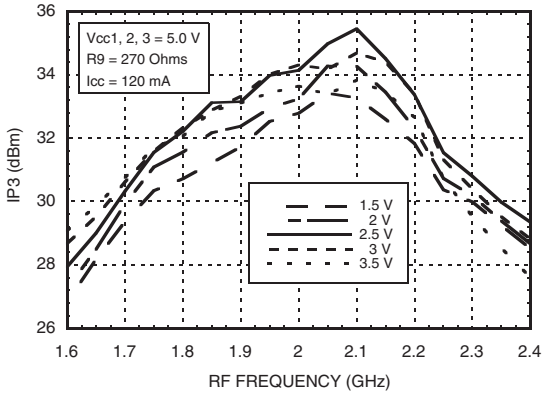
Input IP3 vs. G_Bias Voltage [1]



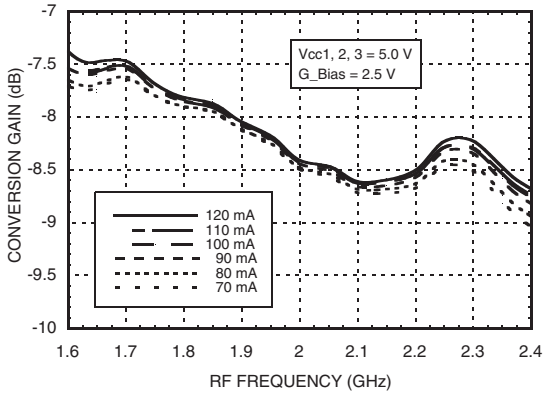
Conversion Gain vs. G_Bias Voltage



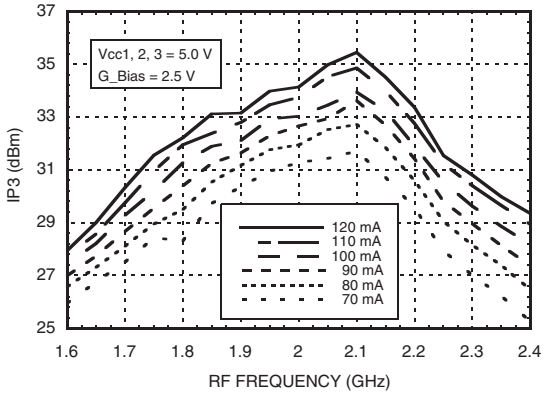
Input IP3 vs. G_Bias Voltage [1]



Conversion Gain vs. Icc



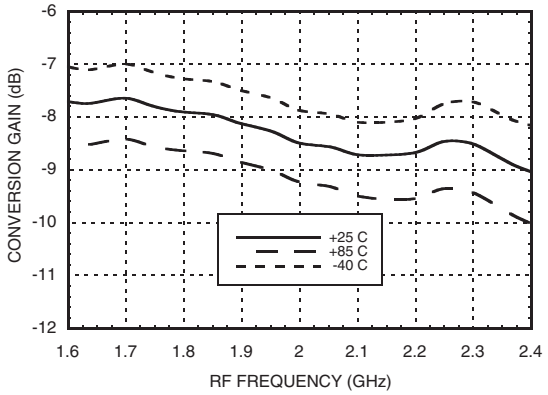
Input IP3 vs. Icc [1]



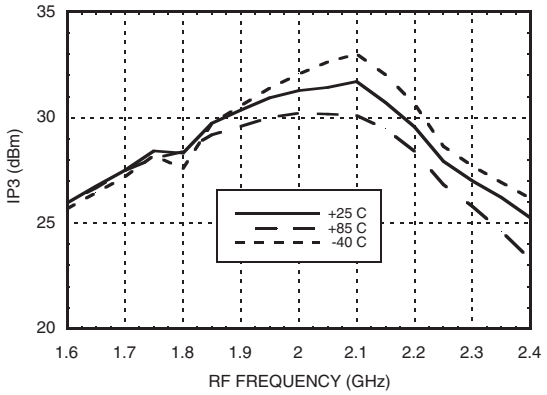
[1] Two-tone input power = +9 dBm each tone, 1 MHz spacing

Low Power Consumption Performance

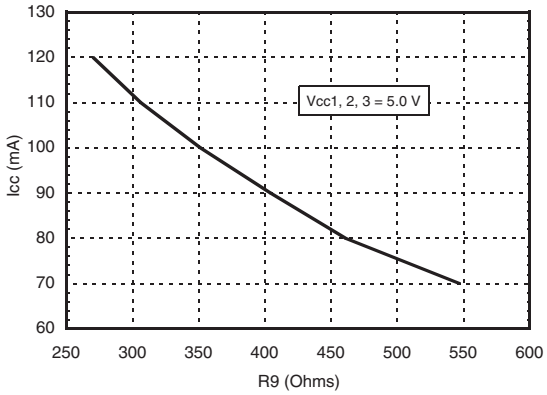
Conversion Gain vs. Temperature, Icc = 70 mA



Input IP3 vs. Temperature, Icc = 70 mA [1]

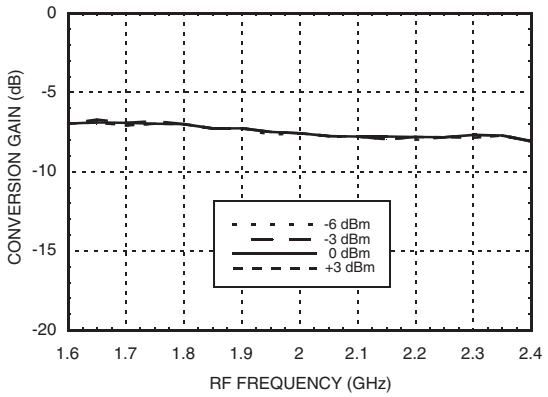


Icc vs. R9

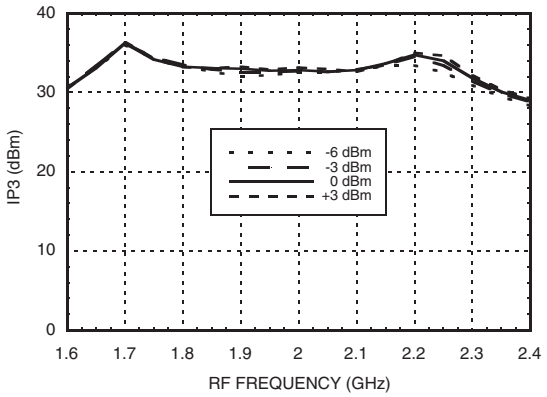


Typical Upconverter Performance

Conversion Gain vs. LO Drive



Input IP3 vs. LO Drive [1]



[1] Two-tone input power = +9 dBm each tone, 1 MHz spacing.

Absolute Maximum Ratings

RF / IF Input (Vcc1, 2, 3 = +5V)	+26 dBm
LO Drive (Vcc1, 2, 3 = +5V)	+10 dBm
Vcc1-3	5.5V
Channel Temperature	125 °C
Continuous Pdiss (T = 85°C) (derate 20.69 mW/°C above 85°C)	0.83 mW
Thermal Resistance (channel to ground paddle)	48.33 °C/W
Storage Temperature	-65 to 150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 1A

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Typical Supply Current vs. Vcc

Vcc1, 2, 3 (V)	Icc total (mA)
4.75	113
5.00	120
5.25	127
Downconverter will operate over full voltage range shown above.	

MxN Spurious @ IF Port

	nLO				
mRF	0	1	2	3	4
0	xx	21	16	37	29
1	39	0	37	24	53
2	67	64	54	66	76
3	106	77	95	69	89
4	106	116	115	99	105

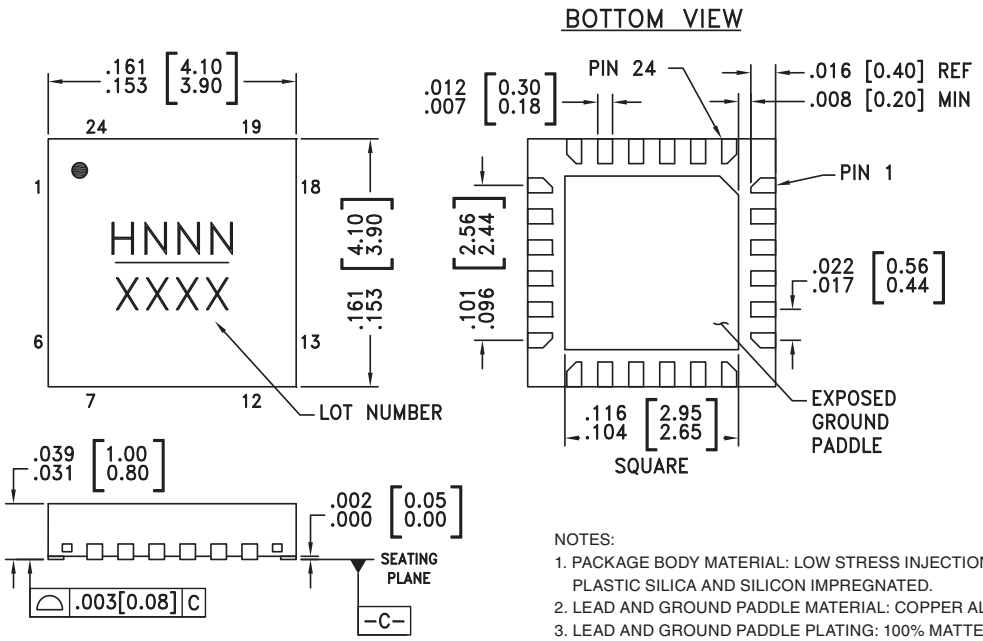
RF Freq. = 1.9 GHz @ 0 dBm
LO Freq. = 1.7 GHz @ 0 dBm
All values in dBc below IF power level (1RF - 1LO).

Harmonics of LO

	nLO Spur @ RF Port			
LO Freq. (GHz)	1	2	3	4
1.6	29	13	32	25
1.7	28	13	35	19
1.8	29	14	41	18
1.9	29	16	41	20
2.0	29	20	42	28
2.1	30	22	37	30
2.2	31	22	35	31
2.3	35	21	34	33

LO = 0 dBm
All values in dBc below input LO level measured at RF port.

Outline Drawing



NOTES:

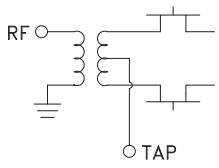
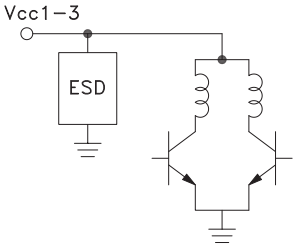
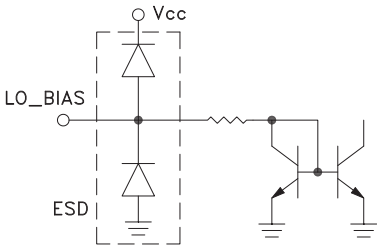
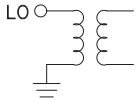
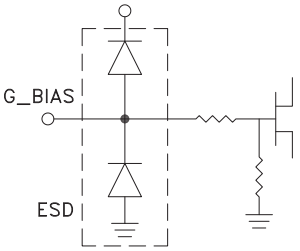
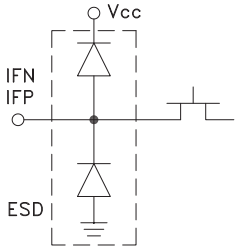
1. PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
2. LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY.
3. LEAD AND GROUND PADDLE PLATING: 100% MATTE TIN.
4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
5. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
6. PAD BURR LENGTH SHALL BE 0.15mm MAX. PAD BURR HEIGHT SHALL BE 0.25mm MAX.
7. PACKAGE WARP SHALL NOT EXCEED 0.05mm
8. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
9. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

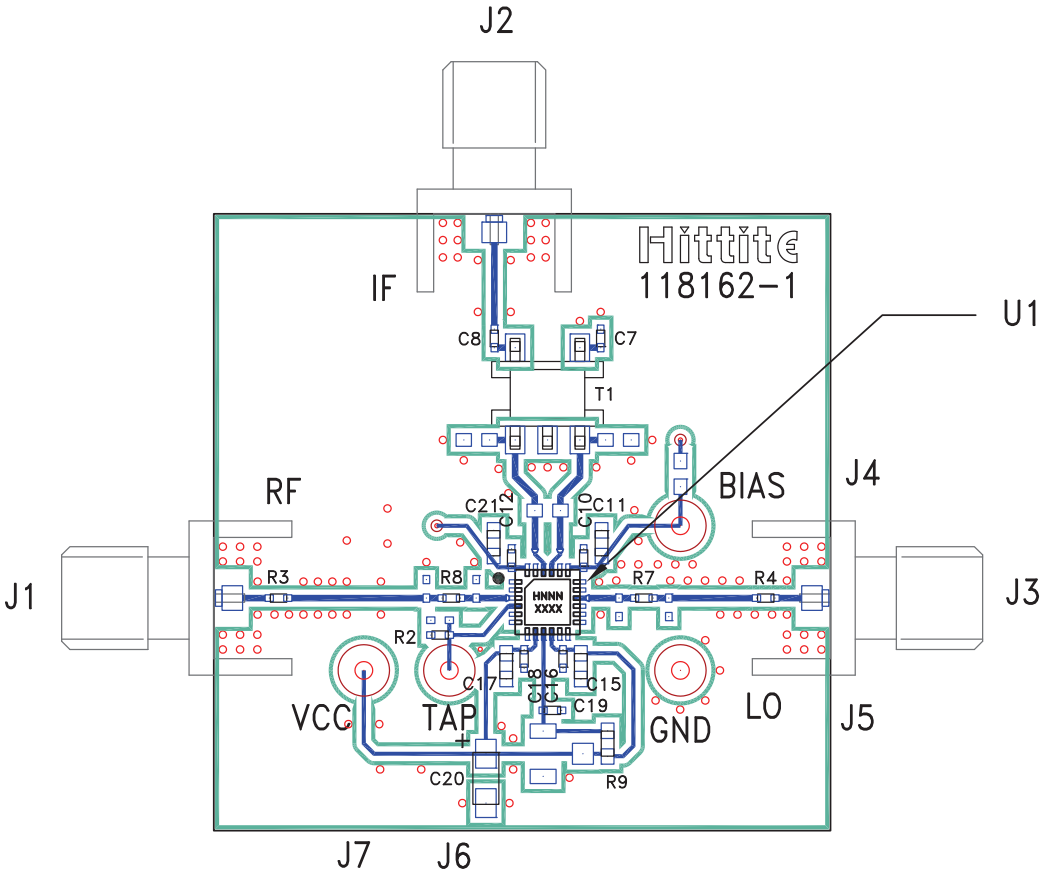
Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC685LP4	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	H685 XXXX
HMC685LP4E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H685 XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 6, 7, 11 - 14, 18, 20, 23	N/C	No connection. These pins may be connected to RF ground. Performance will not be affected.	
2, 5, 15, 17	GND	Package bottom must be connected to RF/DC ground.	
3	RF	This pin is matched single-ended 50 Ohm and DC shorted to ground through a balun.	
4	TAP	Center tap of secondary side of the internal RF balun. Short to ground with a zero ohm close to the IC.	
8, 10, 24	Vcc1, Vcc2, Vcc3	Power supply voltage. See application circuit for required external components.	
9	LO_BIAS	LO buffer current adjustment pin. Adjust the LO buffer current through the external resistor R9 shown in the application circuit (connect 270 Ohms for nominal operation). This adjustment allows for a trade-off between power dissipation and linearity performance of the converter.	
16	LO	This pin is matched single-ended 50 Ohm and DC shorted to ground through a balun.	
19	G_BIAS	External bias. See application circuit for recommended external components. Apply +2.5V for nominal operation at 5V supply voltage. G_Bias can be set to between 0 and 5Vdc. The G_bias pin has an internal 15K ohm resistance to ground. This adjustment allows for a trade off between conversion loss and linearity performance of the converter (see figures CG, IP3 vs. G-Bias).	
21, 22	IFN, IFP	Differential IF input / output pins matched to differential 50 Ohms. For applications not requiring operation to DC an off chip DC blocking capacitor should be used.	

Evaluation PCB

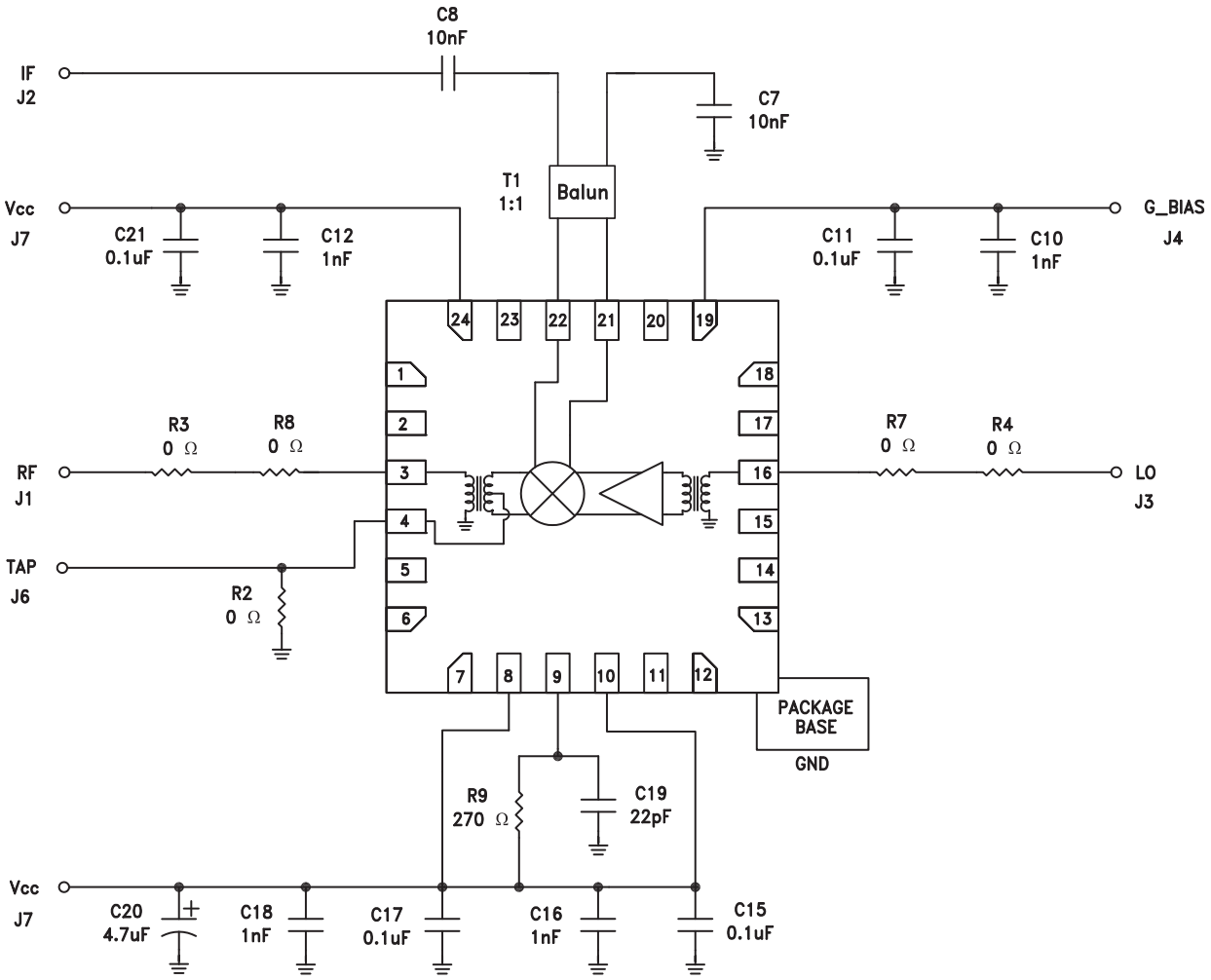


List of Materials for Evaluation PCB 119935 [1]

Item	Description
J1 - J3	SMA Connector
J4 - J7	DC Pin
C19	22 pF Capacitor, 0402 Pkg.
C7, C8	10 nF Capacitor, 0402 Pkg.
C10, C12, C16, C18	1 nF Capacitor, 0402 Pkg.
C11, C15, C17, C21	0.1 µF Capacitor, 0402 Pkg.
C20	4.7 µF Case A, Tantulum
R2 - R4, R7, R8	0 Ohm Resistor, 0402 Pkg.
R9	270 Ohm Resistor, 0603 Pkg.
T1	1:1 Transformer - Tyco MABA CT0039
U1	HMC685LP4(E) Downconverter
PCB [2]	118162 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25R, FR4

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Application Circuit