



BUK764R0-40E

N-channel TrenchMOS standard level FET

28 July 2016

Product data sheet

1. General description

Standard level N-channel MOSFET in a SOT404 package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

2. Features and benefits

- AEC Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True standard level gate with VGS(th) rating of greater than 1V at 175 °C

3. Applications

- 12 V Automotive systems
- Motors, lamps and solenoid control
- Start-Stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V _{DS}	drain-source voltage	T _J ≥ 25 °C; T _J ≤ 175 °C		-	-	40	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2	[1]	-	-	75	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1		-	-	182	W
Static characteristics							
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _J = 25 °C; Fig. 11		-	3.3	4	mΩ
Dynamic characteristics							
Q _{GD}	gate-drain charge	V _{GS} = 10 V; I _D = 25 A; V _{DS} = 32 V; Fig. 13 ; Fig. 14		-	15.5	-	nC

[1] Continuous current is limited by package.

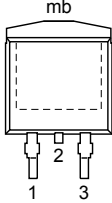


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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 D2PAK (SOT404)	 mbb076
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK764R0-40E	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK764R0-40E	BUK764R0-40E

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$		-	40	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$		-	40	V
V_{GS}	gate-source voltage	$T_j \leq 175\text{ °C}$; DC		-20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1		-	182	W
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; Fig. 2	[1]	-	75	A
		$T_{mb} = 100\text{ °C}$; $V_{GS} = 10\text{ V}$; Fig. 2	[1]	-	75	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Fig. 3		-	620	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C

Symbol	Parameter	Conditions		Min	Max	Unit
Source-drain diode						
I_S	source current	$T_{mb} = 25\text{ }^{\circ}\text{C}$	[1]	-	75	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ }^{\circ}\text{C}$		-	620	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 75\text{ A}$; $V_{sup} \leq 40\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$; unclamped; Fig. 4	[2][3]	-	302	mJ

[1] Continuous current is limited by package.

[2] Single-pulse avalanche rating limited by maximum junction temperature of $175\text{ }^{\circ}\text{C}$.

[3] Refer to application note AN10273 for further information.

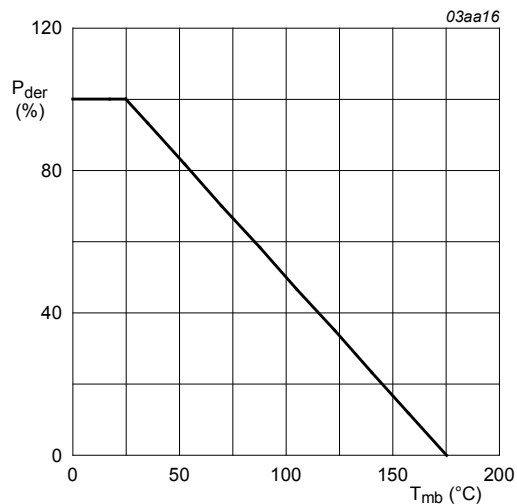
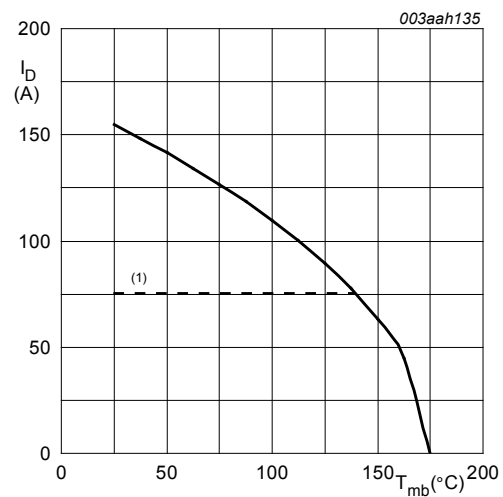


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100\%$$



(1) Capped at 75A due to package

Fig. 2. Continuous drain current as a function of mounting base temperature

$$V_{GS} \geq 10\text{ V}$$

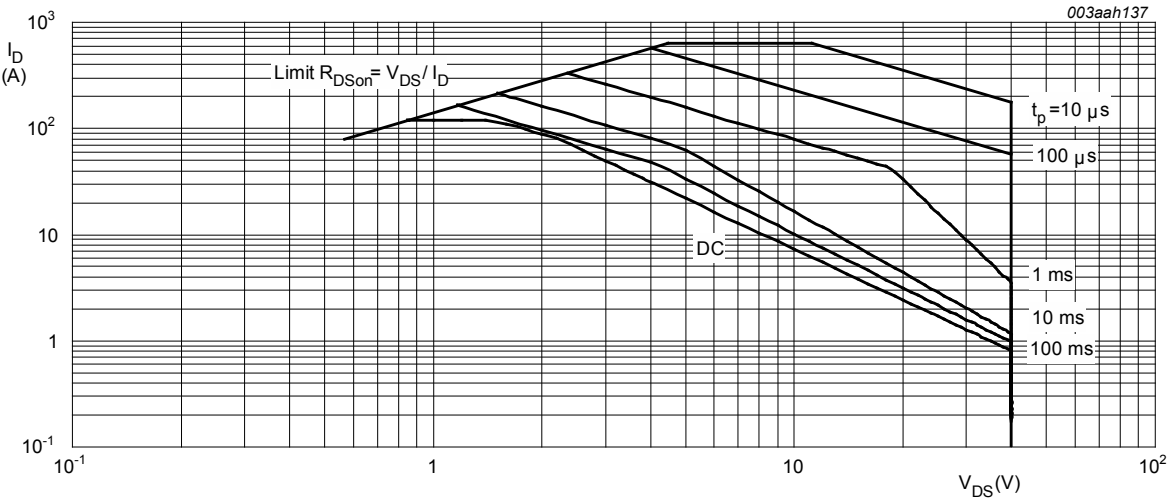


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage
 $T_{mb} = 25^{\circ}\text{C}$; I_{DM} is a single pulse

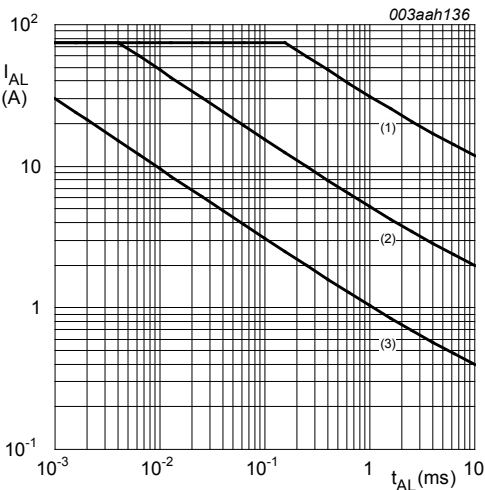
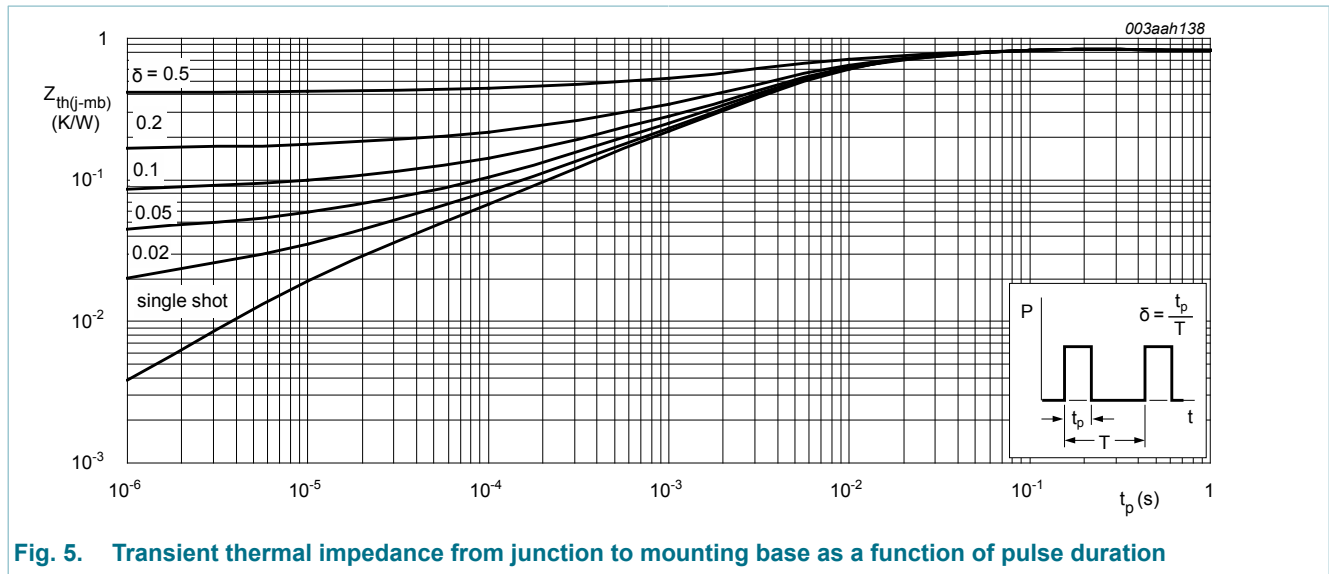


Fig. 4. Single pulse avalanche rating; avalanche current as a function of avalanche time
 (1) $T_j(\text{init}) = 25^{\circ}\text{C}$; (2) $T_j(\text{init}) = 150^{\circ}\text{C}$; (3) Repetitive Avalanche

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	-	0.82	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint; mounted on a printed-circuit board	-	50	-	K/W



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C}$		40	-	-	V
		$I_D = 250\text{ }\mu\text{A}; V_{GS} = 0\text{ V}; T_j = -55\text{ }^\circ\text{C}$		36	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}; V_{DS} = V_{GS}; T_j = 25\text{ }^\circ\text{C};$ Fig. 9; Fig. 10		2.4	3	4	V
		$I_D = 1\text{ mA}; V_{DS} = V_{GS}; T_j = -55\text{ }^\circ\text{C};$ Fig. 10		-	-	4.5	V
		$I_D = 1\text{ mA}; V_{DS} = V_{GS}; T_j = 175\text{ }^\circ\text{C};$ Fig. 10		1	-	-	V
I_{DSS}	drain leakage current	$V_{DS} = 40\text{ V}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C}$		-	0.12	1	μA
		$V_{DS} = 40\text{ V}; V_{GS} = 0\text{ V}; T_j = 175\text{ }^\circ\text{C}$		-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = 20\text{ V}; V_{DS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C}$		-	2	100	nA
		$V_{GS} = -20\text{ V}; V_{DS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C}$		-	2	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ }^\circ\text{C};$ Fig. 11		-	3.3	4	m Ω
		$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 175\text{ }^\circ\text{C};$ Fig. 12; Fig. 11		-	-	7.6	m Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	$I_D = 25\text{ A}; V_{DS} = 32\text{ V}; V_{GS} = 10\text{ V};$ Fig. 13; Fig. 14		-	54	-	nC
Q_{GS}	gate-source charge			-	13.6	-	nC
Q_{GD}	gate-drain charge			-	15.5	-	nC

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz; T _j = 25 °C; Fig. 15		-	3304	4405	pF
C _{oss}	output capacitance			-	634	761	pF
C _{rss}	reverse transfer capacitance			-	333	456	pF
t _{d(on)}	turn-on delay time	V _{DS} = 30 V; R _L = 1.2 Ω; V _{GS} = 10 V; R _{G(ext)} = 5 Ω		-	22	-	ns
t _r	rise time			-	20	-	ns
t _{d(off)}	turn-off delay time			-	43	-	ns
t _f	fall time			-	20	-	ns
L _D	internal drain inductance	from upper edge of drain mounting base to center of die		-	2.5	-	nH
L _S	internal source inductance	from source lead to source bonding pad		-	7.5	-	nH
Source-drain diode							
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _j = 25 °C; Fig. 16		-	0.84	1.2	V
t _{rr}	reverse recovery time	I _S = 20 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V;		-	31.1	-	ns
Q _r	recovered charge	V _{DS} = 25 V		-	28.9	-	nC

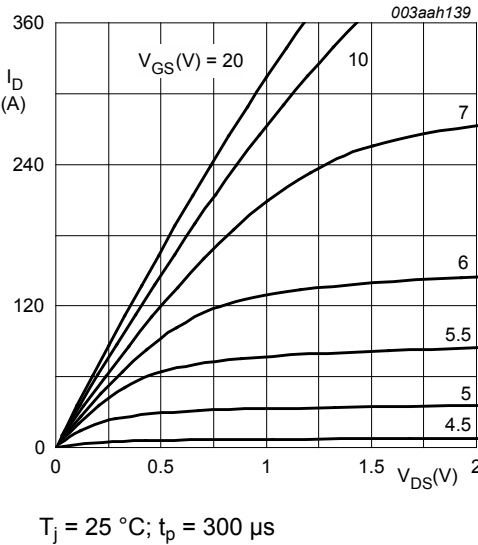


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

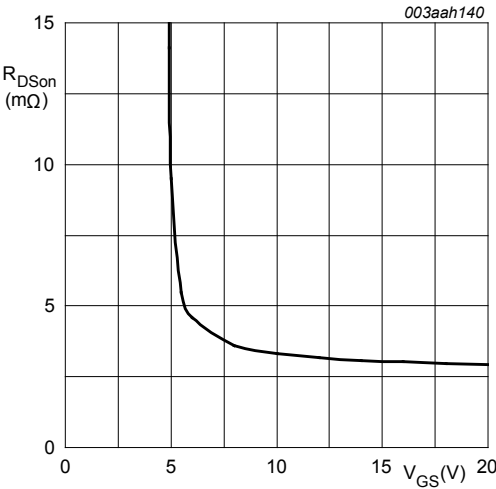


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25\text{ °C}; I_D = 25\text{ A}$

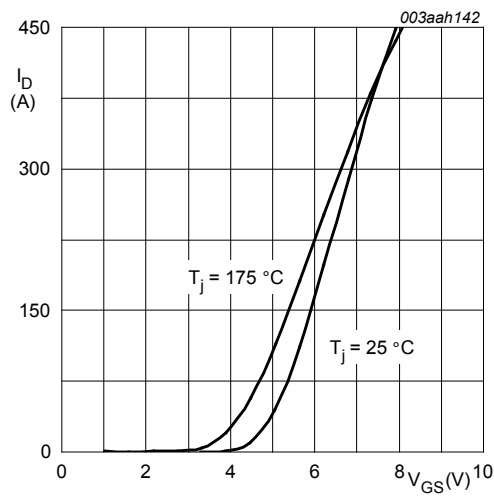


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$V_{DS} = 10V$

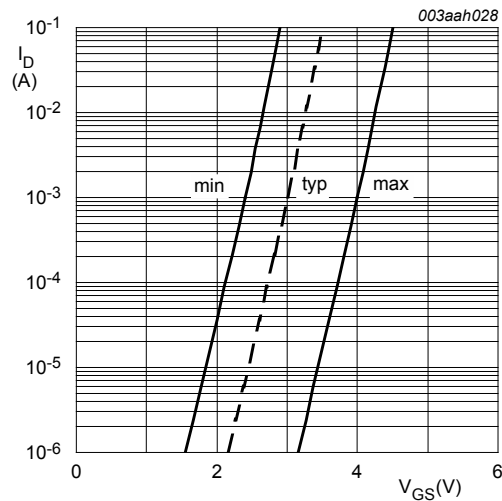


Fig. 9. Sub-threshold drain current as a function of gate-source voltage

$T_J = 25^{\circ}C; V_{DS} = 5V$

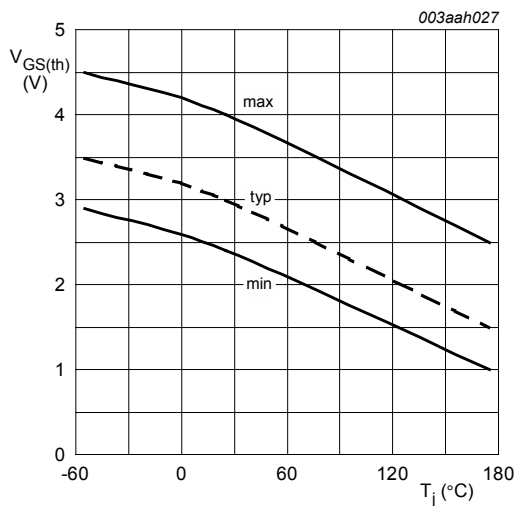


Fig. 10. Gate-source threshold voltage as a function of junction temperature

$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

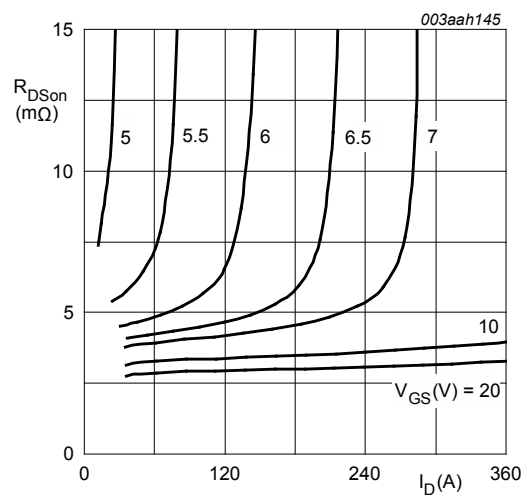


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

$T_J = 25^{\circ}C; t_p = 300 \mu s$

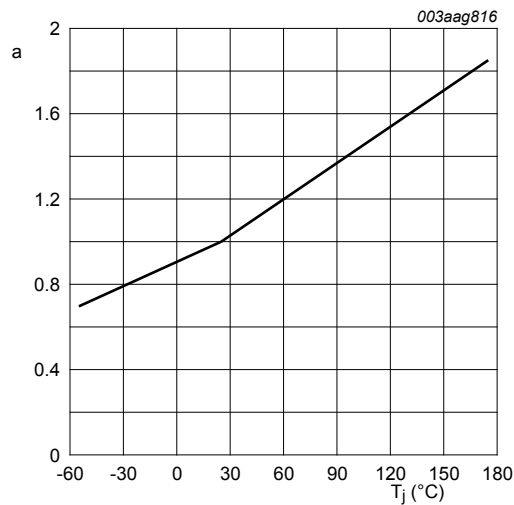


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon}(25^{\circ}\text{C})}$$

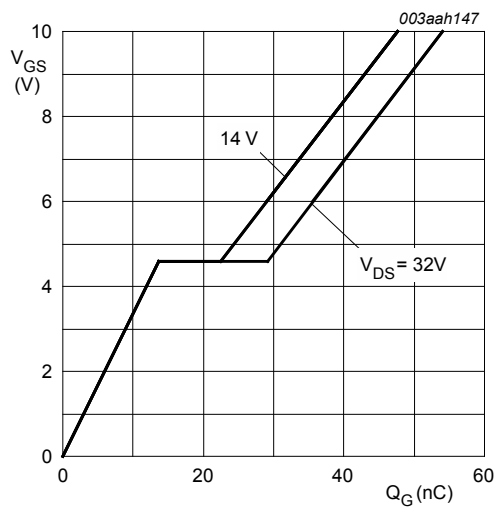


Fig. 14. Gate-source voltage as a function of gate charge; typical values

$$T_j = 25^{\circ}\text{C}; I_D = 25\text{ A}$$

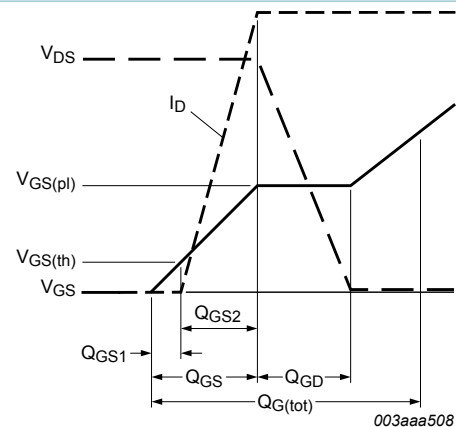


Fig. 13. Gate charge waveform definitions

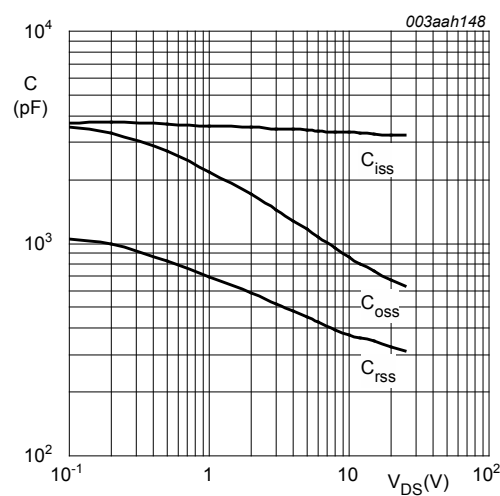


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$$

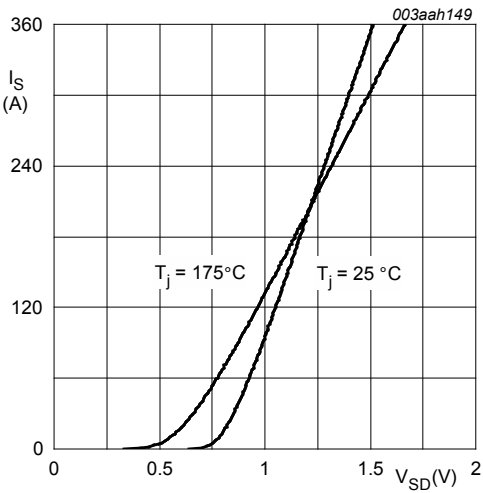


Fig. 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values
 $V_{GS} = 0\text{V}$

11. Package outline

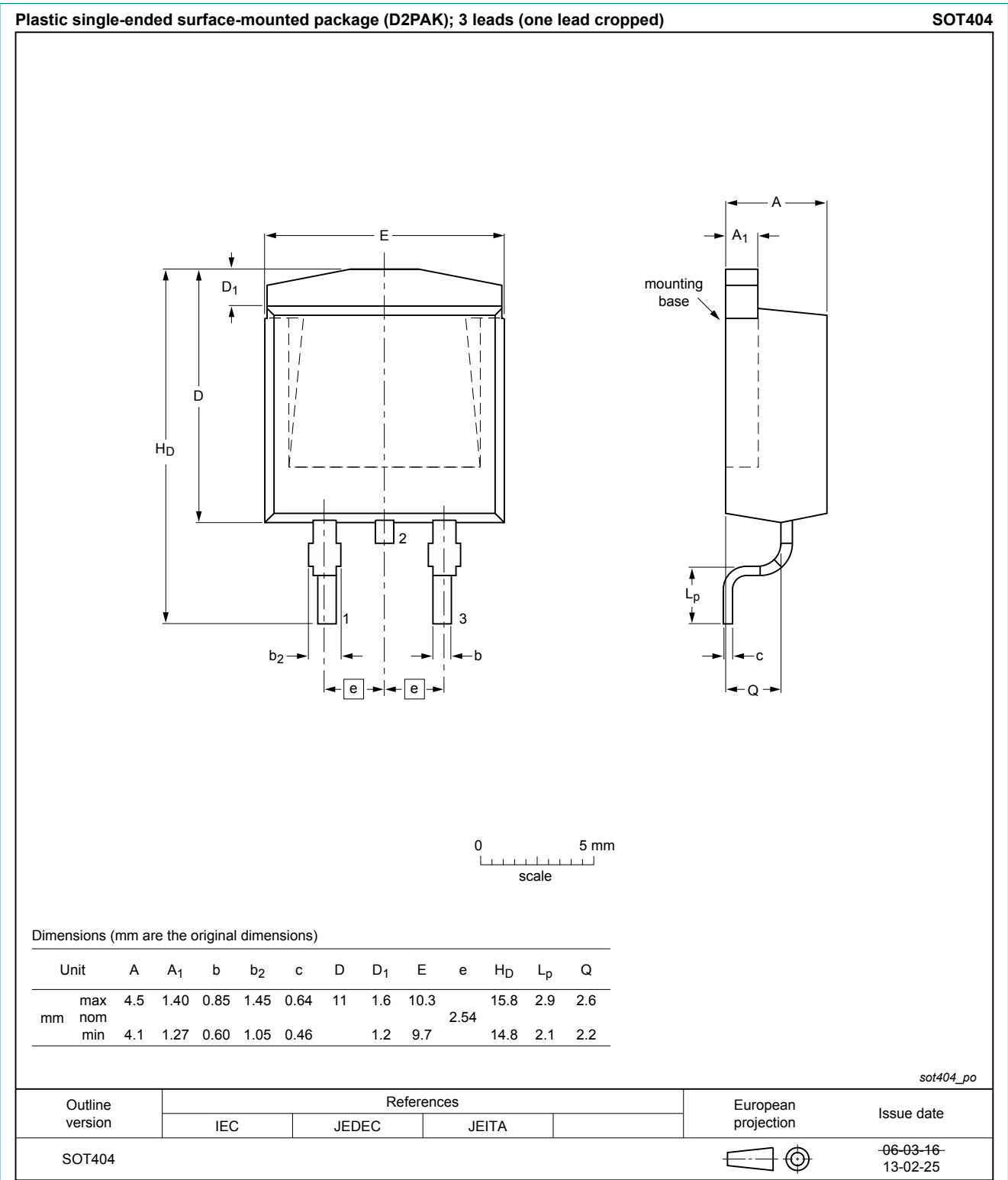


Fig. 17. Package outline D2PAK (SOT404)

12. Legal information

12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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