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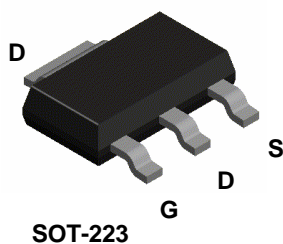
## NDT3055 N-Channel Enhancement Mode Field Effect Transistor

### General Description

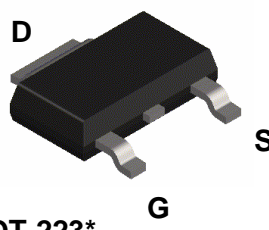
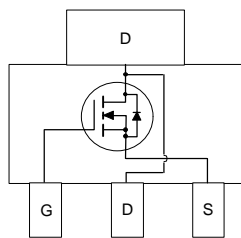
These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as DC motor control and DC/DC conversion where fast switching, low in-line power loss, and resistance to transients are needed.

### Features

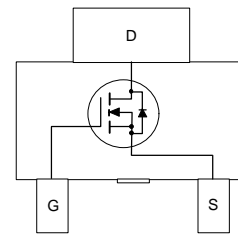
- 4 A, 60 V.  $R_{DS(ON)} = 0.100 \Omega @ V_{GS} = 10 \text{ V}$ .
- High density cell design for extremely low  $R_{DS(ON)}$ .
- High power and current handling capability in a widely used surface mount package.



SOT-223



SOT-223\*  
(J23Z)



### Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	NDT3055	Units
$V_{DSS}$	Drain-Source Voltage	60	V
$V_{GSS}$	Gate-Source Voltage - Continuous	$\pm 20$	V
$I_D$	Maximum Drain Current - Continuous (Note 1a)	4	A
	- Pulsed	25	
$P_D$	Maximum Power Dissipation (Note 1a)	3	W
	(Note 1b)	1.3	
	(Note 1c)	1.1	
$T_J, T_{STG}$	Operating and Storage Temperature Range	-65 to 150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	42	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	12	$^\circ\text{C/W}$

\* Order option J23Z for cropped center drain lead.

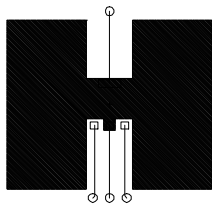
**Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	60			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		63		mV/°C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 48\text{ V}, V_{GS} = 0\text{ V}$ $T_J = 125^\circ\text{C}$			10	$\mu\text{A}$
					100	$\mu\text{A}$
$I_{GSSF}$	Gate - Body Leakage, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA
$I_{GSSR}$	Gate - Body Leakage, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$			-100	nA
<b>ON CHARACTERISTICS</b> (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$ $T_J = 125^\circ\text{C}$	2	3	4	V
			1.5	2.4	3	
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 4\text{ A}$ $T_J = 125^\circ\text{C}$		0.084	0.1	$\Omega$
				0.14	0.18	
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 10\text{ V}$	15			A
$g_{FS}$	Forward Transconductance	$V_{DS} = 15\text{ V}, I_D = 4\text{ A}$		6		S
<b>DYNAMIC CHARACTERISTICS</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		250		pF
$C_{oss}$	Output Capacitance			100		pF
$C_{rss}$	Reverse Transfer Capacitance			30		pF
<b>SWITCHING CHARACTERISTICS</b> (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	$V_{DD} = 25\text{ V}, I_D = 1.2\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 50\ \Omega$		10	25	ns
$t_r$	Turn - On Rise Time			18	50	ns
$t_{D(off)}$	Turn - Off Delay Time			37	65	ns
$t_f$	Turn - Off Fall Time			30	60	ns
$Q_g$	Total Gate Charge		$V_{DS} = 40\text{ V}, I_D = 4\text{ A},$ $V_{GS} = 10\text{ V}$		9	15
$Q_{gs}$	Gate-Source Charge			2.3		nC
$Q_{gd}$	Gate-Drain Charge			2.6		nC
<b>DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b>						
$I_S$	Maximum Continuous Drain-Source Diode Forward Current				2.5	A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2.5\text{ A}$ (Note 2)		0.85	1.2	V

Notes:

- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.

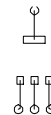
Typical  $R_{\theta JA}$  using the board layouts shown below on FR-4 PCB in a still air environment:



a.  $42^\circ\text{C/W}$  when mounted on a  $1\text{ in}^2$  pad of 2oz Cu.



b.  $95^\circ\text{C/W}$  when mounted on a  $0.066\text{ in}^2$  pad of 2oz Cu.



c.  $110^\circ\text{C/W}$  when mounted on a  $0.00123\text{ in}^2$  pad of 2oz Cu.

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$

## Typical Electrical Characteristics

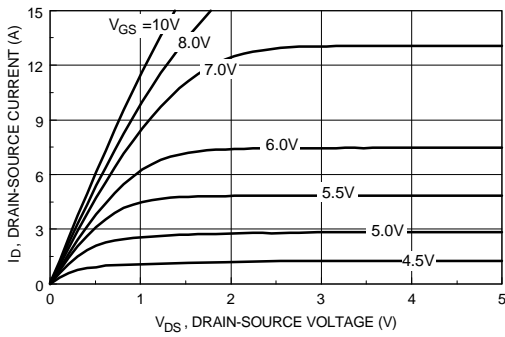


Figure 1. On-Region Characteristics.

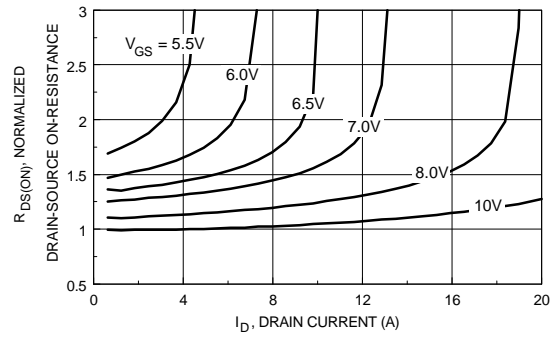


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

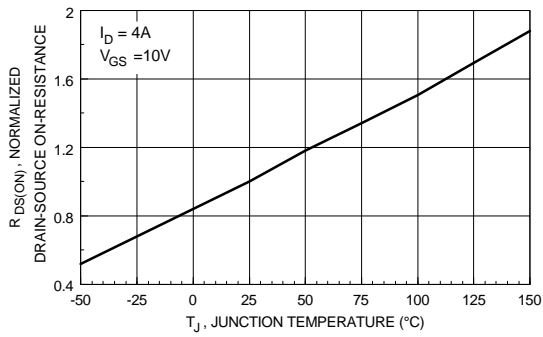


Figure 3. On-Resistance Variation with Temperature.

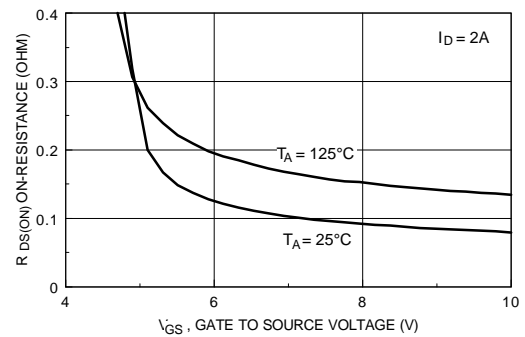


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

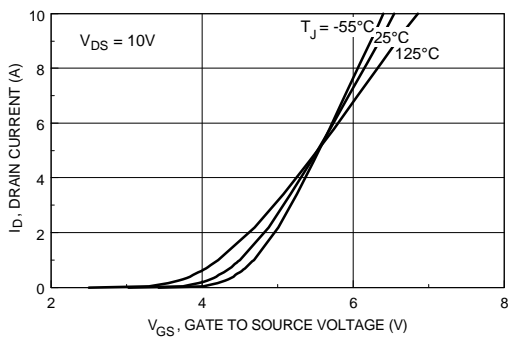


Figure 5. Transfer Characteristics.

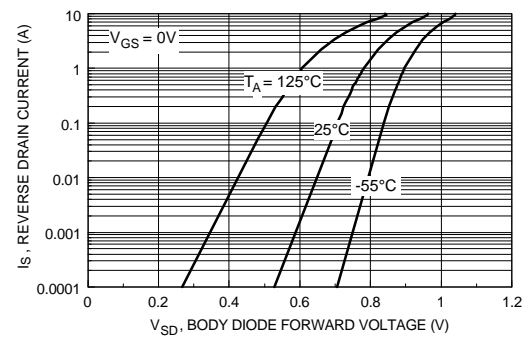


Figure 6. Body Diode Forward Voltage Variation with Current and Temperature.

## Typical Electrical Characteristics (continued)

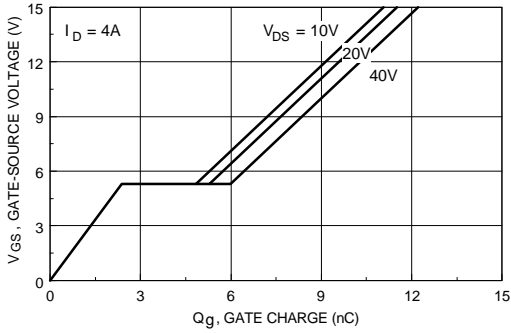


Figure 7. Gate Charge Characteristics.

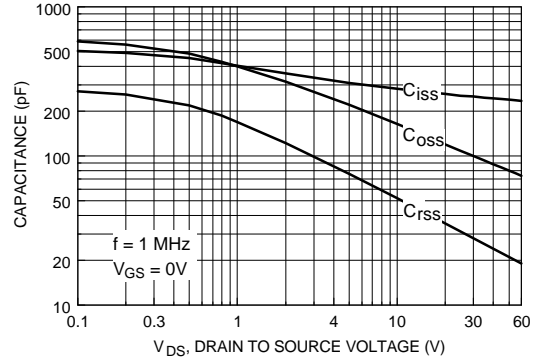


Figure 8. Capacitance Characteristics.

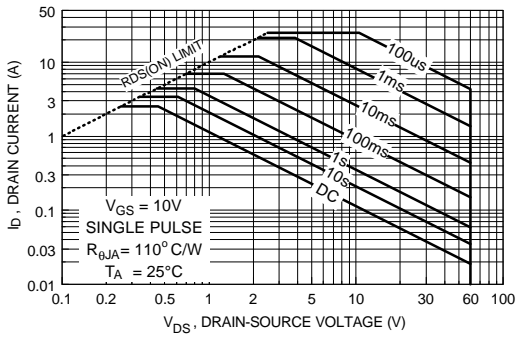


Figure 9. Maximum Safe Operating Area.

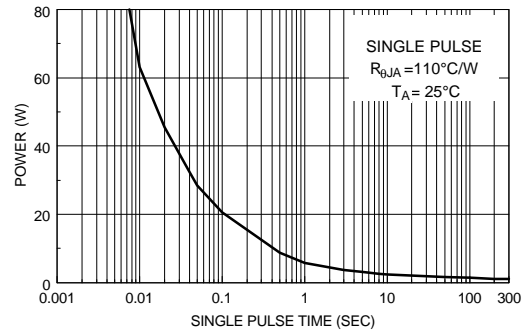


Figure 10. Single Pulse Maximum Power Dissipation.

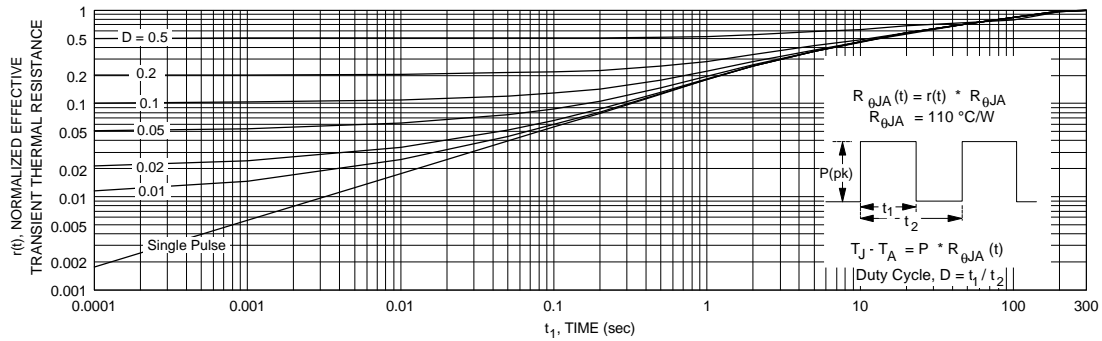
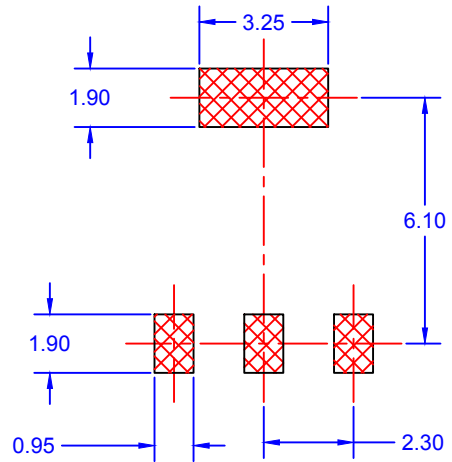
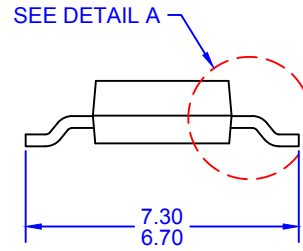
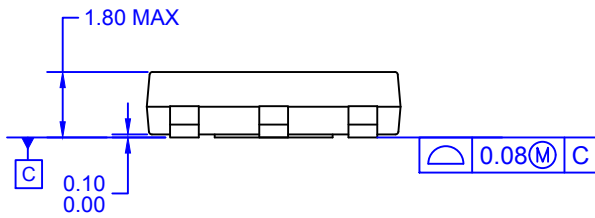


Figure 11. Transient Thermal Response Curve.

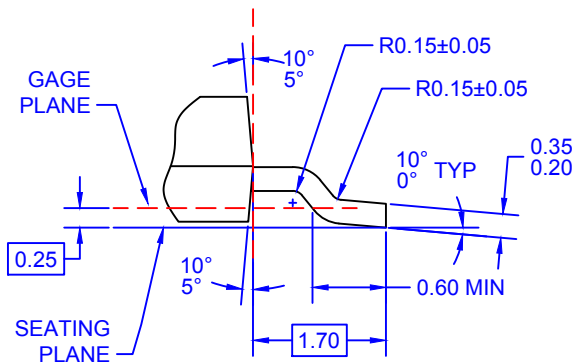
Thermal characterization performed using the conditions described in note 1c.  
Transient thermal response will change depending on the circuit board design.



LAND PATTERN RECOMMENDATION



- NOTES: UNLESS OTHERWISE SPECIFIED  
 A) DRAWING BASED ON JEDEC REGISTRATION TO-261C, VARIATION AA.  
 B) ALL DIMENSIONS ARE IN MILLIMETERS.  
 C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.  
 D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.  
 E) LANDPATTERN NAME: SOT230P700X180-4BN  
 F) DRAWING FILENAME: MKT-MA04AREV3



DETAIL A  
 SCALE: 2:1



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