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October 2015

FDG327NZ

# FDG327NZ

## 20V N-Channel PowerTrench<sup>®</sup> MOSFET

### General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized use in small switching regulators, providing an extremely low  $R_{DS(ON)}$  and gate charge ( $Q_G$ ) in a small package.

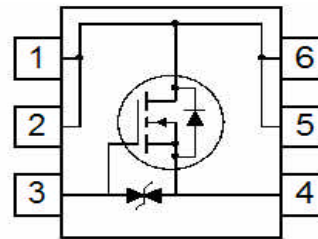
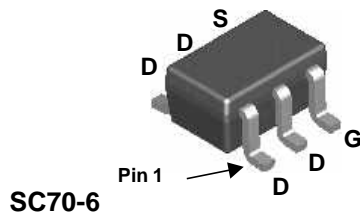
### Applications

- DC/DC converter
- Power management
- Load switch



### Features

- 1.5 A, 20 V.  $R_{DS(ON)} = 90 \text{ m}\Omega @ V_{GS} = 4.5 \text{ V}$ .  
 $R_{DS(ON)} = 100 \text{ m}\Omega @ V_{GS} = 2.5 \text{ V}$   
 $R_{DS(ON)} = 140 \text{ m}\Omega @ V_{GS} = 1.8 \text{ V}$
- Fast switching speed
- Low gate charge
- High performance trench technology for extremely low  $R_{DS(ON)}$
- High power and current handling capability.



### Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain-Source Voltage	20	V
$V_{GSS}$	Gate-Source Voltage	$\pm 8$	
$I_D$	Drain Current – Continuous (Note 1a) – Pulsed	1.5	A
		6	
$P_D$	Power Dissipation for Single Operation (Note 1a) (Note 1b)	0.42	W
		0.38	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	300	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1b)	333	

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
.37	FDG327NZ	7"	8mm	3000 units

**Electrical Characteristics** $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		11		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 16\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate–Body Leakage	$V_{GS} = \pm 8\text{ V}, V_{DS} = 0\text{ V}$			$\pm 10$	$\mu\text{A}$

**On Characteristics (Note 2)**

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	0.4	0.7	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		-2		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 4.5\text{ V}, I_D = 1.5\text{ A}$ $V_{GS} = 2.5\text{ V}, I_D = 1.4\text{ A}$ $V_{GS} = 1.8\text{ V}, I_D = 1.2\text{ A}$ $V_{GS} = 4.5\text{ V}, I_D = 1.5\text{ A}, T_J = 125^\circ\text{C}$		68 77 90 86	90 100 140 123	m $\Omega$
$I_{D(on)}$	On–State Drain Current	$V_{GS} = 4.5\text{ V}, V_{DS} = 5\text{ V}$	3			A
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 1.5\text{ A}$		9		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}$		412		pF
$C_{oss}$	Output Capacitance	$f = 1.0\text{ MHz}$		81		pF
$C_{rss}$	Reverse Transfer Capacitance			44		pF
$R_G$	Gate Resistance	$V_{GS} = 15\text{ mV}, f = 1.0\text{ MHz}$		1.9		$\Omega$

**Switching Characteristics (Note 2)**

$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 10\text{ V}, I_D = 1\text{ A},$		6.2	13	ns
$t_r$	Turn–On Rise Time	$V_{GS} = 4.5\text{ V}, R_{GEN} = 6\ \Omega$		2.3	10	ns
$t_{d(off)}$	Turn–Off Delay Time			18	33	ns
$t_f$	Turn–Off Fall Time			2.9	10	ns
$Q_g$	Total Gate Charge	$V_{DS} = 10\text{ V}, I_D = 1.5\text{ A},$		4.2	6	nC
$Q_{gs}$	Gate–Source Charge	$V_{GS} = 4.5\text{ V}$		0.4		nC
$Q_{gd}$	Gate–Drain Charge			1		nC

**Drain–Source Diode Characteristics and Maximum Ratings**

$V_{SD}$	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 0.32\text{ A}$ (Note 2)		0.6	1.2	V
$t_{rr}$	Diode Reverse Recovery Time	$I_F = 1.5\text{ A}, di_F/dt = 100\text{ A}/\mu\text{s}$		4		nS
$Q_{rr}$	Diode Reverse Recovery Charge			2		nC

**Notes:**

1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



- a)  $300^\circ\text{C}/\text{W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper.



- b)  $333^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 $\mu\text{s}$ , Duty Cycle < 2.0%

## Typical Characteristics

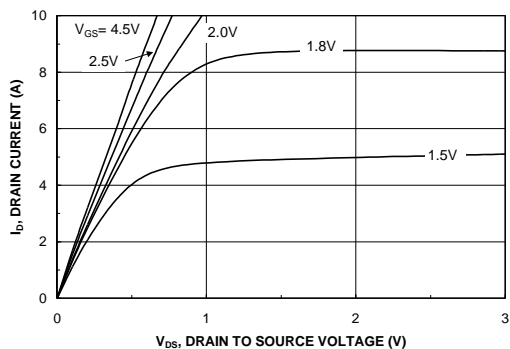


Figure 1. On-Region Characteristics.

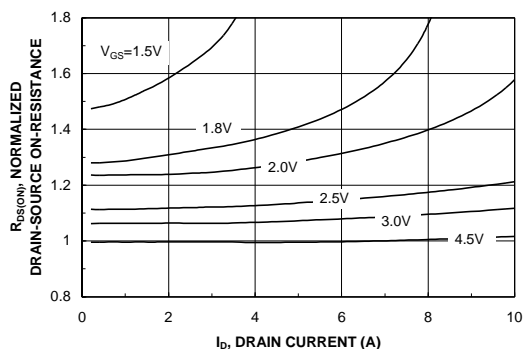


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

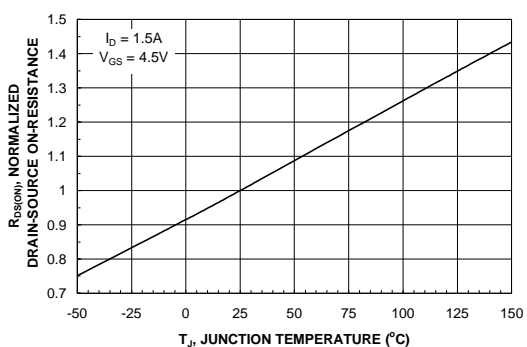


Figure 3. On-Resistance Variation with Temperature.

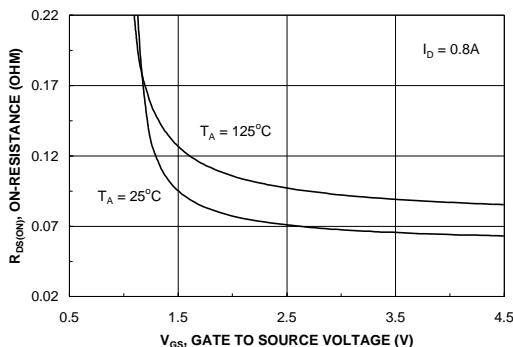


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

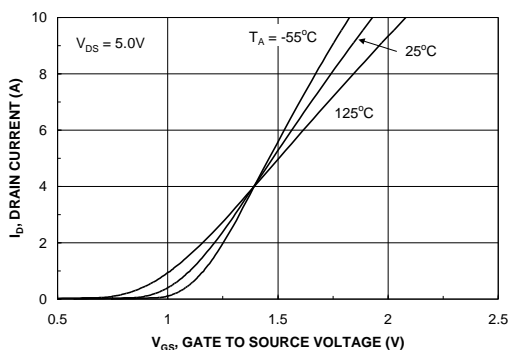


Figure 5. Transfer Characteristics.

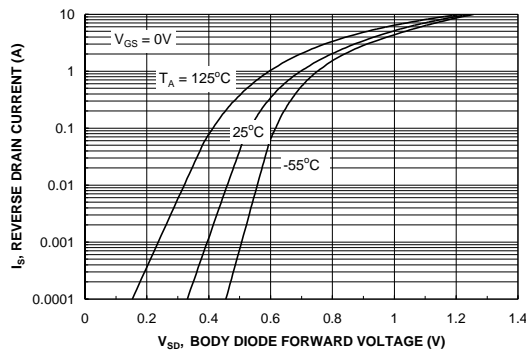


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

### Typical Characteristics

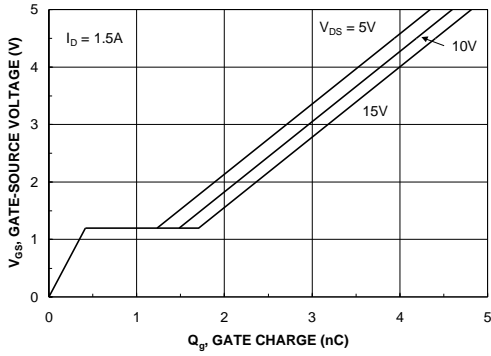


Figure 7. Gate Charge Characteristics.

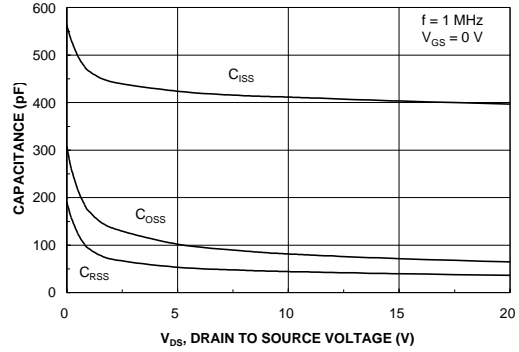


Figure 8. Capacitance Characteristics.

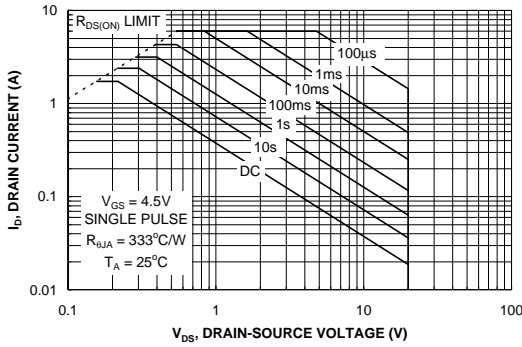


Figure 9. Maximum Safe Operating Area.

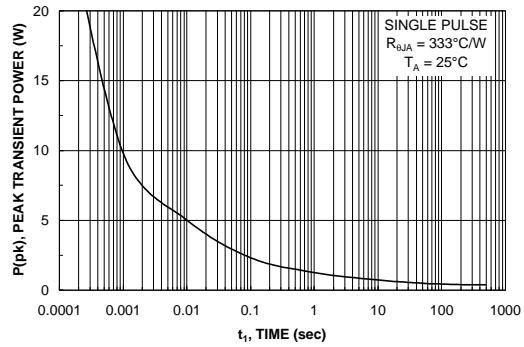


Figure 10. Single Pulse Maximum Power Dissipation.

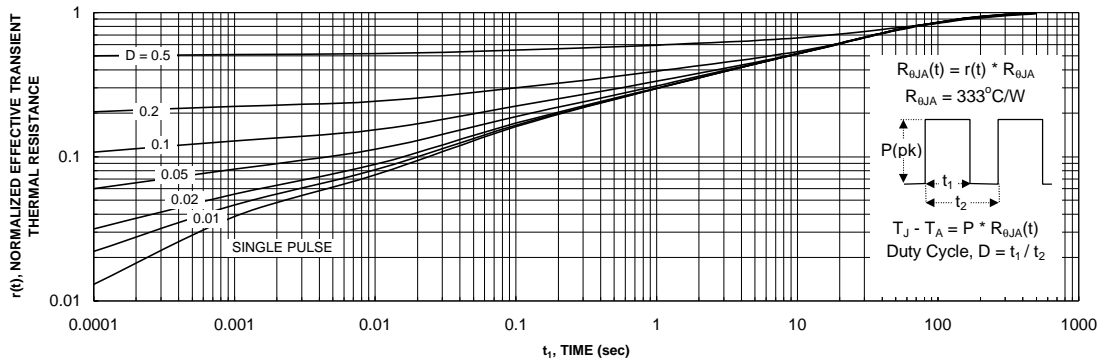
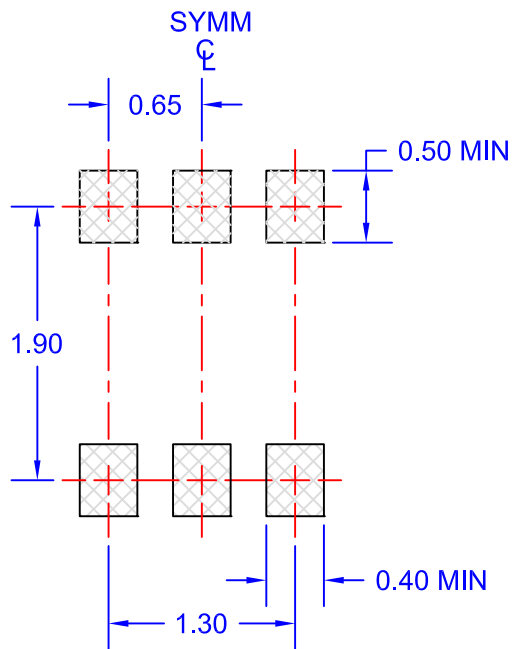
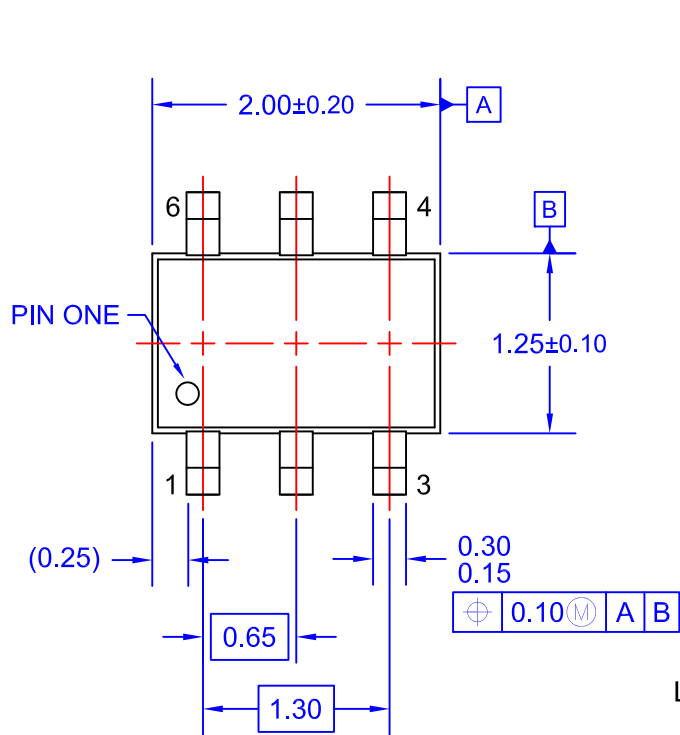
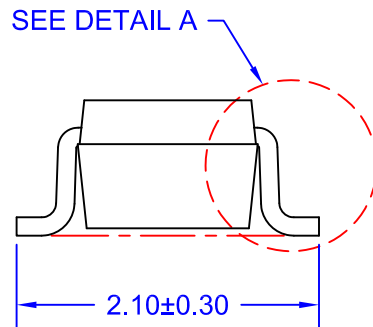
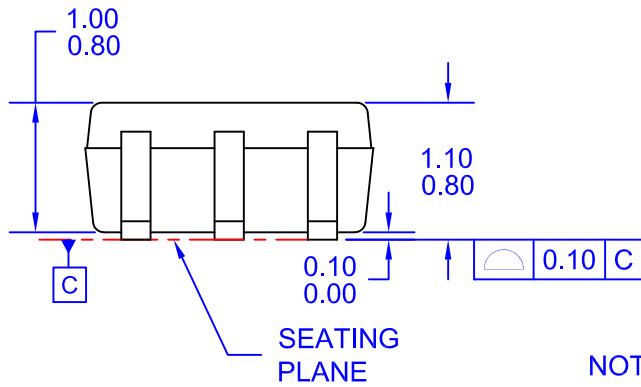


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.



LAND PATTERN RECOMMENDATION

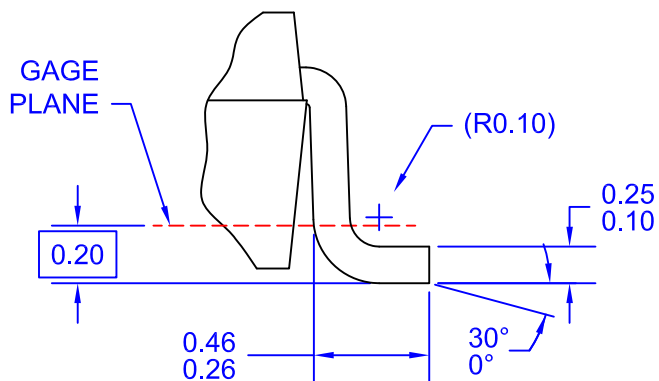


NOTES: UNLESS OTHERWISE SPECIFIED  
 A) THIS PACKAGE CONFORMS TO EIAJ SC-88, 1996.

B) ALL DIMENSIONS ARE IN MILLIMETERS.  
 C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.

D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009

E) DRAWING FILENAME: MKT-MAA06AREV7



DETAIL A  
 SCALE: 60X



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