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74VHC138 3-to-8 Decoder/Demultiplexer

General Description

The VHC138 is an advanced high speed CMOS 3-to-8 decoder/demultiplexer fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

When the device is enabled, 3 binary select inputs (A_0 , A_1 and A_2) determine which one of the outputs (\overline{O}_0 – \overline{O}_7) will go LOW. When enable input E_3 is held LOW or either \overline{E}_1 or \overline{E}_2 is held HIGH, decoding function is inhibited and all outputs go HIGH. E_3 , \overline{E}_1 and \overline{E}_2 inputs are provided to ease cascade connection and for use as an address decoder for memory systems. An input protection circuit ensures that

0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

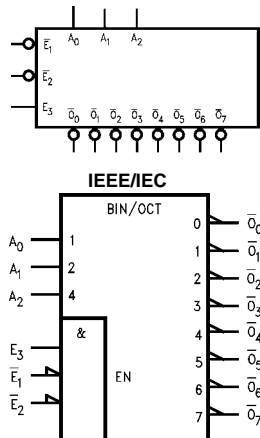
- High Speed: $t_{PD} = 5.7ns$ (typ) at $T_A = 25^\circ C$
- Low power dissipation: $I_{CC} = 4 \mu A$ (max.) at $T_A = 25^\circ C$
- High noise immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (min.)
- Power down protection provided on all inputs
- Pin and function compatible with 74HC138

Ordering Code:

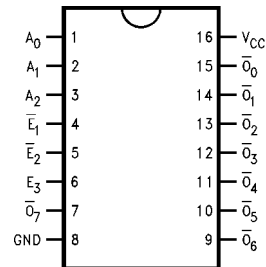
| Order Number | Package Number | Package Description |
|--------------|----------------|--|
| 74VHC138M | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| 74VHC138SJ | M16D | 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74VHC138MTC | MTC16 | 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| 74VHC138N | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



Pin Descriptions

| Pin Names | Description |
|-------------------------------------|----------------|
| A_0 – A_2 | Address Inputs |
| \overline{E}_1 – \overline{E}_2 | Enable Inputs |
| E_3 | Enable Input |
| \overline{O}_0 – \overline{O}_7 | Outputs |

Truth Table

| Inputs | | | | | | Outputs | | | | | | | |
|------------------|------------------|-------|-------|-------|-------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| \overline{E}_1 | \overline{E}_2 | E_3 | A_0 | A_1 | A_2 | \overline{O}_0 | \overline{O}_1 | \overline{O}_2 | \overline{O}_3 | \overline{O}_4 | \overline{O}_5 | \overline{O}_6 | \overline{O}_7 |
| H | X | X | X | X | X | H | H | H | H | H | H | H | H |
| X | H | X | X | X | X | H | H | H | H | H | H | H | H |
| X | X | L | X | X | X | H | H | H | H | H | H | H | H |
| L | L | H | L | L | L | L | H | H | H | H | H | H | H |
| L | L | H | H | L | L | H | L | H | H | H | H | H | H |
| L | L | H | L | H | L | H | H | L | H | H | H | H | H |
| L | L | H | H | H | L | H | H | H | L | H | H | H | H |
| L | L | H | L | L | H | H | H | H | H | L | H | H | H |
| L | L | H | H | L | H | H | H | H | H | H | L | H | H |
| L | L | H | L | H | H | H | H | H | H | H | H | L | H |
| L | L | H | H | H | H | H | H | H | H | H | H | H | L |

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial

Absolute Maximum Ratings (Note 1)

| | |
|---|--------------------------|
| Supply Voltage (V_{CC}) | -0.5V to +7.0V |
| DC Input Voltage (V_{IN}) | -0.5V to +7.0V |
| DC Output Voltage (V_{OUT}) | -0.5V to $V_{CC} + 0.5V$ |
| Input Diode Current (I_{IK}) | -20 mA |
| Output Diode Current (I_{OK}) | ± 20 mA |
| DC Output Current (I_{OUT}) | ± 25 mA |
| DC V_{CC} /GND Current (I_{CC}) | ± 75 mA |
| Storage Temperature (T_{STG}) | -65°C to +150°C |
| Lead Temperature (T_L) (Soldering, 10 seconds) | 260°C |

Recommended Operating Conditions (Note 2)

| | |
|---|----------------|
| Supply Voltage (V_{CC}) | 2.0V to +5.5V |
| Input Voltage (V_{IN}) | 0V to +5.5V |
| Output Voltage (V_{OUT}) | 0V to V_{CC} |
| Operating Temperature (T_{OPR}) | -40°C to +85°C |
| Input Rise and Fall Time (t_r, t_f) | |
| $V_{CC} = 3.3V \pm 0.3V$ | 0 ~ 100 ns/V |
| $V_{CC} = 5.0V \pm 0.5V$ | 0 ~ 20 ns/V |

Note 1: Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside databook specifications.

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

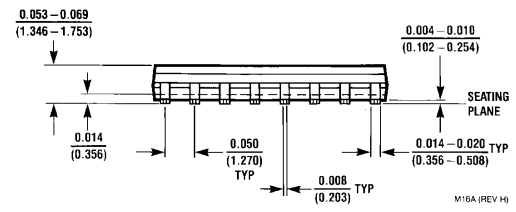
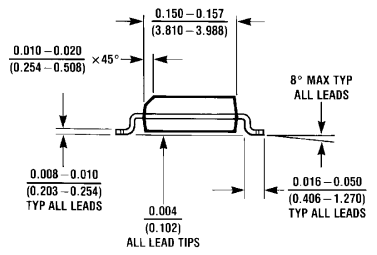
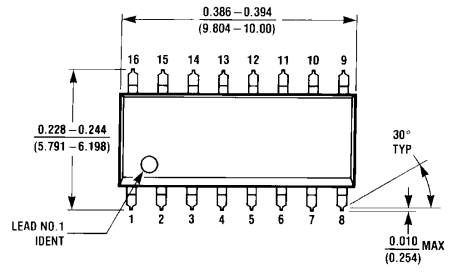
| Symbol | Parameter | V_{CC} (V) | $T_A = 25^\circ\text{C}$ | | | $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ | | Units | Conditions | |
|----------|---------------------------|------------------|--------------------------|------|----------------------|---|------|---------------|----------------------------------|--|
| | | | Min | Typ | Max | Min | Max | | | |
| V_{IH} | HIGH Level Input Voltage | 2.0 3.0 – 5.5 | 1.50 $0.7 V_{CC}$ | | | 1.50 $0.7 V_{CC}$ | | V | | |
| V_{IL} | LOW Level Input Voltage | 2.0 3.0 – 5.5 | | | 0.50 $0.3 V_{CC}$ | 0.50 $0.3 V_{CC}$ | | V | | |
| V_{OH} | HIGH Level Output Voltage | 2.0 | 1.9 | 2.0 | | 1.9 | | V | $V_{IN} = V_{IH}$ or V_{IL} | $I_{OH} = -50 \mu\text{A}$ |
| | | 3.0 | 2.9 | 3.0 | | 2.9 | | | | |
| | | 4.5 | 4.4 | 4.5 | | 4.4 | | V | | $I_{OH} = -4 \text{ mA}$ $I_{OH} = -8 \text{ mA}$ |
| | | 3.0 | 2.58 | | | 2.48 | | | | |
| 4.5 | 3.94 | | | 3.80 | | | | | | |
| V_{OL} | LOW Level Output Voltage | 2.0 | | 0.0 | 0.1 | | 0.1 | V | $V_{IN} = V_{IH}$ or V_{IL} | $I_{OL} = 50 \mu\text{A}$ |
| | | 3.0 | | 0.0 | 0.1 | | 0.1 | | | |
| | | 4.5 | | 0.0 | 0.1 | | 0.1 | V | | $I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$ |
| | | 3.0 | | | 0.36 | | 0.44 | | | |
| 4.5 | | | 0.36 | | 0.44 | | | | | |
| I_{IN} | Input Leakage Current | 0 – 5.5 | | | ± 0.1 | ± 1.0 | | μA | $V_{IN} = 5.5V$ or GND | |
| I_{CC} | Quiescent Supply Current | 5.5 | | | 4.0 | 40.0 | | μA | $V_{IN} = V_{CC}$ or GND | |

AC Electrical Characteristics

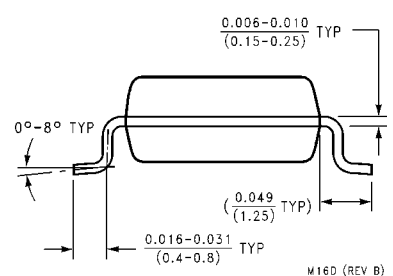
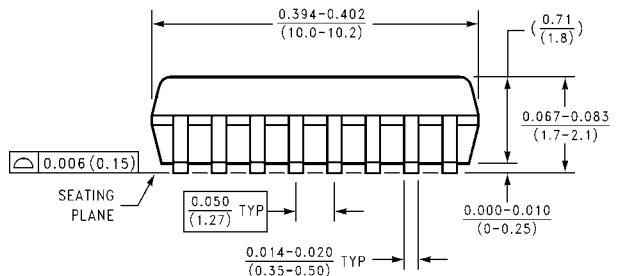
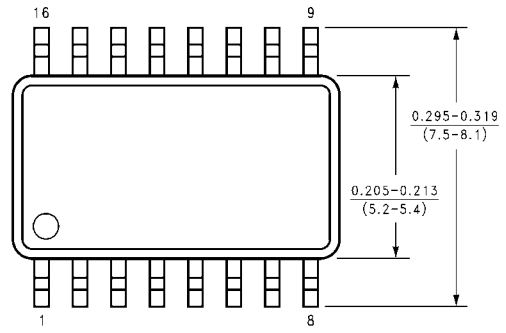
| Symbol | Parameter | V _{CC} (V) | T _A = 25°C | | | T _A = -40°C to +85°C | | Units | Conditions |
|------------------|---|------------------------|-----------------------|------|-----|---------------------------------|-----|------------------------|------------|
| | | | Min | Typ | Max | Min | Max | | |
| t _{PLH} | Propagation Delay A _n to \overline{O}_n | 3.3 ± 0.3 | 8.2 | 11.4 | 1.0 | 13.5 | ns | C _L = 15 pF | |
| t _{PHL} | | | 10.0 | 15.8 | 1.0 | 18.0 | | C _L = 50 pF | |
| | | 5.0 ± 0.5 | 5.7 | 8.1 | 1.0 | 9.5 | ns | C _L = 15 pF | |
| | | | 7.2 | 10.1 | 1.0 | 11.5 | | C _L = 50 pF | |
| t _{PLH} | Propagation Delay E ₃ to \overline{O}_n | 3.3 ± 0.3 | 8.1 | 12.8 | 1.0 | 15.0 | ns | C _L = 15 pF | |
| t _{PHL} | | | 10.6 | 16.3 | 1.0 | 18.5 | | C _L = 50 pF | |
| | | 5.0 ± 0.5 | 5.6 | 8.1 | 1.0 | 9.5 | ns | C _L = 15 pF | |
| | | | 7.1 | 10.1 | 1.0 | 11.5 | | C _L = 50 pF | |
| t _{PLH} | Propagation Delay \overline{E}_1 or \overline{E}_2 to \overline{O}_n | 3.3 ± 0.3 | 8.2 | 11.4 | 1.0 | 13.5 | ns | C _L = 15 pF | |
| t _{PHL} | | | 10.7 | 14.9 | 1.0 | 17.0 | | C _L = 50 pF | |
| | | 5.0 ± 0.5 | 5.8 | 8.1 | 1.0 | 9.5 | ns | C _L = 15 pF | |
| | | | 7.3 | 10.1 | 1.0 | 11.5 | | C _L = 50 pF | |
| C _{IN} | Input Capacitance | | 4 | 10 | | 10 | pF | V _{CC} = Open | |
| C _{PD} | Power Dissipation Capacitance | | 34 | | | | pF | (Note 3) | |

Note 3: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC (opr.)} = C_{PD} * V_{CC} * f_{IN} + I_{CC}.

Physical Dimensions inches (millimeters) unless otherwise noted

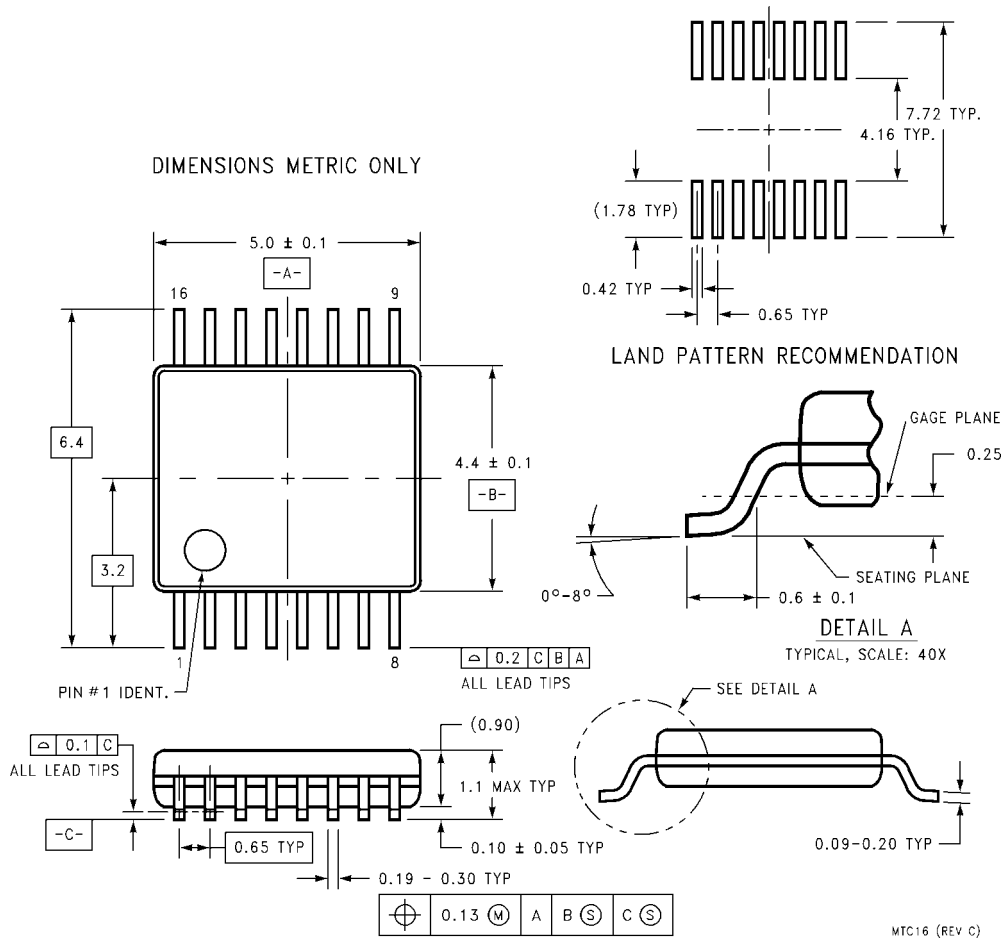


**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A**



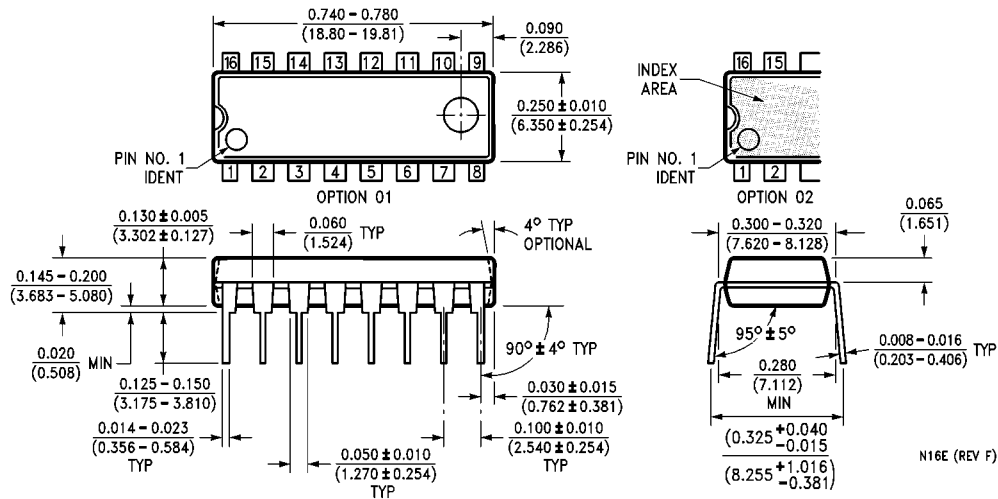
**16-Lead Small Outline Package (SOP) EIAJ TYPE II, 5.3mm Wide
Package Number M16D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16E

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