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April 2015

74LCX157
Low Voltage Quad 2-Input Multiplexer with 5 V Tolerant Inputs

Features

- 5 V Tolerant Inputs
- 2.3 V – 3.6 V, V_{CC} Specifications Provided
- 5.8 ns t_{PD} max. (V_{CC} = 3.3 V), 10 µA I_{CC} max.
- Power Down High Impedance Inputs and Outputs
- ±24 mA Output Drive (V_{CC} = 3.0 V)
- Implements Patented Noise/EMI Reduction Circuitry
- Latch-Up Performance Exceeds 500 mA
- ESD Performance:
  Human Body Model > 2000 V
  Machine Model > 200 V

General Description

The LCX157 is a high-speed quad 2-input multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four outputs present the selected data in the true (noninverted) form.

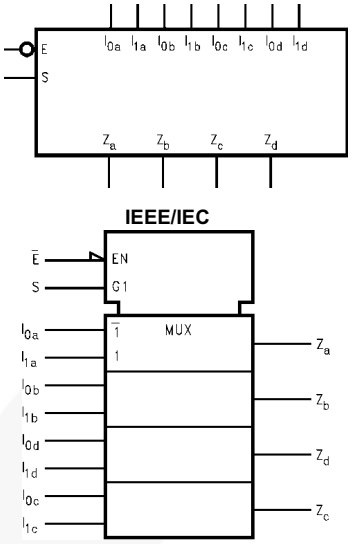
The LCX157 can also be used as a function generator.

The 74LCX157 is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

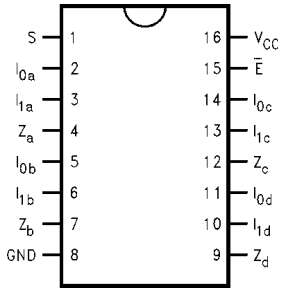
Ordering Information

Part Number	Top Mark	Package	Packing Method
74LCX157M	LCX157	SOIC 16L	Rail
74LCX157MX	LCX157	SOIC 16L	Tape and Reel
74LCX157MTC	LCX157	TSSOP 16L	Rail
74LCX157MTCX	LCX157	TSSOP 16L	Tape and Reel

Logic Symbols



Connection Diagram



Pin Descriptions

Pin Names	Description
I_{0a}–I_{0d}	Source 0 Data Inputs
I_{1a}–I_{1d}	Source 1 Data Inputs
$\overline{E}$	Enable Input
S	Select Input
Z_a–Z_d	Outputs

Functional Description

The LCX157 is a quad 2-input multiplexer. It selects four bits of data from two sources under the control of a common Select input (S). The Enable input ($\overline{E}$) is active-LOW. When $\overline{E}$ is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs. The LCX157 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$Z_a = \overline{E} \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S})$
$Z_b = \overline{E} \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$
$Z_c = \overline{E} \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S})$
$Z_d = \overline{E} \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$

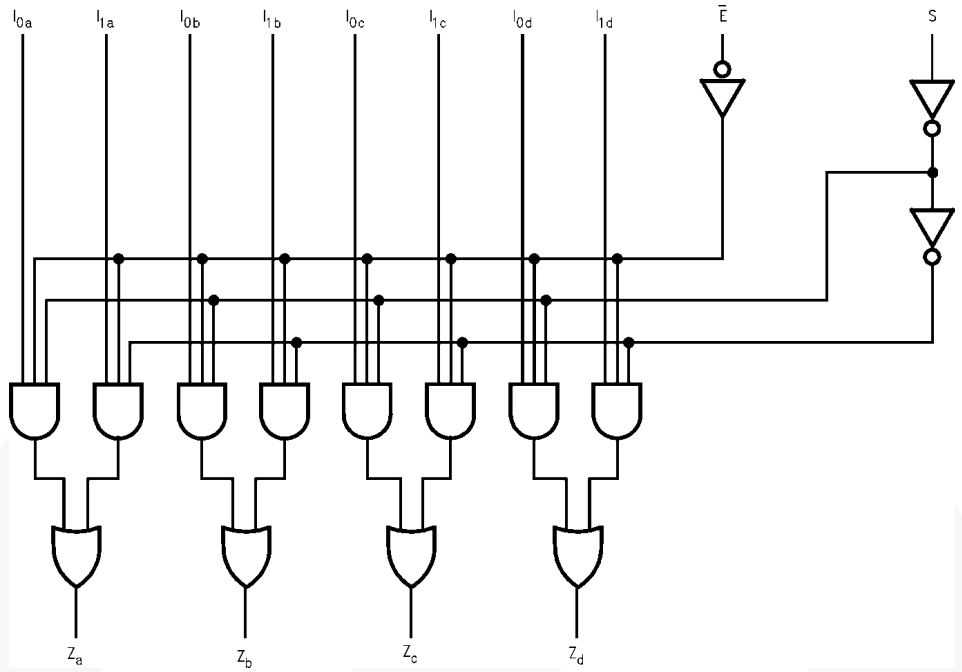
A common use of the LCX157 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The LCX157 can generate any four of the sixteen different functions of two variables with one variable common. This is useful for implementing gating functions.

Truth Table

Inputs				Outputs
$\overline{E}$	S	I_0	I_1	Z
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram(1)



Note:

1. Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(2)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Value	Conditions	Unit
V_{CC}	Supply Voltage	-0.5 to +7.0		V
V_I	DC Input Voltage	-0.5 to +7.0		V
V_O	DC Output Voltage	-0.5 to V_{CC}+0.5	Output in HIGH or LOW State(3)	V
I_{IK}	DC Input Diode Current	-50	V_I < GND	mA
I_{OK}	DC Output Diode Current	-50	V_O < GND	mA
		+50	V_O > V_{CC}	
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	-65 to +150		°C

Notes:

2. The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The “Recommended Operating Conditions” table will define the conditions for actual device operation.

3. I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions(4)

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage	Operating	2.0	3.6	V
V_{IN}	Input Voltage		0	5.5	V
V_{OUT}	Output Voltage	HIGH or LOW State	0	V_{CC}	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0 V - 3.6 V		±24	mA
		V_{CC} = 2.7 V - 3.0 V		±12	
		V_{CC} = 2.3 V - 2.7 V		±8	
T_A	Free-Air Operating Temperature		-40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8 V - 2.0 V, V_{CC} = 3.0 V		0	10	ns/V

Note:

4. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = -40 to +85°C		Unit
				Min.	Max.	
V_{IH}	HIGH Level Input Voltage		2.3 - 2.7	1.7		V
			2.7 - 3.6	2.0		
V_{IL}	LOW Level Input Voltage		2.3 - 2.7		0.7	V
			2.7 - 3.6		0.8	
V_{OH}	HIGH Level Output Voltage	I_{OH} = -100 µA	2.3 - 3.6	V_{CC} - 0.2		V
		I_{OH} = -8 mA	2.3	1.8		
		I_{OH} = -12 mA	2.7	2.2		
		I_{OH} = -18 mA	3.0	2.4		
		I_{OH} = -24 mA	3.0	2.2		
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 µA	2.3 - 3.6		0.2	V
		I_{OL} = 8 mA	2.3		0.6	
		I_{OL} = 12 mA	2.7		0.4	
		I_{OL} = 16 mA	3.0		0.4	
		I_{OL} = 24 mA	3.0		0.55	
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5 V	2.3 - 3.6		±5.0	µA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5 V	0		10	µA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.3 - 3.6		10	µA
		3.6 V ≤ V_I ≤ 5.5 V	2.3 - 3.6		±10	
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} - 0.6 V	2.3 - 3.6		500	µA

AC Electrical Characteristics

Symbol	Parameter	T_A = -40 to +85°C, R_L = 500 Ω						Unit
		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 2.5 V ± 0.2 V		
		C_L = 50 pF		C_L = 50 pF		C_L = 30 pF		
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PHL}	Propagation Delay S -> Z_n	1.5	7.0	1.5	8.0	1.5	8.4	ns
t_{PLH}		1.5	7.0	1.5	8.0	1.5	8.4	
t_{PHL}	Propagation Delay $\overline{E}$ -> Z_n	1.5	7.0	1.5	8.0	1.5	8.4	ns
t_{PLH}		1.5	7.0	1.5	8.0	1.5	8.4	
t_{PHL}	Propagation Delay I_n -> Z_n	1.5	5.8	1.5	6.3	1.5	7.0	ns
t_{PLH}		1.5	5.8	1.5	6.3	1.5	7.0	
t_{OSHL}	Output to Output Skew(5)		1.0					ns
t_{OSLH}			1.0					

Note:

5. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}). Parameter guaranteed by design.

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = 25°C	Unit
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	C_L = 50 pF, V_{IH} = 3.3 V, V_{IL} = 0 V	3.3	0.8	V
		C_L = 30 pF, V_{IH} = 2.5 V, V_{IL} = 0 V	2.5	0.6	
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	C_L = 50 pF, V_{IH} = 3.3 V, V_{IL} = 0 V	3.3	-0.8	V
		C_L = 30 pF, V_{IH} = 2.5 V, V_{IL} = 0 V	2.5	-0.6	

Capacitance

Symbol	Parameter	Conditions	Typical	Unit
C_{IN}	Input Capacitance	V_{CC} = Open, V_I = 0 V or V_{CC}	7	pF
C_{OUT}	Output Capacitance	V_{CC} = 3.3 V, V_I = 0 V or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	V_{CC} = 3.3 V, V_I = 0 V or V_{CC}, f = 10 MHz	25	pF

AC Loading and Waveforms Generic for LCX Family

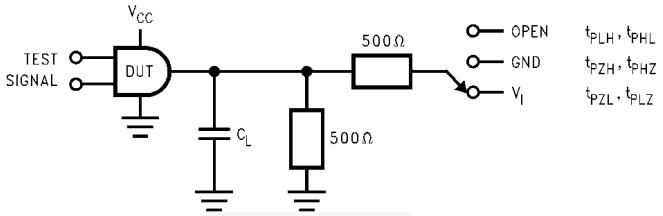
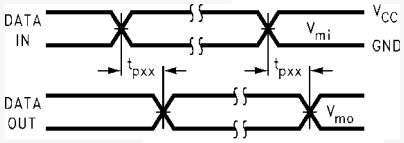
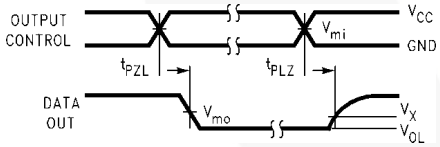


Figure 1. AC Test Circuit (C_L includes probe and jig capacitance)

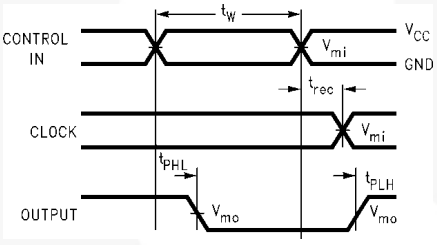
Test	Switch
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at V_{CC} = 3.3 ± 0.3V V_{CC} x 2 at V_{CC} = 2.5 ± 0.2V
t_{PZH}, t_{PHZ}	GND



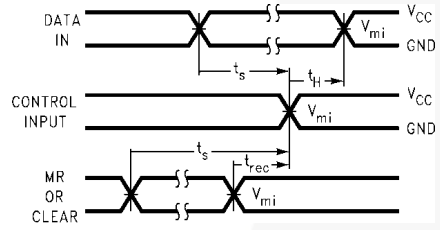
Waveform for Inverting and Non-Inverting Functions



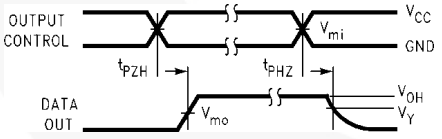
3-STATE Output Low Enable and Disable Times for Logic



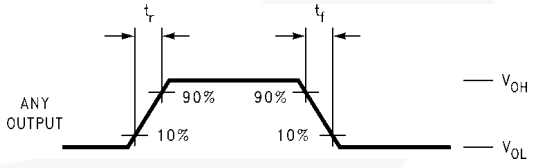
Propagation Delay. Pulse Width and t_{rec} Waveforms



Setup Time, Hold Time and Recovery Time for Logic



3-STATE Output High Enable and Disable Times for Logic



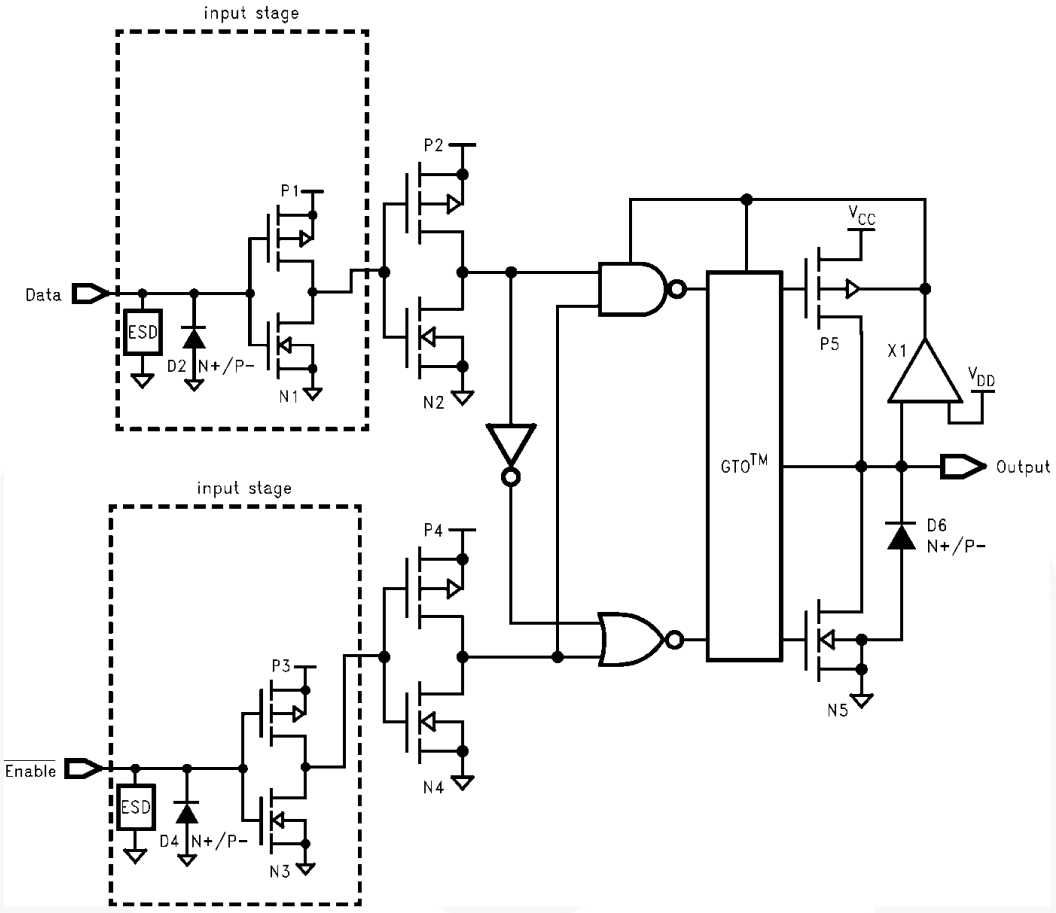
t_{rise} and t_{fall}

Figure 2. Waveforms

(Input Characteristics; f = 1 MHz, t_r = t_f = 3 ns)

Symbol	V_{CC}		
	3.3V ± 0.3V	**2.7V**	**2.5V ± 0.2V**
V_{mi}	1.5V	1.5V	V_{CC}/2
V_{mo}	1.5V	1.5V	V_{CC}/2
V_x	V_{OL} + 0.3V	V_{OL} + 0.3V	V_{OL} + 0.15V
V_y	V_{OH} − 0.3V	V_{OH} − 0.3V	V_{OH} − 0.15V

Schematic Diagram Generic for LCX Family



Physical Dimensions

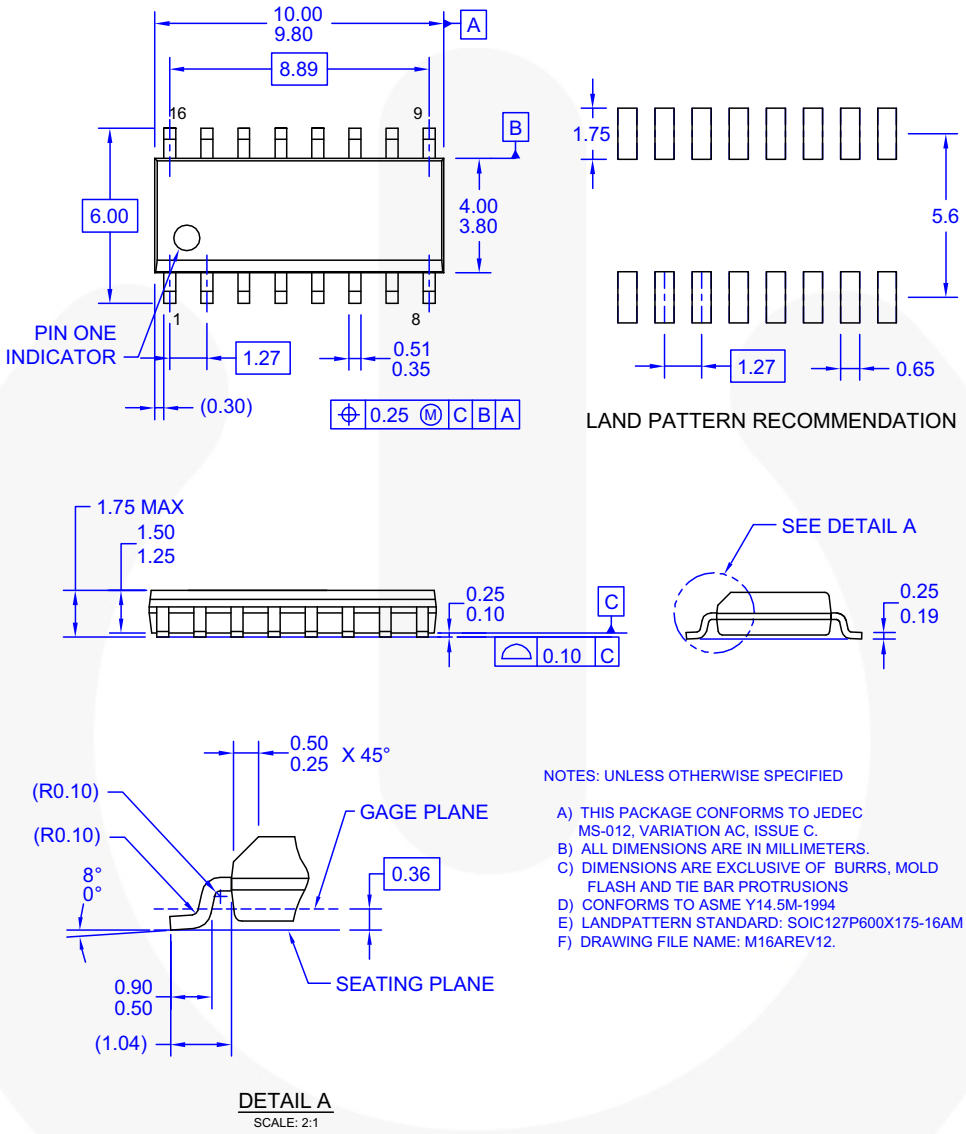


Figure 3. 16-LEAD, SOIC, JEDEC MS-012, 0.150 INCH, NARROW BODY

Physical Dimensions (Continued)

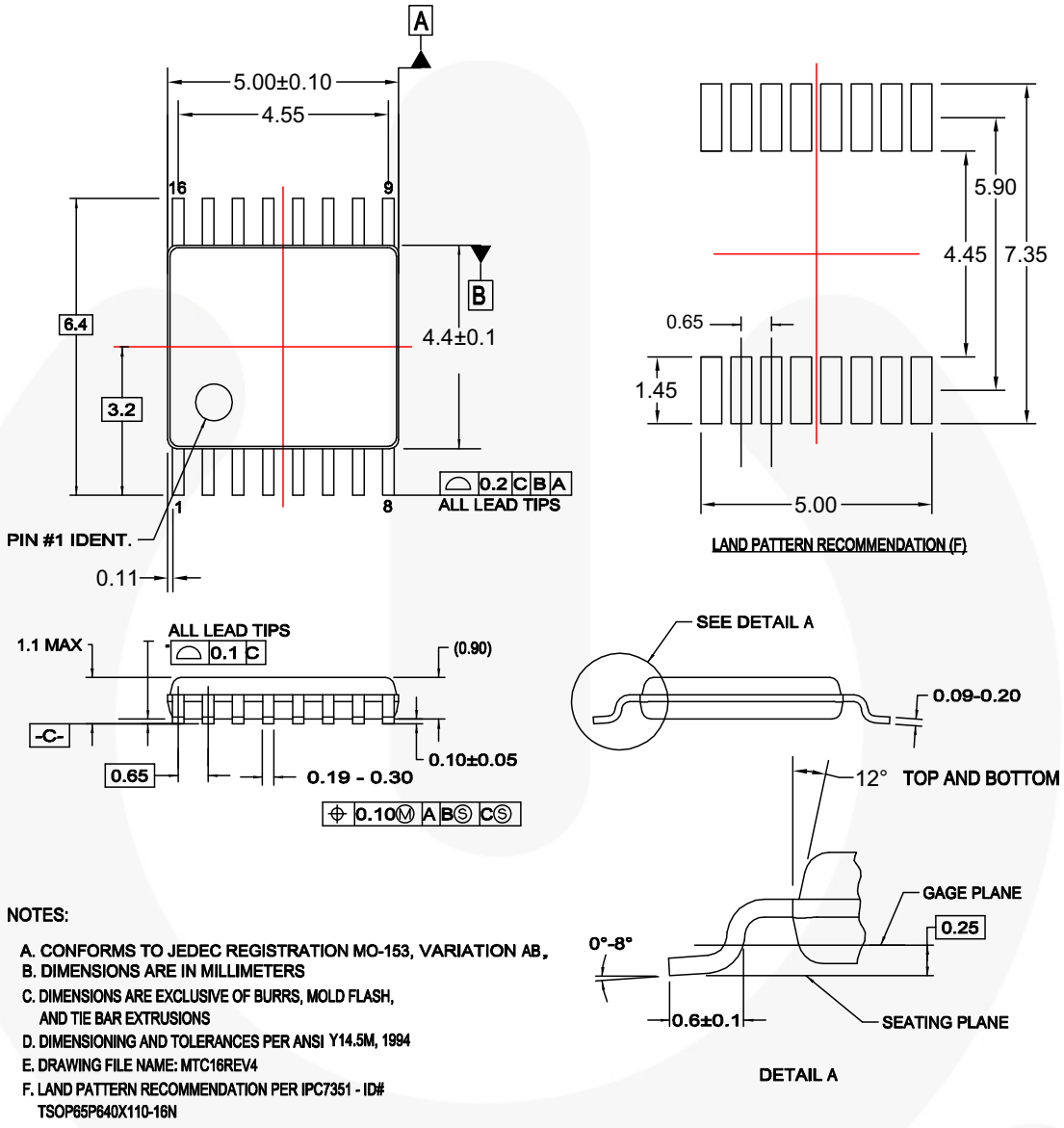


Figure 4. 16-LEAD, TSSOP, JEDEC MO-153, 4.4 MM WIDE

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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