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# FDP18N50 / FDPF18N50 / FDPF18N50T

## N-Channel UniFET™ MOSFET

500 V, 18 A, 265 mΩ

### Features

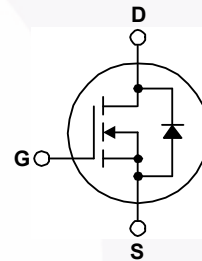
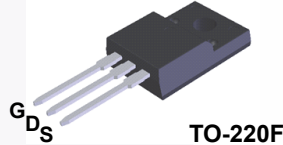
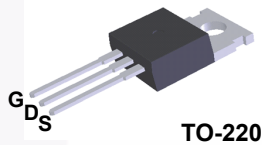
- $R_{DS(on)} = 220 \text{ m}\Omega$  (Typ.) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 9 \text{ A}$
- Low Gate Charge (Typ. 45 nC)
- Low  $C_{rss}$  (Typ. 25 pF)
- 100% Avalanche Tested

### Applications

- LCD/LED/PDP TV
- Lighting
- Uninterruptible Power Supply

### Description

UniFET™ MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.



### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FDP18N50	FDPF18N50 / FDPF18N50T	Unit
$V_{DSS}$	Drain-Source Voltage	500		V
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ\text{C}$ )	18	18 *
		- Continuous ( $T_C = 100^\circ\text{C}$ )	10.8	10.8 *
$I_{DM}$	Drain Current	- Pulsed (Note 1)	72	72 *
$V_{GSS}$	Gate-Source voltage	$\pm 30$		V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	945		mJ
$I_{AR}$	Avalanche Current (Note 1)	18		A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	23.5		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5		V/ns
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	235	38.5
		- Derate Above $25^\circ\text{C}$	1.88	0.3
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150		$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300		$^\circ\text{C}$

\* Drain current limited by maximum junction temperature

### Thermal Characteristics

Symbol	Parameter	FDP18N50	FDPF18N50 / FDPF18N50T	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.53	3.3	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	62.5	$^\circ\text{C}/\text{W}$

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDP18N50	FDP18N50	TO-220	Tube	N/A	N/A	50 units
FDPF18N50	FDPF18N50	TO-220F	Tube	N/A	N/A	50 units
FDPF18N50T	FDPF18N50T	TO-220F	Tube	N/A	N/A	50 units

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

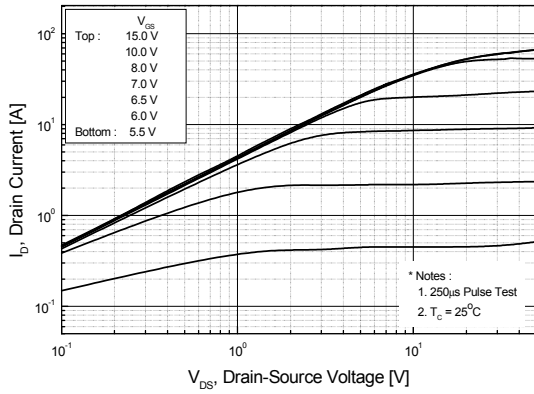
Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	500	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	0.5	--	$\text{V}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$ $V_{DS} = 400\text{ V}, T_C = 125^\circ\text{C}$	--	--	1 10	$\mu\text{A}$ $\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA
<b>On Characteristics</b>						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	3.0	--	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 9\text{ A}$	--	0.220	0.265	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 9\text{ A}$	--	25	--	S
<b>Dynamic Characteristics</b>						
$C_{ISS}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$	--	2200	2860	pF
$C_{OSS}$	Output Capacitance		--	330	430	pF
$C_{RSS}$	Reverse Transfer Capacitance		--	25	40	pF
<b>Switching Characteristics</b>						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 250\text{ V}, I_D = 18\text{ A},$ $V_{GS} = 10\text{ V}, R_G = 25\ \Omega$	--	55	120	ns
$t_r$	Turn-On Rise Time		--	165	340	ns
$t_{d(off)}$	Turn-Off Delay Time		--	95	200	ns
$t_f$	Turn-Off Fall Time		(Note 4)	--	90	190
$Q_g$	Total Gate Charge	$V_{DS} = 400\text{ V}, I_D = 18\text{ A},$ $V_{GS} = 10\text{ V}$	--	45	60	nC
$Q_{gs}$	Gate-Source Charge		--	12.5	--	nC
$Q_{gd}$	Gate-Drain Charge		(Note 4)	--	19	--
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
$I_S$	Maximum Continuous Drain-Source Diode Forward Current		--	--	18	A
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current		--	--	72	A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 18\text{ A}$	--	--	1.4	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 18\text{ A},$ $di_f/dt = 100\text{ A}/\mu\text{s}$	--	500	--	ns
$Q_{rr}$	Reverse Recovery Charge		--	5.4	--	$\mu\text{C}$

### Notes:

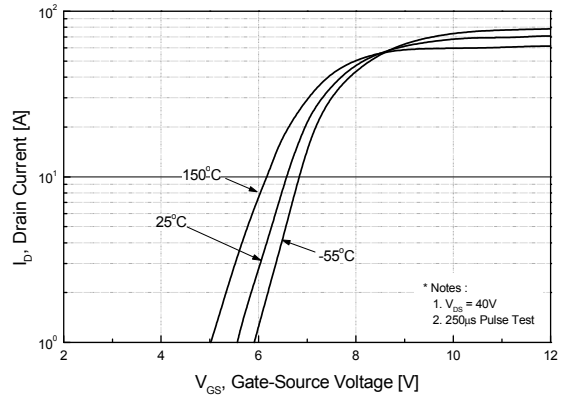
1. Repetitive rating: pulse-width limited by maximum junction temperature.
2.  $L = 5.2\text{ mH}, I_{AS} = 18\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\ \Omega$ , starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq 18\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , starting  $T_J = 25^\circ\text{C}$ .
4. Essentially independent of operating temperature typical characteristics.

## Typical Performance Characteristics

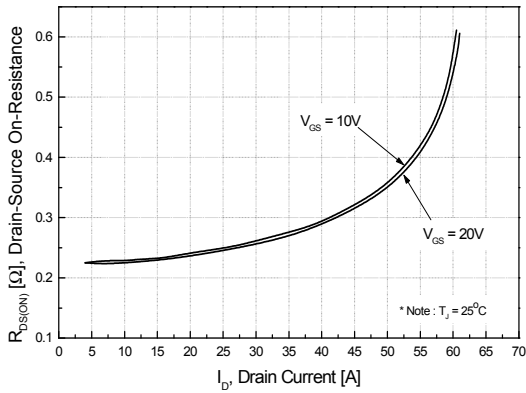
**Figure 1. On-Region Characteristics**



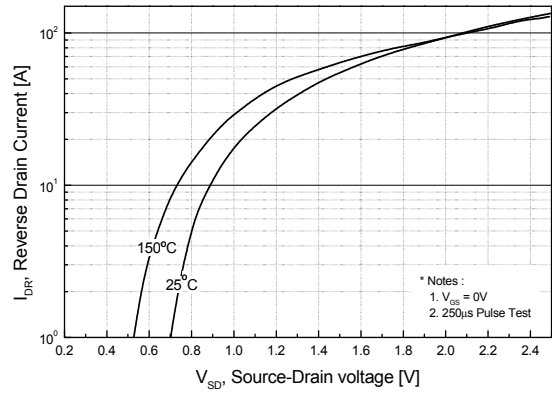
**Figure 2. Transfer Characteristics**



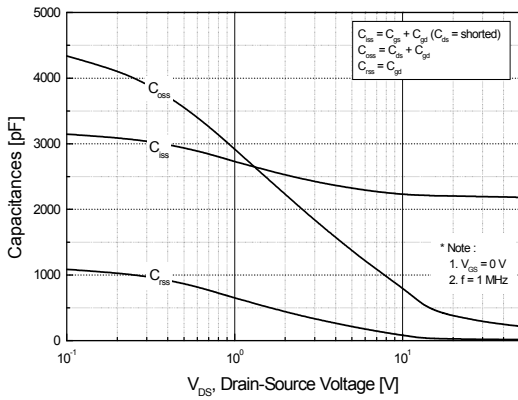
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



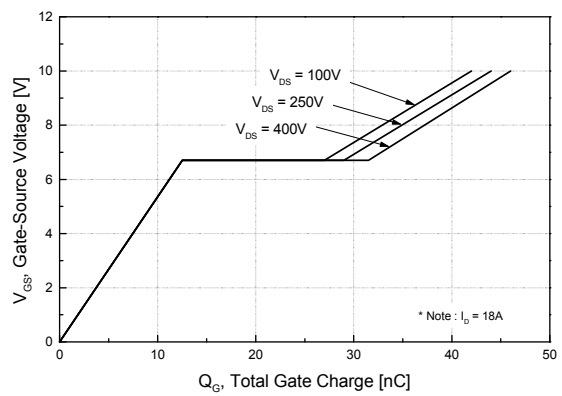
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**

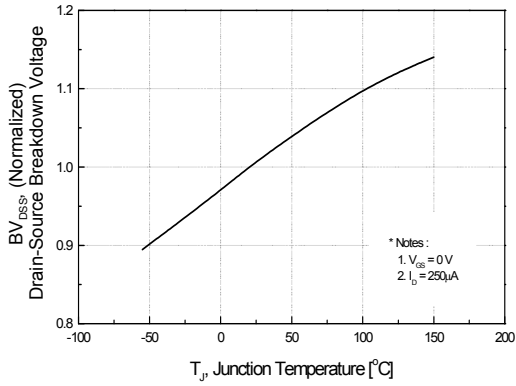


**Figure 6. Gate Charge Characteristics**

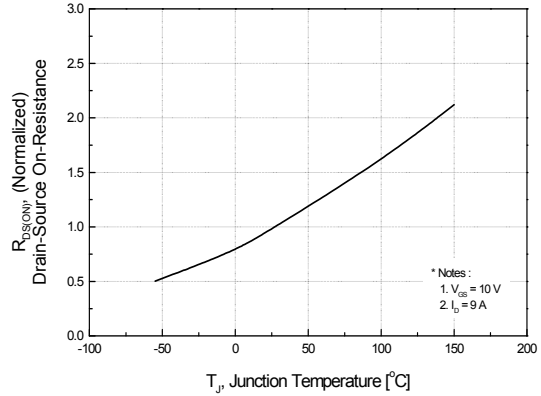


**Typical Performance Characteristics** (Continued)

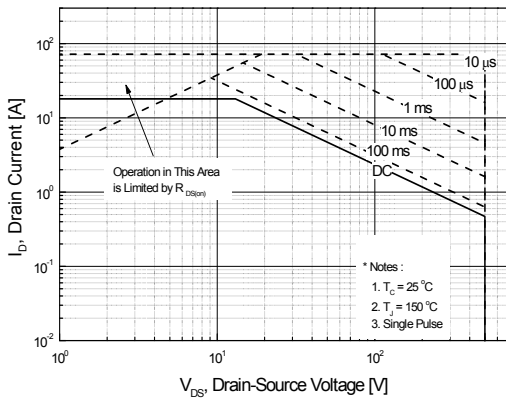
**Figure 7. Breakdown Voltage Variation vs. Temperature**



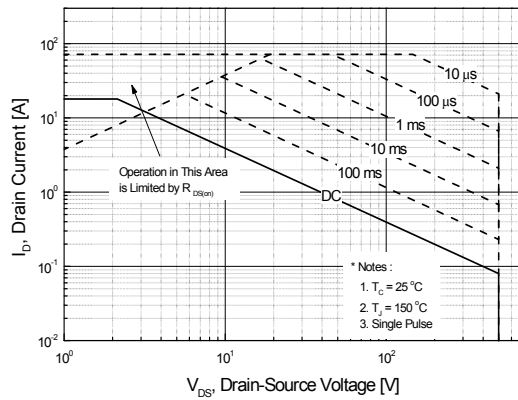
**Figure 8. On-Resistance Variation vs. Temperature**



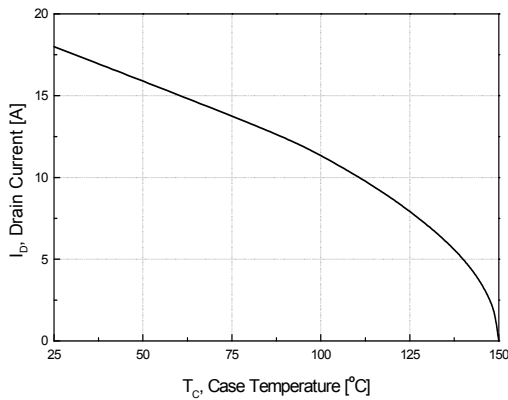
**Figure 9-1. Maximum Safe Operating Area - FDP18N50**



**Figure 9-2. Maximum Safe Operating Area - FDPF18N50 / FDPF18N50T**

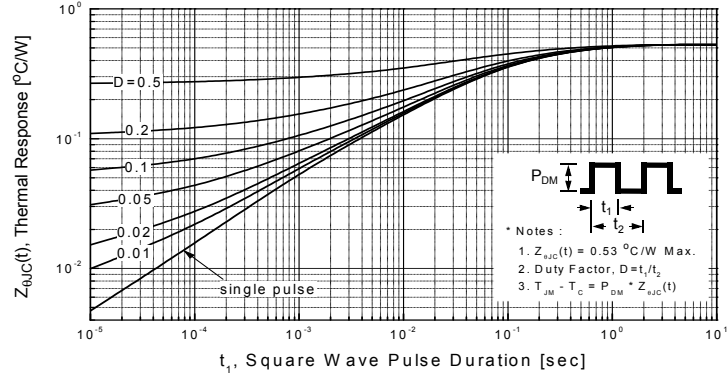


**Figure 10. Maximum Drain Current vs. Case Temperature**



**Typical Performance Characteristics** (Continued)

**Figure 11-1. Transient Thermal Response Curve - FDP18N50**



**Figure 11-2. Transient Thermal Response Curve - FDPF18N50 / FDPF18N50T**

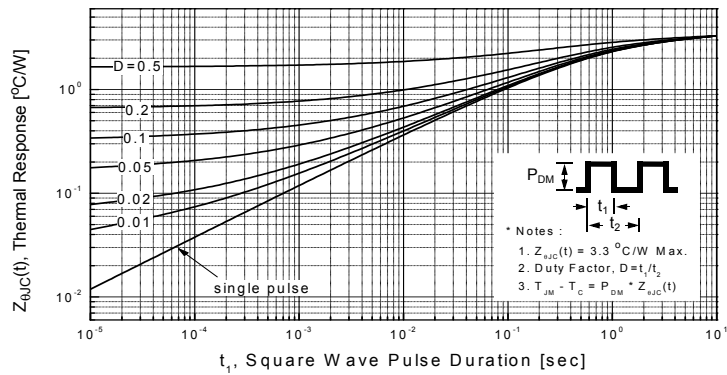




Figure 12. Gate Charge Test Circuit & Waveform



Figure 13. Resistive Switching Test Circuit & Waveforms



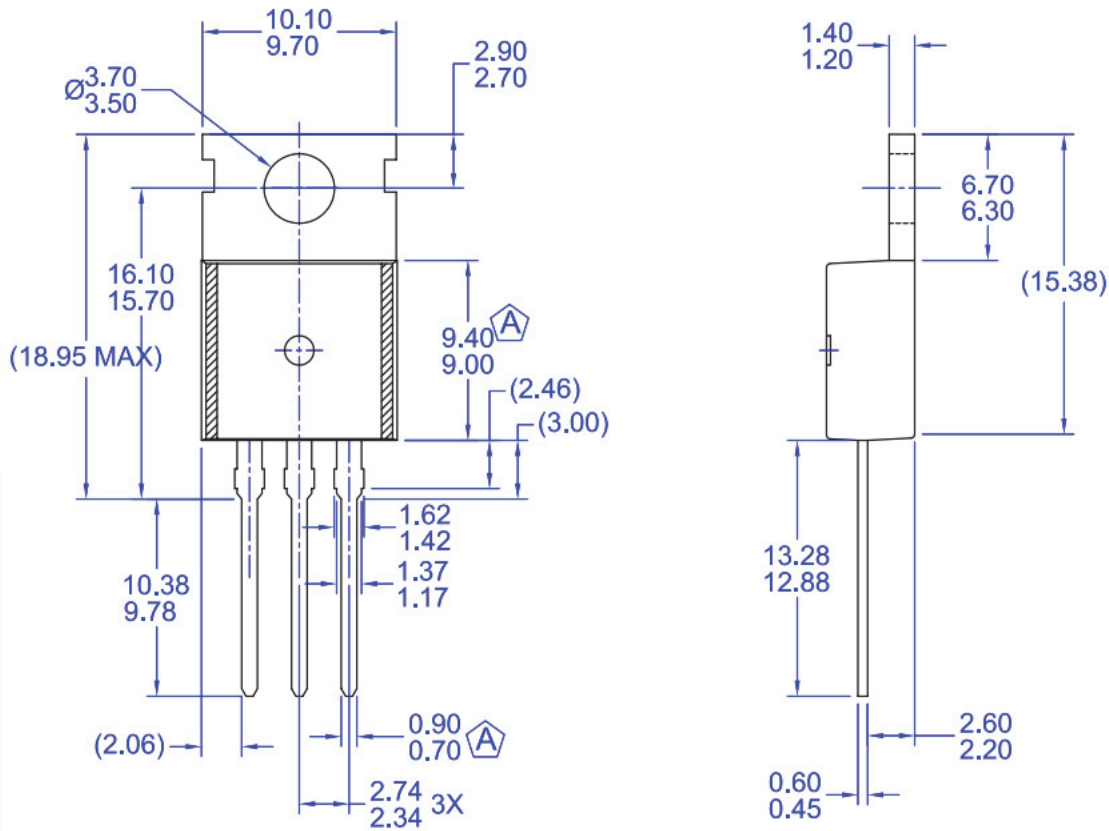
Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms



## Mechanical Dimensions



### NOTES:

- A) CONFORMS TO JEDEC TO-220 VARIATION AB EXCEPT WHERE NOTED
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D) DRAWING FILE/REVISION: MKT-TO220Y03REV1

**Figure 16. TO220, Molded, 3-Lead, Jedec Variation AB**

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## Mechanical Dimensions



### NOTES:

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- B. DOES NOT COMPLY EIAJ STD. VALUE.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- E. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
- F. OPTION 1 - WITH SUPPORT PIN HOLE.  
OPTION 2 - NO SUPPORT PIN HOLE.
- G. DRAWING FILE NAME: TO220M03REV3

**Figure 17. TO220, Molded, 3-Lead, Full Pack, EIAJ SC91, Straight Lead**

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