

## FEATURES

- 1.5  $\Omega$  on resistance
- 0.3  $\Omega$  on-resistance flatness
- 0.1  $\Omega$  on-resistance match between channels
- Up to 400 mA continuous current
- Fully specified at +12 V,  $\pm 15$  V, and  $\pm 5$  V
- No  $V_L$  supply required
- 3 V logic-compatible inputs
- Rail-to-rail operation
- 14-lead TSSOP and 4 mm  $\times$  4 mm, 16-lead LFCSP

## APPLICATIONS

- Automatic test equipment
- Data acquisition systems
- Battery-powered systems
- Sample-and-hold systems
- Audio signal routing
- Communication systems
- Relay replacement

## GENERAL DESCRIPTION

The ADG1404 is a complementary metal-oxide semiconductor (CMOS) analog multiplexer, comprising four single channels designed on an *i*CMOS<sup>®</sup> process. *i*CMOS (industrial CMOS) is a modular manufacturing process that combines high voltage CMOS and bipolar technologies. It enables the development of a wide range of high performance analog ICs capable of 33 V operation in a footprint that no previous generation of high voltage devices achieve. Unlike analog ICs using conventional CMOS processes, *i*CMOS components can tolerate high supply voltages while providing increased performance, dramatically lower power consumption, and reduced package size.

The on-resistance profile is very flat over the full analog input range, ensuring excellent linearity and low distortion when switching audio signals.

*i*CMOS construction ensures ultralow power dissipation, making the device ideally suited for portable and battery-powered instruments.

## FUNCTIONAL BLOCK DIAGRAM

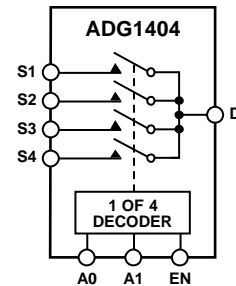


Figure 1.

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The ADG1404 switches one of four inputs to a common output, D, as determined by the 3-bit binary address lines, A0, A1, and EN. Logic 0 on the EN pin disables the device. Each switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked. All switches exhibit break-before-make switching action. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

## PRODUCT HIGHLIGHTS

1. 2.6  $\Omega$  maximum on resistance over temperature.
2. Minimum distortion.
3. Ultralow power dissipation: <0.03  $\mu$ W.
4. 14-lead TSSOP and 16-lead, 4 mm  $\times$  4 mm LFCSP package.

### Rev. B

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# ADG1404\* Product Page Quick Links

Last Content Update: 10/05/2016

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### **Application Notes**

- AN-1024: How to Calculate the Settling Time and Sampling Rate of a Multiplexer

### **Data Sheet**

- ADG1404: 1.5  $\Omega$  On Resistance,  $\pm 15$  V/12 V/ $\pm 5$  V, 4:1, iCMOS Multiplexer Data Sheet

## [Reference Materials](#)

### **Informational**

- iCMOS Technology Enabling the +/-10V World

### **Product Selection Guide**

- Switches and Multiplexers Product Selection Guide

## [Design Resources](#)

- ADG1404 Material Declaration
- PCN-PDN Information
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## TABLE OF CONTENTS

Features .....	1	Continuous Current, S or D.....	6
Applications.....	1	Absolute Maximum Ratings .....	7
Functional Block Diagram .....	1	ESD Caution.....	7
General Description .....	1	Pin Configurations and Function Descriptions .....	8
Product Highlights .....	1	Truth Table .....	8
Revision History .....	2	Typical Performance Characteristics .....	9
Specifications.....	3	Terminology .....	12
15 V Dual Supply.....	3	Test Circuits.....	13
12 V Single Supply.....	4	Outline Dimensions .....	16
5 V Dual Supply.....	5	Ordering Guide .....	16

## REVISION HISTORY

### 9/2016—Rev. A to Rev. B

Changes to Figure 3.....	8
Updated Outline Dimensions.....	16
Changes to Ordering Guide .....	16

### 3/2009—Rev. 0 to Rev. A

Changes to Power Requirements, $I_{DD}$ , Digital Inputs = 5 V Parameter, Table 1.....	3
Changes to Power Requirements, $I_{DD}$ , Digital Inputs = 5 V Parameter, Table 2.....	4
Updated Outline Dimensions .....	16

### 7/2008—Revision 0: Initial Version

# SPECIFICATIONS

## 15 V DUAL SUPPLY

$V_{DD} = 15\text{ V} \pm 10\%$ ,  $V_{SS} = -15\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ , unless otherwise noted.

Table 1.

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			$V_{DD}$ to $V_{SS}$	V	
On Resistance ( $R_{ON}$ )	1.5			$\Omega$ typ	$V_S = \pm 10\text{ V}$ , $I_S = -10\text{ mA}$ ; see Figure 22
	1.8	2.3	2.6	$\Omega$ max	$V_{DD} = +13.5\text{ V}$ , $V_{SS} = -13.5\text{ V}$
On-Resistance Match Between Channels ( $\Delta R_{ON}$ )	0.1			$\Omega$ typ	$V_S = \pm 10\text{ V}$ , $I_S = -10\text{ mA}$
	0.18	0.19	0.21	$\Omega$ max	
On-Resistance Flatness ( $R_{FLAT(ON)}$ )	0.3			$\Omega$ typ	$V_S = \pm 10\text{ V}$ , $I_S = -10\text{ mA}$
	0.36	0.4	0.45	$\Omega$ max	
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage, $I_S$ (Off)	$\pm 0.03$			nA typ	$V_{DD} = +16.5\text{ V}$ , $V_{SS} = -16.5\text{ V}$
	$\pm 0.55$	$\pm 2$	$\pm 12.5$	nA max	$V_S = \pm 10\text{ V}$ , $V_S = \mp 10\text{ V}$ ; see Figure 23
Drain Off Leakage, $I_D$ (Off)	$\pm 0.04$			nA typ	
	$\pm 0.55$	$\pm 4$	$\pm 30$	nA max	$V_S = \pm 10\text{ V}$ , $V_S = \mp 10\text{ V}$ ; see Figure 23
Channel On Leakage, $I_D$ , $I_S$ (On)	$\pm 0.1$			nA typ	$V_S = V_D = \pm 10\text{ V}$ ; see Figure 24
	$\pm 2$	$\pm 4$	$\pm 30$	nA max	
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$			2.0	V min	
Input Low Voltage, $V_{INL}$			0.8	V max	
Input Current, $I_{INL}$ or $I_{INH}$	0.005			$\mu\text{A}$ typ	$V_{IN} = V_{GND}$ or $V_{DD}$
			$\pm 0.1$	$\mu\text{A}$ max	
Digital Input Capacitance, $C_{IN}$	3.5			pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>					
Transition Time, $t_{TRANSITION}$	150			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	180	220	250	ns max	$V_S = +10\text{ V}$ ; see Figure 29
$t_{ON}$ (EN)	100			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	120	145	165	ns max	$V_S = +10\text{ V}$ ; see Figure 31
$t_{OFF}$ (EN)	110			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	135	165	185	ns max	$V_S = +10\text{ V}$ ; see Figure 31
Break-Before-Make Time Delay, $t_{BBM}$	35			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
			10	ns min	$V_{S1} = V_{S2} = 10\text{ V}$ ; see Figure 30
Charge Injection	-20			pC typ	$V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; see Figure 32
Off Isolation	70			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 100\text{ kHz}$ ; see Figure 25
Channel-to-Channel Crosstalk	82			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 100\text{ kHz}$ ; see Figure 27
Total Harmonic Distortion + Noise	0.011			% typ	$R_L = 110\ \Omega$ , 10 V p-p, $f = 20\text{ Hz}$ to 20 kHz; see Figure 28
-3 dB Bandwidth	55			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; see Figure 26
Insertion Loss	-0.17			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 26
$C_S$ (Off)	23			pF typ	$f = 1\text{ MHz}$ , $V_S = 0\text{ V}$
$C_D$ (Off)	90			pF typ	$f = 1\text{ MHz}$ , $V_S = 0\text{ V}$
$C_D$ , $C_S$ (On)	170			pF typ	$f = 1\text{ MHz}$ , $V_S = 0\text{ V}$
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	0.001			$\mu\text{A}$ typ	$V_{DD} = +16.5\text{ V}$ , $V_{SS} = -16.5\text{ V}$
			1	$\mu\text{A}$ max	Digital inputs = 0 V or $V_{DD}$
$I_{DD}$	170			$\mu\text{A}$ typ	Digital inputs = 5 V
			285	$\mu\text{A}$ max	
$I_{SS}$	0.001			$\mu\text{A}$ typ	Digital inputs = 0 V or $V_{DD}$
			1	$\mu\text{A}$ max	
$V_{DD}/V_{SS}$			$\pm 4.5/\pm 16.5$	V min/max	$GND = 0\text{ V}$

<sup>1</sup> Guaranteed by design, not subject to production test.

**12 V SINGLE SUPPLY**

$V_{DD} = 12\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $GND = 0\text{ V}$ , unless otherwise noted.

**Table 2.**

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			0 V to $V_{DD}$	V	
On Resistance ( $R_{ON}$ )	2.8 3.5	4.3	4.8	$\Omega$ typ $\Omega$ max	$V_S = 0\text{ V to }10\text{ V}$ , $I_S = -10\text{ mA}$ ; see Figure 22 $V_{DD} = 10.8\text{ V}$ , $V_{SS} = 0\text{ V}$
On-Resistance Match Between Channels ( $\Delta R_{ON}$ )	0.13			$\Omega$ typ	$V_S = 0\text{ V to }10\text{ V}$ , $I_S = -10\text{ mA}$
On-Resistance Flatness ( $R_{FLAT(ON)}$ )	0.21 0.6	0.23	0.25	$\Omega$ max $\Omega$ typ	$V_S = 0\text{ V to }10\text{ V}$ , $I_S = -10\text{ mA}$
	1.1	1.2	1.3	$\Omega$ max	
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage, $I_S$ (Off)	$\pm 0.02$ $\pm 0.55$	$\pm 2$	$\pm 12.5$	nA typ nA max	$V_{DD} = 13.2\text{ V}$ , $V_{SS} = 0\text{ V}$ $V_S = 1\text{ V}/10\text{ V}$ , $V_D = 10\text{ V}/1\text{ V}$ ; see Figure 23
Drain Off Leakage, $I_D$ (Off)	$\pm 0.03$ $\pm 0.55$	$\pm 4$	$\pm 30$	nA typ nA max	$V_S = 1\text{ V}/10\text{ V}$ , $V_D = 10\text{ V}/1\text{ V}$ ; see Figure 23
Channel On Leakage, $I_D$ , $I_S$ (On)	$\pm 0.1$ $\pm 1.5$	$\pm 4$	$\pm 30$	nA typ nA max	$V_S = V_D = 1\text{ V or }10\text{ V}$ ; see Figure 24
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$			2.0	V min	
Input Low Voltage, $V_{INL}$			0.8	V max	
Input Current, $I_{INL}$ or $I_{INH}$	0.001		$\pm 0.1$	$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{IN} = V_{GND}$ or $V_{DD}$
Digital Input Capacitance, $C_{IN}$	3.5			pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>					
Transition Time, $t_{TRANSITION}$	230 300	375	430	ns typ ns max	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ $V_S = 8\text{ V}$ ; see Figure 29
$t_{ON}$ (EN)	180 240	295	335	ns typ ns max	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ $V_S = 8\text{ V}$ ; see Figure 31
$t_{OFF}$ (EN)	115 160	190	220	ns typ ns max	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ $V_S = 8\text{ V}$ ; see Figure 31
Break-Before-Make Time Delay, $t_{BBM}$	100		10	ns typ ns min	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ $V_{S1} = V_{S2} = 8\text{ V}$ ; see Figure 30
Charge Injection	30			pC typ	$V_S = 6\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; see Figure 32
Off Isolation	80			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 100\text{ kHz}$ ; see Figure 25
Channel-to-Channel Crosstalk	82			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 100\text{ kHz}$ ; see Figure 27
−3 dB Bandwidth	35			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; see Figure 26
Insertion Loss	−0.3			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 26
$C_S$ (Off)	39			pF typ	$f = 1\text{ MHz}$ , $V_S = 6\text{ V}$
$C_D$ (Off)	150			pF typ	$f = 1\text{ MHz}$ , $V_S = 6\text{ V}$
$C_D$ , $C_S$ (On)	217			pF typ	$f = 1\text{ MHz}$ , $V_S = 6\text{ V}$
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	0.001		1	$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{DD} = 13.2\text{ V}$ Digital inputs = 0 V or $V_{DD}$
$I_{DD}$	170		285	$\mu\text{A}$ typ $\mu\text{A}$ max	Digital inputs = 5 V
$V_{DD}$			5/16.5	V min/max	$GND = 0\text{ V}$ , $V_{SS} = 0\text{ V}$

<sup>1</sup> Guaranteed by design, not subject to production test.

**5 V DUAL SUPPLY**

$V_{DD} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = -5\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ , unless otherwise noted.

**Table 3.**

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			$V_{DD}$ to $V_{SS}$	V	
On Resistance ( $R_{ON}$ )	3.3 4	4.9	5.4	$\Omega$ typ $\Omega$ max	$V_S = \pm 4.5\text{ V}$ , $I_S = -10\text{ mA}$ ; see Figure 22 $V_{DD} = +4.5\text{ V}$ , $V_{SS} = -4.5\text{ V}$
On-Resistance Match Between Channels ( $\Delta R_{ON}$ )	0.13			$\Omega$ typ	$V_S = \pm 4.5\text{ V}$ , $I_S = -10\text{ mA}$
On-Resistance Flatness ( $R_{FLAT(ON)}$ )	0.22 0.9	0.23	0.25	$\Omega$ max $\Omega$ typ	$V_S = \pm 4.5\text{ V}$ , $I_S = -10\text{ mA}$
	1.1	1.24	1.31	$\Omega$ max	
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage, $I_S$ (Off)	$\pm 0.02$			nA typ	$V_{DD} = +5.5\text{ V}$ , $V_{SS} = -5.5\text{ V}$ $V_S = \pm 4.5\text{ V}$ , $V_D = \mp 4.5\text{ V}$ ; see Figure 23
Drain Off Leakage, $I_D$ (Off)	$\pm 0.2$ $\pm 0.02$	$\pm 1$	$\pm 12.5$	nA max nA typ	$V_S = \pm 4.5\text{ V}$ , $V_D = \mp 4.5\text{ V}$ ; see Figure 23
Channel On Leakage, $I_D$ , $I_S$ (On)	$\pm 0.25$ $\pm 0.05$ $\pm 0.25$	$\pm 1.2$	$\pm 15$	nA max nA typ nA max	$V_S = V_D = \pm 4.5\text{ V}$ ; see Figure 24
		$\pm 1.5$	$\pm 20$		
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$			2.0	V min	
Input Low Voltage, $V_{INL}$			0.8	V max	
Input Current, $I_{INL}$ or $I_{INH}$	0.001			$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{IN} = V_{GND}$ or $V_{DD}$
Digital Input Capacitance, $C_{IN}$	3.5			pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>					
Transition Time, $t_{TRANSITION}$	340 470			ns typ ns max	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ $V_S = 3\text{ V}$ ; Figure 29
$t_{ON}$ (EN)	260 355	560	615	ns typ ns max	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ $V_S = 3\text{ V}$ ; Figure 31
$t_{OFF}$ (EN)	220 315	430	480	ns typ ns max	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ $V_S = 3\text{ V}$ ; Figure 31
Break-Before-Make Time Delay, $t_{BBM}$	100	365	400	ns typ ns min	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ $V_{S1} = V_{S2} = 3\text{ V}$ ; see Figure 30
Charge Injection	30		50	pC typ	$V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; see Figure 32
Off Isolation	80			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 100\text{ kHz}$ ; see Figure 25
Channel-to-Channel Crosstalk	82			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 100\text{ kHz}$ ; see Figure 27
-3 dB Bandwidth	40			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; see Figure 26
Insertion Loss	0.27			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 26
Total Harmonic Distortion + Noise	0.03			% typ	$R_L = 110\ \Omega$ , 2.5 V p-p, $f = 20\text{ Hz}$ to 20 kHz; see Figure 28
$C_S$ (Off)	33			pF typ	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$
$C_D$ (Off)	128			pF typ	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$
$C_D$ , $C_S$ (On)	210			pF typ	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	0.001			$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{DD} = 5.5\text{ V}$ , $V_{SS} = -5.5\text{ V}$ Digital inputs = 0 V, 5 V, or $V_{DD}$
$I_{SS}$	0.001		1	$\mu\text{A}$ typ $\mu\text{A}$ max	Digital inputs = 0 V or $V_{DD}$
$V_{DD}/V_{SS}$			1 $\pm 4.5/\pm 16.5$	V min/max	$GND = 0\text{ V}$

<sup>1</sup> Guaranteed by design, not subject to production test.

**CONTINUOUS CURRENT, S OR D**

Table 4.

Parameter	25°C	85°C	125°C	Unit	Test Conditions/Comments
CONTINUOUS CURRENT, S or D <sup>1</sup>					
15 V Dual Supply					$V_{DD} = +13.5\text{ V}, V_{SS} = -13.5\text{ V}$
ADG1404 TSSOP	350	220	100	mA max	
ADG1404 LFCSP	450	300	140	mA max	
12 V Single Supply					$V_{DD} = 10.8\text{ V}, V_{SS} = 0\text{ V}$
ADG1404 TSSOP	300	220	100	mA max	
ADG1404 LFCSP	400	300	140	mA max	
5 V Dual Supply					$V_{DD} = +4.5\text{ V}, V_{SS} = -4.5\text{ V}$
ADG1404 TSSOP	300	220	100	mA max	
ADG1404 LFCSP	400	300	140	mA max	

<sup>1</sup> Guaranteed by design, not subject to production test.

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 5.

Parameter	Rating
$V_{DD}$ to $V_{SS}$	35 V
$V_{DD}$ to GND	-0.3 V to +25 V
$V_{SS}$ to GND	+0.3 V to -25 V
Analog Inputs <sup>1</sup>	$V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Digital Inputs	GND - 0.3 V to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Peak Current, S or D	600 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, S or D <sup>2</sup>	Data + 15%
Operating Temperature Range	
Automotive (Y Version)	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
14-Lead TSSOP, $\theta_{JA}$ Thermal Impedance (4-layer board)	112°C/W
16-Lead LFCSOP, $\theta_{JA}$ Thermal Impedance	30.4°C/W
Reflow Soldering Peak Temperature, Pb free	260(+0/-5)°C

<sup>1</sup> Overvoltages at IN, S, and D are clamped by internal diodes. Current must be limited to the maximum ratings given.

<sup>2</sup> See data given in Table 4.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.



PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

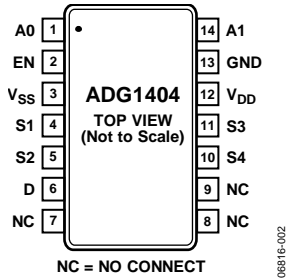
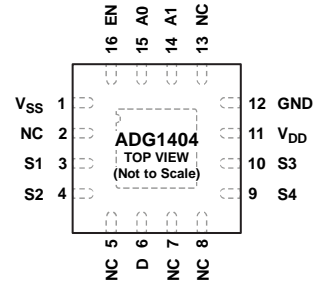


Figure 2. TSSOP Pin Configuration



NOTES  
 1. EXPOSED PAD TIED TO SUBSTRATE, V<sub>SS</sub>.  
 2. NC = NO CONNECT.

Figure 3. LFCSP Pin Configuration

Table 6. Pin Function Descriptions

Pin No.		Mnemonic	Description
TSSOP	LFCSP		
1	15	A0	Logic Control Input.
2	16	EN	Active High Digital Input. When this pin is low, the device is disabled and all switches are off. When this pin is high, the Ax logic inputs determine the on switches.
3	1	V <sub>SS</sub>	Most Negative Power Supply Potential.
4	3	S1	Source Terminal. Can be an input or an output.
5	4	S2	Source Terminal. Can be an input or an output.
6	6	D	Drain Terminal. Can be an input or an output.
7 to 9	2, 5, 7, 8, 13	NC	No Connection.
10	9	S4	Source Terminal. Can be an input or an output.
11	10	S3	Source Terminal. Can be an input or an output.
12	11	V <sub>DD</sub>	Most Positive Power Supply Potential.
13	12	GND	Ground (0 V) Reference.
14	14	A1	Logic Control Input.

TRUTH TABLE

Table 7.

EN	A1	A0	S1	S2	S3	S4
0	X	X	Off	Off	Off	Off
1	0	0	On	Off	Off	Off
1	0	1	Off	On	Off	Off
1	1	0	Off	Off	On	Off
1	1	1	Off	Off	Off	On

TYPICAL PERFORMANCE CHARACTERISTICS

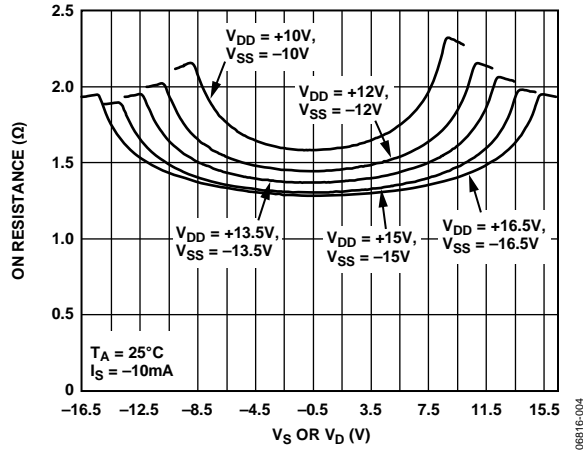


Figure 4. On Resistance as a Function of  $V_D$  ( $V_S$ ), Dual Supply

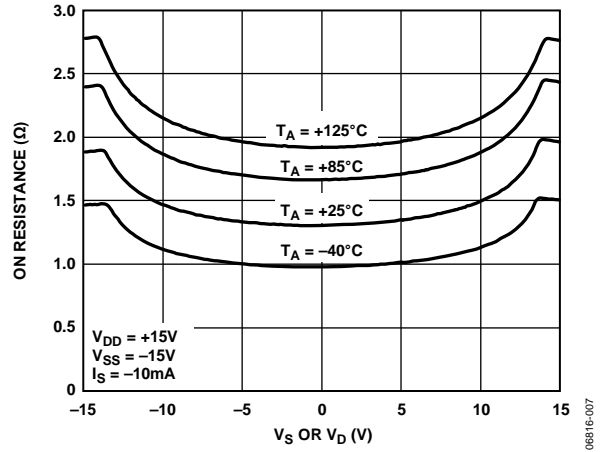


Figure 7. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures, 15 V Dual Supply

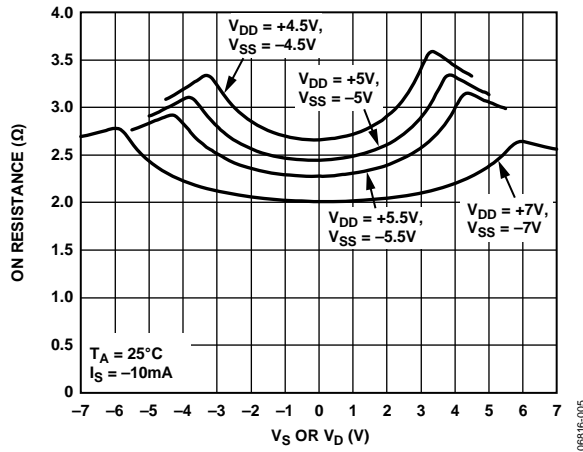


Figure 5. On Resistance as a Function of  $V_D$  ( $V_S$ ), Dual Supply

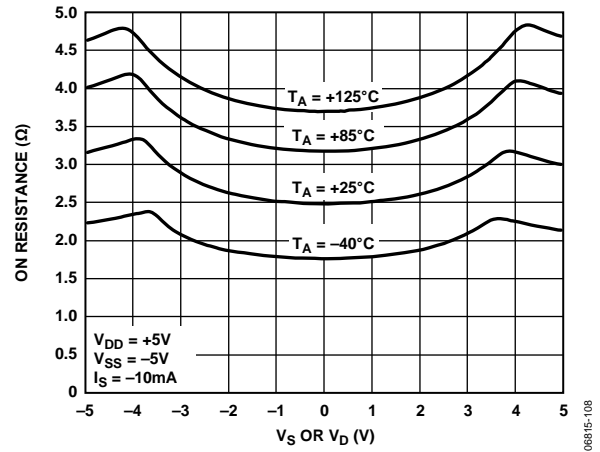


Figure 8. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures, 5 V Dual Supply

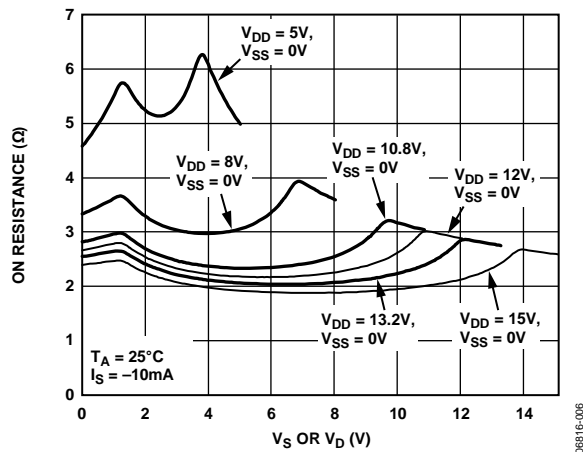


Figure 6. On Resistance as a Function of  $V_D$  ( $V_S$ ), Single Supply

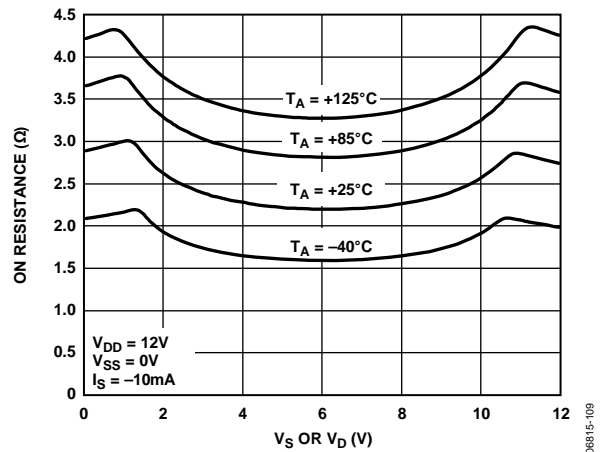


Figure 9. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures, Single Supply

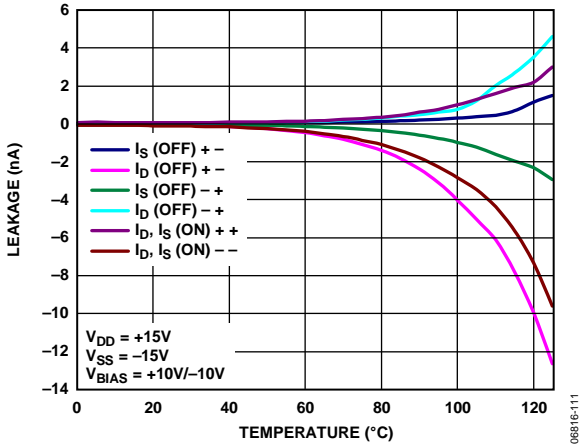


Figure 10. Leakage Currents as a Function of Temperature, 15 V Dual Supply

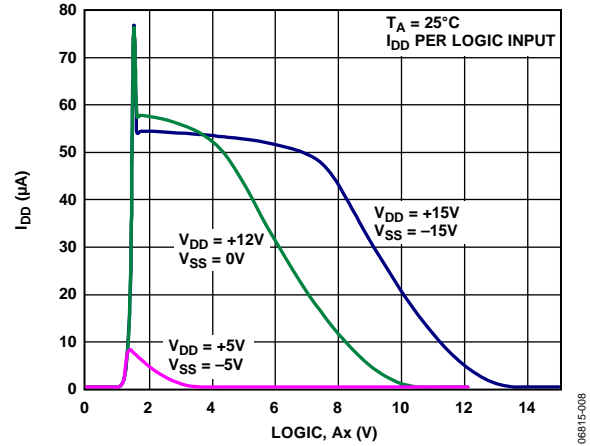


Figure 13.  $I_{DD}$  vs. Logic Level

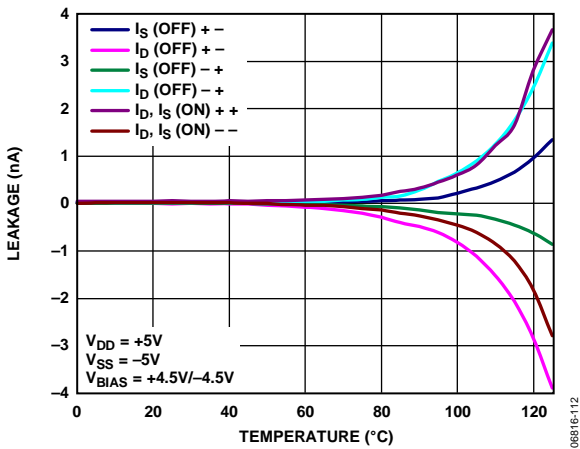


Figure 11. Leakage Currents as a Function of Temperature, 5 V Dual Supply

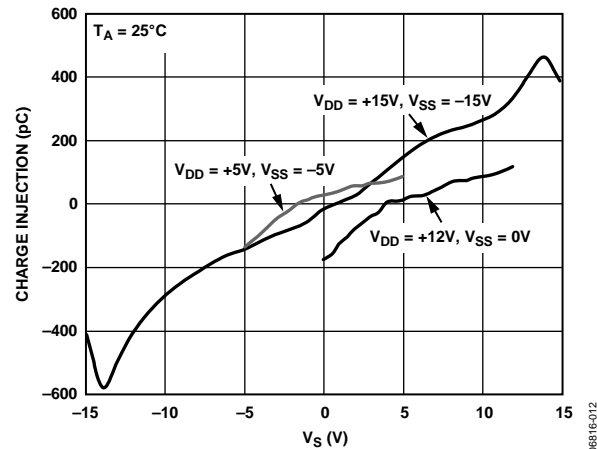


Figure 14. Charge Injection vs. Source Voltage

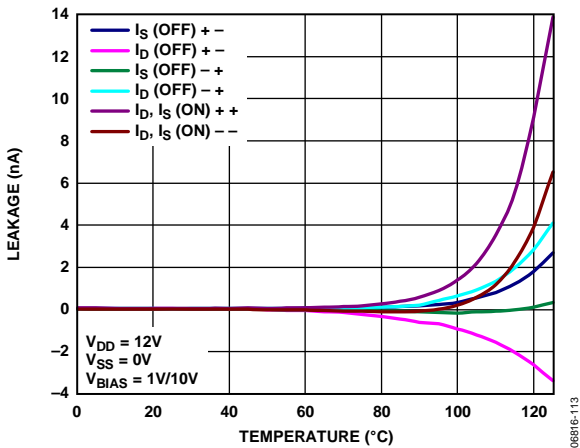


Figure 12. Leakage Currents as a Function of Temperature, 12 V Single Supply

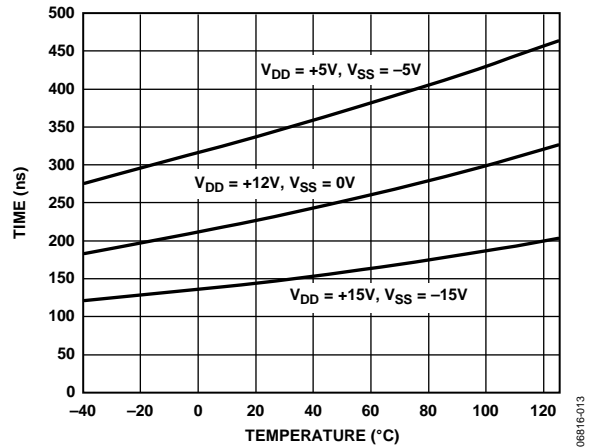


Figure 15. Transition Times vs. Temperature

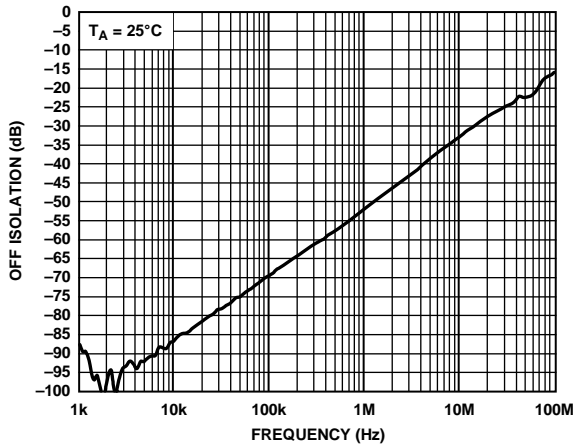


Figure 16. Off Isolation vs. Frequency

06816-014

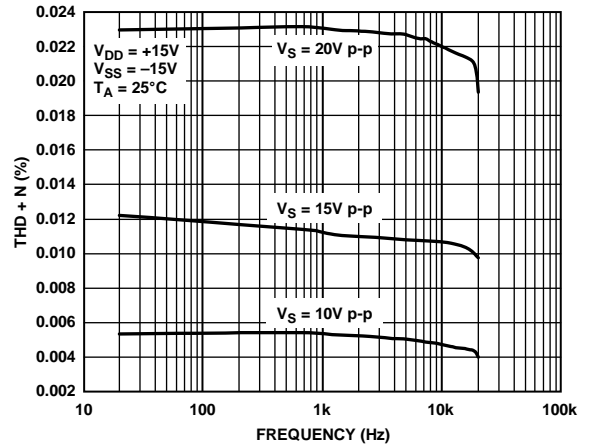


Figure 19. THD + N vs. Frequency at  $\pm 15 V$

06816-017

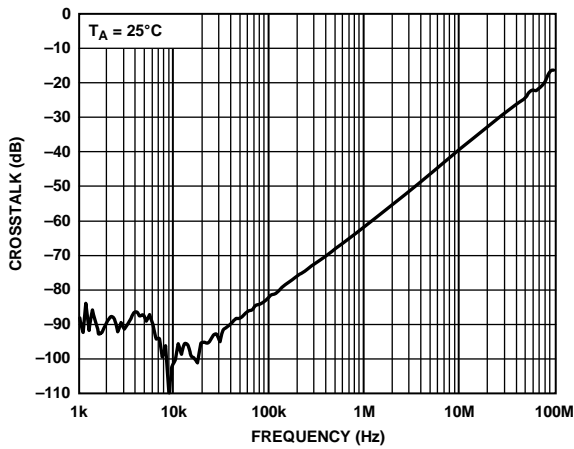


Figure 17. Crosstalk vs. Frequency

06816-015

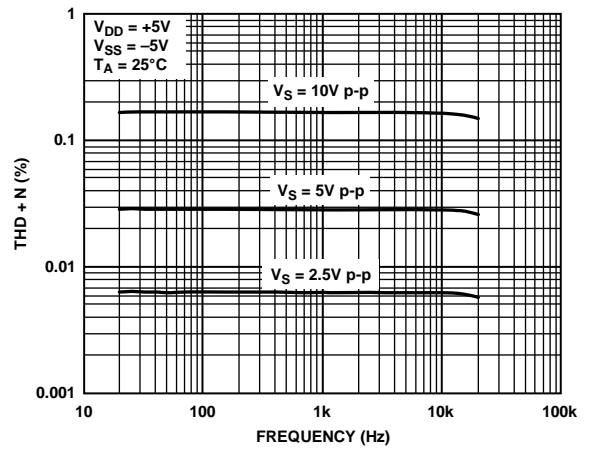


Figure 20. THD + N vs. Frequency at  $\pm 5 V$

06816-018

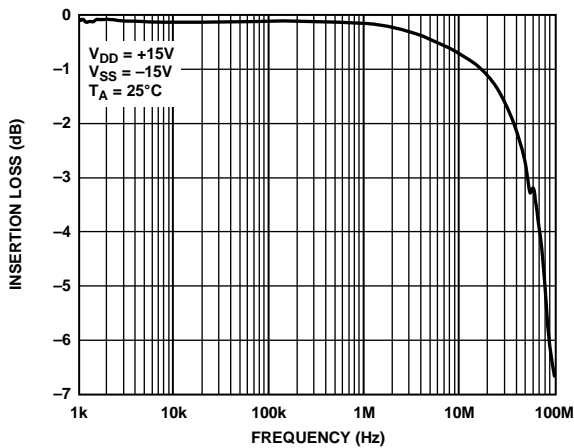


Figure 18. On Response vs. Frequency

06816-016

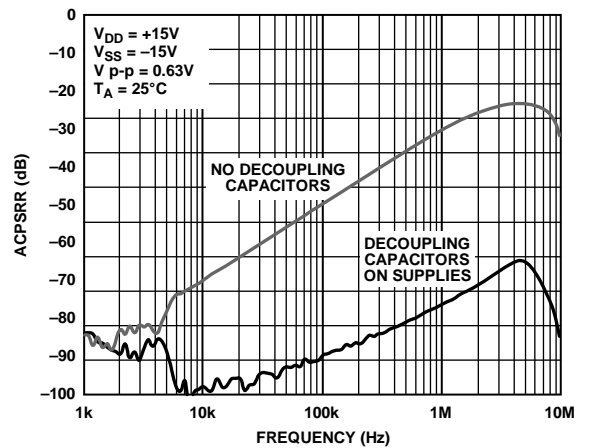


Figure 21. ACPSRR vs. Frequency

06815-017

## TERMINOLOGY

**I<sub>DD</sub>**

The positive supply current.

**I<sub>SS</sub>**

The negative supply current.

**V<sub>D</sub> (V<sub>S</sub>)**

The analog voltage on Terminal D and Terminal S.

**R<sub>ON</sub>**

The ohmic resistance between Terminal D and Terminal S.

**R<sub>FLAT(ON)</sub>**

Flatness that is defined as the difference between the maximum and minimum value of on resistance measured over the specified analog signal range.

**I<sub>S</sub> (Off)**

The source leakage current with the switch off.

**I<sub>D</sub> (Off)**

The drain leakage current with the switch off.

**I<sub>D</sub>, I<sub>S</sub> (On)**

The channel leakage current with the switch on.

**V<sub>INL</sub>**

The maximum input voltage for Logic 0.

**V<sub>INH</sub>**

The minimum input voltage for Logic 1.

**I<sub>INL</sub> (I<sub>INH</sub>)**

The input current of the digital input.

**C<sub>S</sub> (Off)**

The off switch source capacitance, which is measured with reference to ground.

**C<sub>D</sub> (Off)**

The off switch drain capacitance, which is measured with reference to ground.

**C<sub>D</sub>, C<sub>S</sub> (On)**

The on switch capacitance, which is measured with reference to ground.

**C<sub>IN</sub>**

The digital input capacitance.

**t<sub>TRANSITION</sub>**

The delay time between the 50% and 90% points of the digital input and switch on condition when switching from one address state to another.

**t<sub>ON</sub> (EN)**

The delay between applying the digital control input and the output switching on. See Figure 29, Test Circuit 4.

**t<sub>OFF</sub> (EN)**

The delay between applying the digital control input and the output switching off.

**Charge Injection**

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

**Off Isolation**

A measure of unwanted signal coupling through an off switch.

**Crosstalk**

A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

**Bandwidth**

The frequency at which the output is attenuated by 3 dB.

**On Response**

The frequency response of the on switch.

**Insertion Loss**

The loss due to the on resistance of the switch.

**THD + N**

The ratio of the harmonic amplitude plus noise of the signal to the fundamental.

**ACPSRR (AC Power Supply Rejection Ratio)**

The ratio of the amplitude of signal on the output to the amplitude of the modulation. This is a measure of the ability of the device to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p.

TEST CIRCUITS

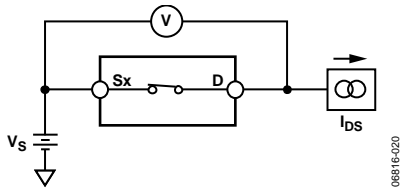
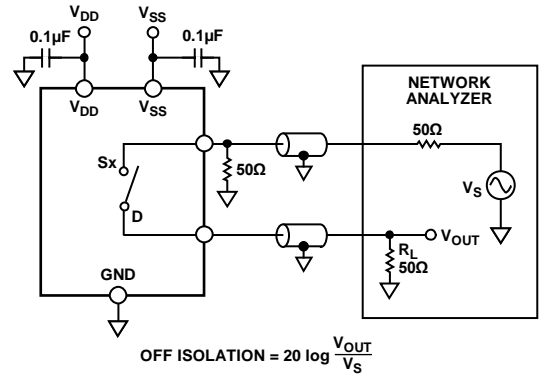


Figure 22. On Resistance

06816-020



$$\text{OFF ISOLATION} = 20 \log \frac{V_{\text{OUT}}}{V_s}$$

Figure 25. Off Isolation

06816-027

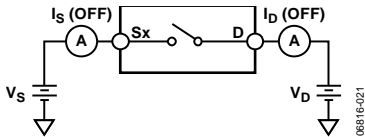
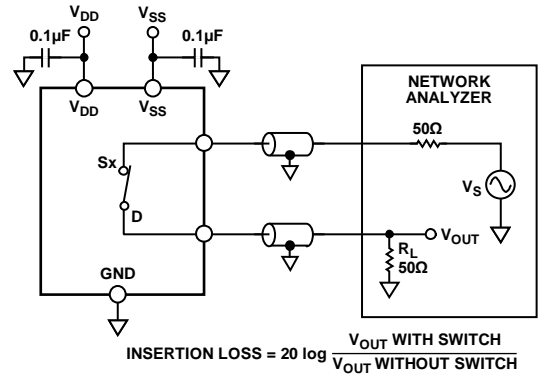


Figure 23. Off Leakage

06816-021



$$\text{INSERTION LOSS} = 20 \log \frac{V_{\text{OUT WITH SWITCH}}}{V_{\text{OUT WITHOUT SWITCH}}}$$

Figure 26. Bandwidth

06816-028

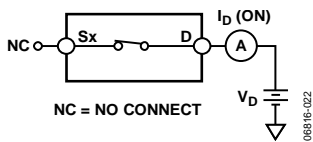
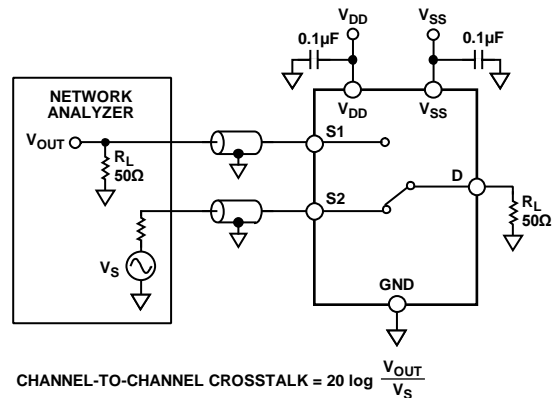


Figure 24. On Leakage

06816-022



$$\text{CHANNEL-TO-CHANNEL CROSSTALK} = 20 \log \frac{V_{\text{OUT}}}{V_s}$$

Figure 27. Channel-to-Channel Crosstalk

06816-029

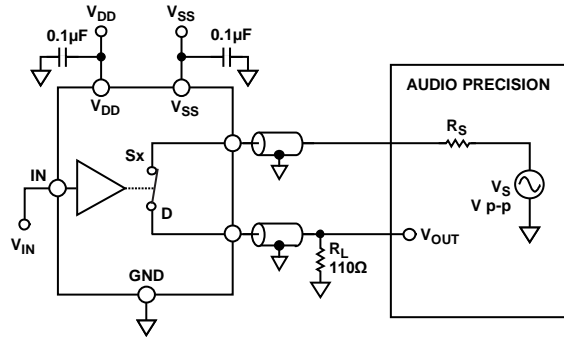


Figure 28. THD + Noise

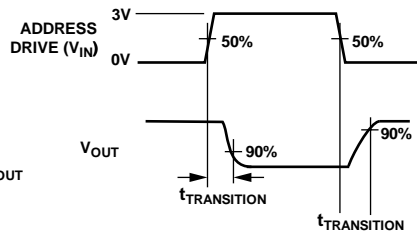
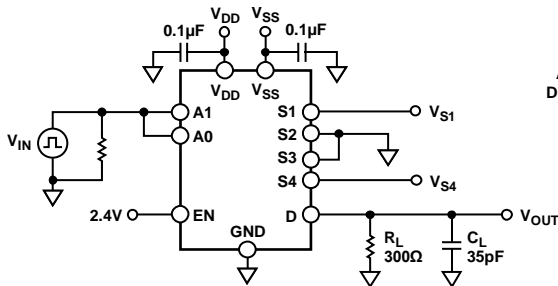


Figure 29. Address to Output Switching Times

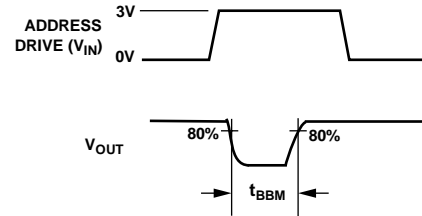
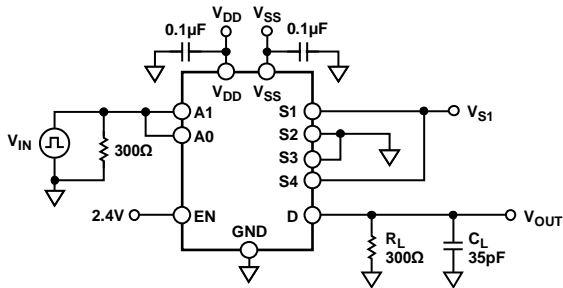


Figure 30. Break-Before-Make Time Delay

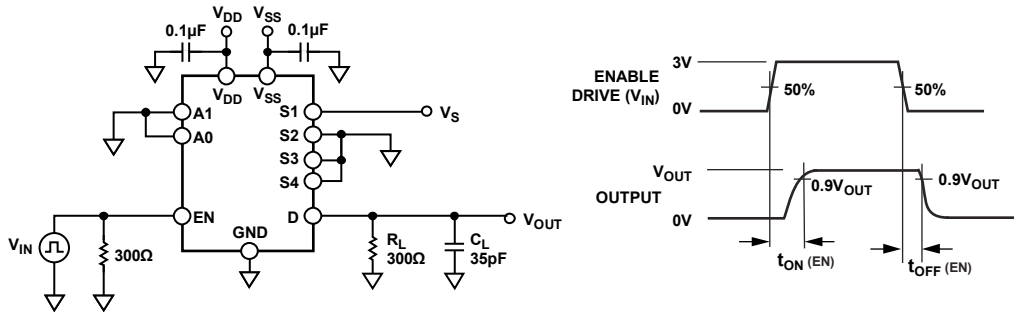


Figure 31. Enable-to-Output Switching Delay

06816-025

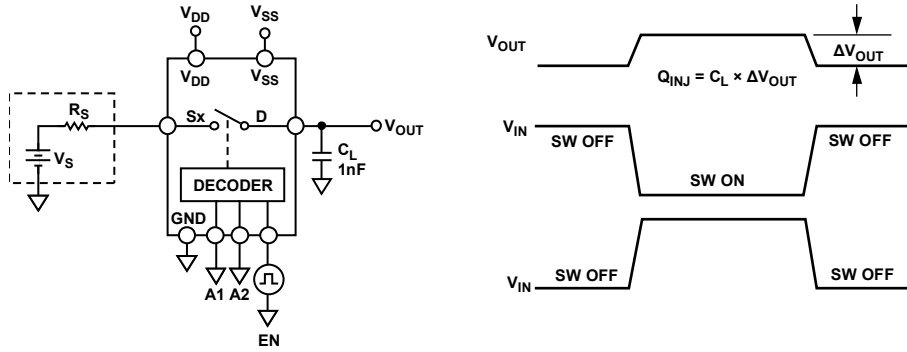
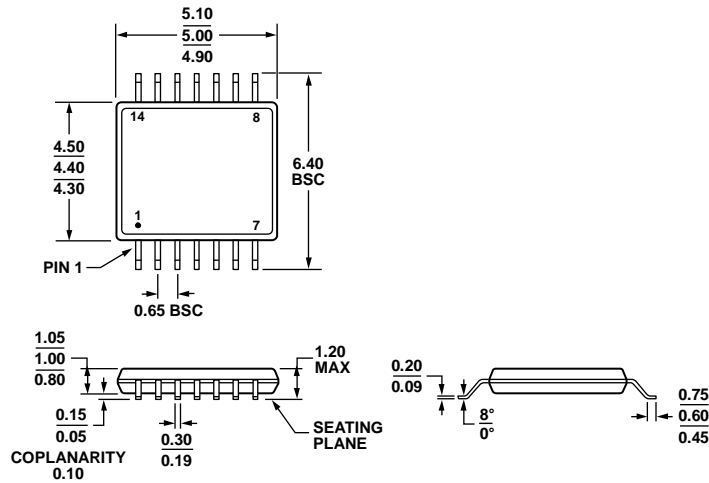


Figure 32. Charge Injection

06816-026



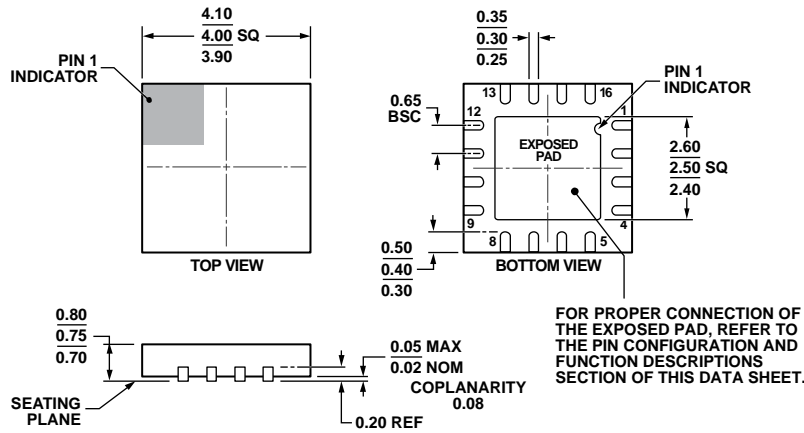
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

Figure 33. 14-Lead Thin Shrink Small Outline Package [TSSOP] (RU-14)

Dimension shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WGGC.

Figure 34. 16-Lead Lead Frame Chip Scale Package [LFCSP] 4 mm x 4 mm Body and 0.75 mm Package Height (CP-16-26)

Dimensions shown in millimeters

ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option
ADG1404YRUZ	-40°C to +125°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14
ADG1404YRUZ-REEL7	-40°C to +125°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14
ADG1404YCPZ-REEL	-40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-26
ADG1404YCPZ-REEL7	-40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-26

<sup>1</sup> Z = RoHS Compliant Part.