

N-channel TrenchMOS logic level FET 28 July 2016

Product data sheet

1. General description

Logic level N-channel MOSFET in a SOT404 package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

2. Features and benefits

- AEC Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with Vgst(th) rating of greater than 0.5V at 175 °C

3. Applications

- 12 V Automotive systems
- Motors, lamps and solenoid control
- Start-Stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

4. Quick reference data

Table 1. Qui	ck reference data						
Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C		-	-	40	V
I _D	drain current	V _{GS} = 5 V; T _{mb} = 25 °C; <u>Fig. 2</u>	[1]	-	-	120	А
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 1</u>		-	-	349	W
Static characteristics							
R _{DSon}	drain-source on-state resistance	V _{GS} = 5 V; I _D = 25 A; T _j = 25 °C; <u>Fig. 11</u>		-	1.35	1.6	mΩ
Dynamic characteristics							
Q _{GD}	gate-drain charge	V _{GS} = 5 V; I _D = 25 A; V _{DS} = 32 V; Fig. 13; Fig. 14		-	40.9	-	nC

[1] Continuous current is limited by package.





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5. Pinning information

Table 2.	Pinning	information		
Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	mb	D
2	D	drain		
3	S	source		G-UFA
mb	D	mounting base; connected to drain	D2PAK (SOT404)	mbb076 S

6. Ordering information

Table 3. Ordering information							
Type number	Package	Je					
	Name	Description	Version				
BUK961R6-40E	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404				

7. Marking

Table 4. Marking codes	
Type number	Marking code
BUK961R6-40E	BUK961R6-40E

8. Limiting values

Table 5.Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

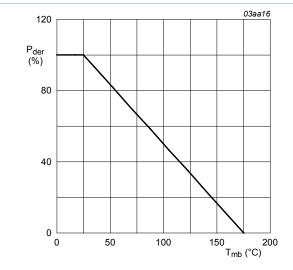
drain-source voltage drain-gate voltage	$T_j ≥ 25 °C; T_j ≤ 175 °C$ $R_{GS} = 20 kΩ$		-	40	V
	R _{GS} = 20 kΩ				
			-	40	V
gate-source voltage	T _j ≤ 175 °C; DC		-10	10	V
	$T_j \le 175 \text{ °C}; \text{Pulsed}$	[1][2]	-15	15	V
total power dissipation	T _{mb} = 25 °C; <u>Fig. 1</u>		-	349	W
drain current	T _{mb} = 25 °C; V _{GS} = 5 V; <u>Fig. 2</u>	[3]	-	120	Α
	T _{mb} = 100 °C; V _{GS} = 5 V; <u>Fig. 2</u>	[3]	-	120	А
peak drain current	T_{mb} = 25 °C; pulsed; $t_p \le 10 \ \mu$ s; <u>Fig. 3</u>		-	1348	А
storage temperature			-55	175	°C
	total power dissipation drain current peak drain current storage temperature	$T_{j} \le 175 \text{ °C; Pulsed}$ total power dissipation $T_{mb} = 25 \text{ °C; Fig. 1}$ drain current $T_{mb} = 25 \text{ °C; V_{GS}} = 5 \text{ V; Fig. 2}$ $T_{mb} = 100 \text{ °C; V_{GS}} = 5 \text{ V; Fig. 2}$ peak drain current $T_{mb} = 25 \text{ °C; pulsed; t}_{p} \le 10 \mu\text{s; Fig. 3}$	$\begin{tabular}{ c c c c } \hline T_j \leq 175 \ ^\circ\mbox{C; Pulsed} & [1][2] \\ \hline T_{mb} = 25 \ ^\circ\mbox{C; Fig. 1} & & & & & & \\ \hline T_{mb} = 25 \ ^\circ\mbox{C; V}_{GS} = 5 \ ^\circ\mbox{V; Fig. 2} & [3] \\ \hline T_{mb} = 100 \ ^\circ\mbox{C; V}_{GS} = 5 \ ^\circ\mbox{V; Fig. 2} & [3] \\ \hline peak drain current & & & & & & \\ \hline T_{mb} = 25 \ ^\circ\mbox{C; pulsed; t}_p \leq 10 \ \mbox{\mus; Fig. 3} & & & \\ \hline storage temperature & & & & & & \\ \hline \end{array}$	$\begin{tabular}{ c c c c } \hline T_{j} \leq 175 \ ^{\circ}C; \ Pulsed & [1][2] & -15 \\ \hline T_{mb} = 25 \ ^{\circ}C; \ Fig. 1 & - \\ \hline drain \ current & $T_{mb} = 25 \ ^{\circ}C; \ V_{GS} = 5 \ V; \ Fig. 2 & [3] & - \\ \hline T_{mb} = 100 \ ^{\circ}C; \ V_{GS} = 5 \ V; \ Fig. 2 & [3] & - \\ \hline T_{mb} = 100 \ ^{\circ}C; \ V_{GS} = 5 \ V; \ Fig. 2 & [3] & - \\ \hline peak \ drain \ current & $T_{mb} = 25 \ ^{\circ}C; \ pulsed; \ t_{p} \leq 10 \ \mu s; \ Fig. 3 & - \\ \hline storage \ temperature & $I = 100 \ ^{\circ}C; \ Pulsed; \ t_{p} \leq 10 \ \mu s; \ Fig. 3 & - \\ \hline Storage \ temperature & $I = 100 \ ^{\circ}C; \ pulsed; \ t_{p} \leq 10 \ \mu s; \ Fig. 3 & - \\ \hline Storage \ temperature & $I = 100 \ ^{\circ}C; \ pulsed; \ t_{p} \leq 10 \ \mu s; \ Fig. 3 & - \\ \hline Storage \ temperature & $I = 100 \ ^{\circ}C; \ pulsed; \ t_{p} \leq 10 \ \mu s; \ Fig. 3 & - \\ \hline Storage \ temperature & $I = 100 \ ^{\circ}C; \ pulsed; \ t_{p} \leq 10 \ \mu s; \ Fig. 3 & - \\ \hline Storage \ temperature & $I = 100 \ ^{\circ}C; \ pulsed; \ t_{p} \leq 10 \ \mu s; \ Fig. 3 & - \\ \hline Storage \ temperature & $I = 100 \ ^{\circ}C; \ pulsed; \ t_{p} \leq 10 \ \mu s; \ Fig. 3 & - \\ \hline Storage \ temperature & $I = 100 \ ^{\circ}C; \ pulsed; \ t_{p} \leq 10 \ \mu s; \ Fig. 3 & - \\ \hline Storage \ temperature & $I = 100 \ ^{\circ}C; \ pulsed; \ t_{p} \leq 10 \ \mu s; \ Fig. 3 & - \\ \hline Storage \ temperature & $I = 100 \ ^{\circ}C; \ Pulsed; \ t_{p} \leq 10 \ \mu s; \ Fig. 3 & - \\ \hline \ Storage \ temperature & $I = 100 \ ^{\circ}C; \ Pulsed; \ t_{p} \leq 10 \ \mu s; \ Fig. 3 & - \\ \hline \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \$	$\begin{tabular}{ c c c c c } \hline T_{j} \leq 175 \ ^{\circ}C; \ Pulsed & [1][2] & -15 & 15 \\ \hline T_{mb} = 25 \ ^{\circ}C; \ Fig. 1 & - & 349 \\ \hline drain \ current & $T_{mb} = 25 \ ^{\circ}C; \ V_{GS} = 5 \ V; \ Fig. 2 & [3] & - & 120 \\ \hline T_{mb} = 100 \ ^{\circ}C; \ V_{GS} = 5 \ V; \ Fig. 2 & [3] & - & 120 \\ \hline T_{mb} = 100 \ ^{\circ}C; \ V_{GS} = 5 \ V; \ Fig. 2 & [3] & - & 120 \\ \hline peak \ drain \ current & $T_{mb} = 25 \ ^{\circ}C; \ pulsed; \ t_p \leq 10 \ \mu s; \ Fig. 3 & - & 1348 \\ \hline storage \ temperature & $I = 0 \ I = 0 $

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Symbol	Parameter	Conditions		Min	Мах	Unit
Tj	junction temperature			-55	175	°C
Source-dra	ain diode			1	- 1	
I _S	source current	T _{mb} = 25 °C	[3]	-	120	А
I _{SM}	peak source current	pulsed; $t_p \le 10 \ \mu s$; $T_{mb} = 25 \ ^{\circ}C$		-	1348	А
Avalanche	ruggedness				- 1	
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	$ I_D = 120 \text{ A}; V_{sup} \le 40 \text{ V}; \text{ R}_{GS} = 50 \Omega; V_{GS} = 5 \text{ V}; \text{ T}_{j(init)} = 25 \text{ °C}; \text{ unclamped}; Fig. 4 $	[4][5]	-	1008	mJ

- Accumulated pulse duration up to 50 hours delivers zero defect ppm [1]
- [2] Significantly longer life times are achieved by lowering T_{j} and or V_{GS}
- [3] Continuous current is limited by package.
- Single-pulse avalanche rating limited by maximum junction temperature of 175 °C. Refer to application note AN10273 for further information. [4]
- [5]



Normalized total power dissipation as a Fig. 1. function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

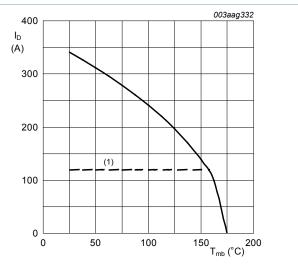
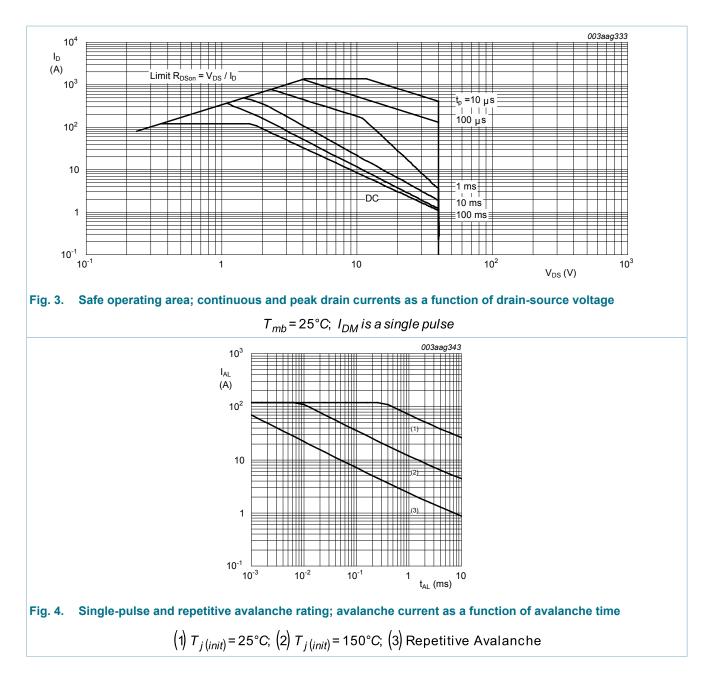


Fig. 2. Continuous drain current as a function of mounting base temperature

$V_{GS} \ge 5V$ (1) Capped at 120 A due to package.

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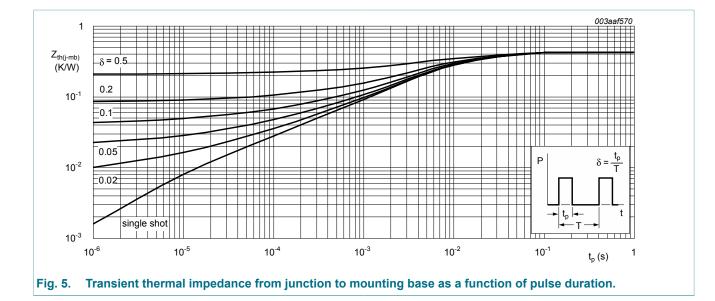


9. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{th(j-mb)}	thermal resistance from junction to mounting base	Fig. <u>5</u>	-	-	0.43	K/W
R _{th(j-a)}	thermal resistance from junction to ambient	minimum footprint ; mounted on a printed-circuit board	-	50	-	K/W

Table 6. Thermal characteristics

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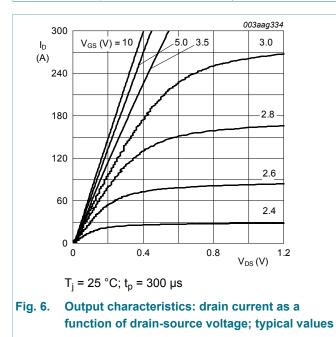


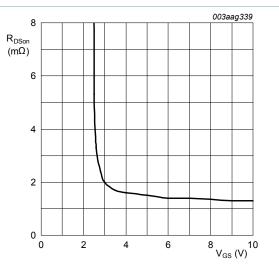
10. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics	· · · ·	I			
V _{(BR)DSS}	drain-source	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C	40	-	-	V
	breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C	36	-	-	V
V _{GS(th)}	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS} ; T_j = 25 °C; Fig. 9; Fig. 10	1.4	1.7	2.1	V
		I_D = 1 mA; V_{DS} = V_{GS} ; T_j = -55 °C; Fig. 9	-	-	2.45	V
	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ °C};$ Fig. 9	0.5	-	-	V	
I _{DSS}	drain leakage current	V_{DS} = 40 V; V_{GS} = 0 V; T_j = 25 °C	-	0.13	1	μA
		V _{DS} = 40 V; V _{GS} = 0 V; T _j = 175 °C	-	-	500	μA
GSS gate leakage current	gate leakage current	V_{GS} = 10 V; V_{DS} = 0 V; T_j = 25 °C	-	2	100	nA
		V_{GS} = -10 V; V_{DS} = 0 V; T_j = 25 °C	-	2	100	nA
R _{DSon} d	drain-source on-state	V _{GS} = 5 V; I _D = 25 A; T _j = 25 °C; <u>Fig. 11</u>	-	1.35	1.6	mΩ
	resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; Fig. 11	-	1.17	1.4	mΩ
		V _{GS} = 5 V; I _D = 25 A; T _j = 175 °C; Fig. 12; Fig. 11	-	-	3.1	mΩ
Dynamic cł	naracteristics	1				
Q _{G(tot)}	total gate charge	I_D = 25 A; V_{DS} = 32 V; V_{GS} = 5 V;	-	120	-	nC
Q _{GS}	gate-source charge	Fig. 13; Fig. 14	-	26.9	-	nC

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Symbol	Parameter	Conditions	N	lin	Тур	Мах	Unit
Q _{GD}	gate-drain charge		-		40.9	-	nC
C _{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz;	-		12300	16400	pF
C _{oss}	output capacitance	T _j = 25 °C; <u>Fig. 15</u>	-		1530	1840	pF
C _{rss}	reverse transfer capacitance		-		740	1020	pF
t _{d(on)}	turn-on delay time	$V_{DS} = 30 \text{ V}; \text{ R}_{L} = 1.2 \Omega; \text{ V}_{GS} = 5 \text{ V};$ $\text{R}_{G(ext)} = 5 \Omega$	-		95	-	ns
t _r	rise time		-		118	-	ns
t _{d(off)}	turn-off delay time		-		195	-	ns
t _f	fall time		-		119	-	ns
L _D	internal drain inductance	from upper edge of drain mounting base to center of die	-		2.5	-	nH
L _S	internal source inductance	from source lead to source bonding pad	-		7.5	-	nH
Source-dra	in diode						,
V _{SD}	source-drain voltage	I_{S} = 25 A; V_{GS} = 0 V; T_{j} = 25 °C; <u>Fig. 16</u>	-		0.77	1.2	V
t _{rr}	reverse recovery time	$I_{\rm S}$ = 20 A; dI _S /dt = -100 A/µs; V _{GS} = 0 V;	-		57	-	ns
Qr	recovered charge	V _{DS} = 25 V	-		97	-	nC



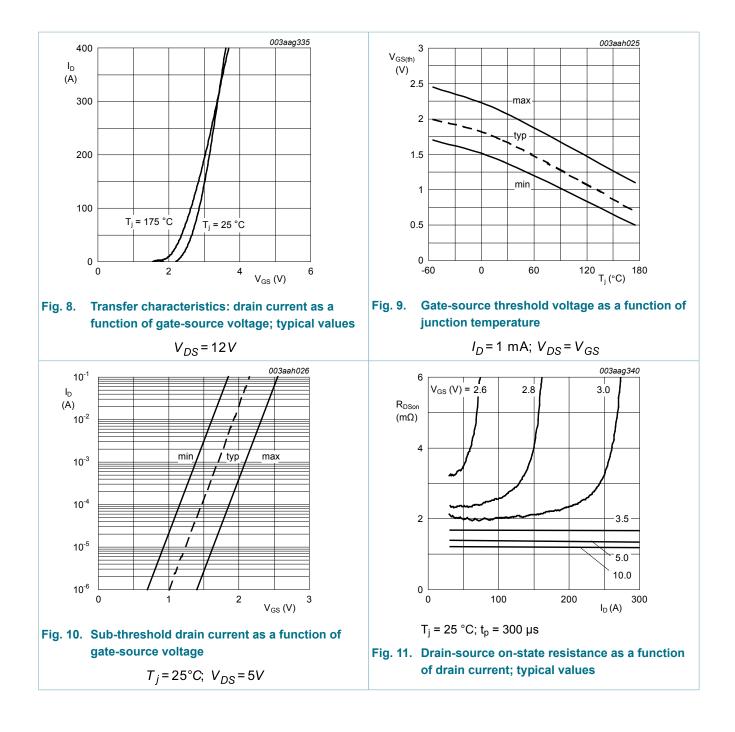




 $T_j = 25 \,^{\circ}C; I_D = 25A$

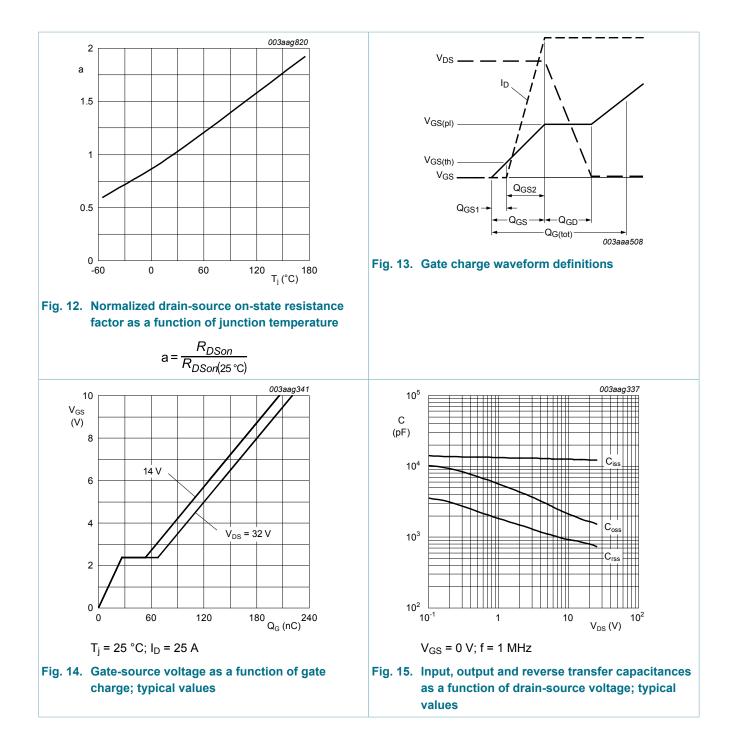
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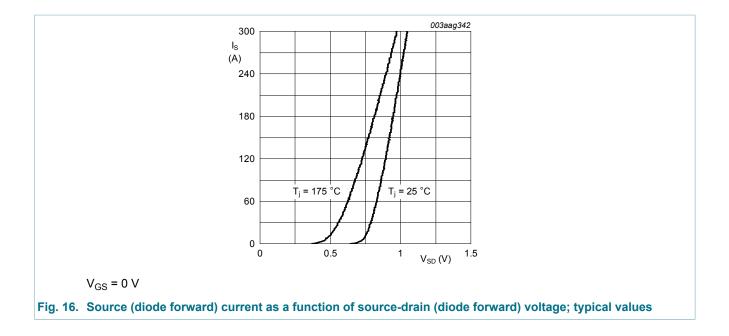
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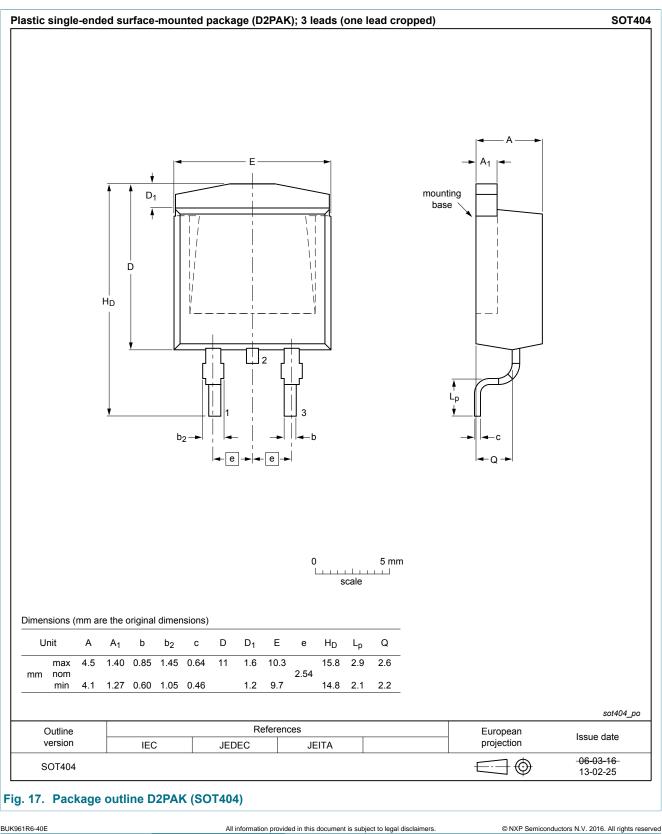
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11. Package outline



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12. Legal information

12.1 Data sheet status

Document status [1][2]	Product status [<u>3]</u>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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