24-Bit, 8-/16-Channel, 250 kSPS, Sigma-Delta ADC with True Rail-to-Rail Buffers

Data Sheet

AD7175-8

FEATURES

Fast and flexible output rate: 5 SPS to 250 kSPS
Channel scan data rate of 50 kSPS/channel (20 µs settling)
Performance specifications
- **17.2 noise free bits at 250 kSPS**
- **20.2 noise free bits at 2.5 kSPS**
- **24 noise free bits at 20 SPS**
- **INL: ±1 ppm of FSR**

85 dB filter rejection of 50 Hz and 60 Hz with 50 ms settling
User configurable input channels
- **8 fully differential channels or 16 single-ended channels**
- **Crosspoint multiplexer**

On-chip 2.5 V reference (±2 ppm/°C drift)
True rail-to-rail analog and reference input buffers
Internal or external clock
Power supply: AVDD1 − AVSS = 5 V, AVDD2 = IOVDD = 2 V to 5 V (nominal)
- **Split supply with AVDD1/AVSS at ±2.5 V**

ADC current: 8.4 mA
Temperature range: −40°C to +105°C
3- or 4-wire serial digital interface (Schmitt trigger on SCLK)
- **Serial port interface (SPI), QSPI, MICROWIRE, and DSP compatible**

APPLICATIONS

Process control: PLC/DCS modules
- **Temperature and pressure measurement**

Medical and scientific multichannel instrumentation
Chromatography

GENERAL DESCRIPTION

The AD7175-8 is a low noise, fast settling, multiplexed, 8-/16-channel (fully/pseudo differential) Σ-Δ analog-to-digital converter (ADC) for low bandwidth inputs. It has a maximum channel scan rate of 50 kSPS (20 µs) for fully settled data. The output data rates range from 5 SPS to 250 kSPS.

The AD7175-8 integrates key analog and digital signal conditioning blocks to allow users to configure an individual setup for each analog input channel in use. Each feature can be user selected on a per channel basis. Integrated true rail-to-rail buffers on the analog inputs and external reference inputs provide easy to drive high impedance inputs. The precision 2.5 V low drift (2 ppm/°C) band gap internal reference (with output reference buffer) adds embedded functionality to reduce external component count.

The digital filter allows simultaneous 50 Hz and 60 Hz rejection at a 27.27 SPS output data rate. The user can switch between different filter options according to the demands of each channel in the application. The ADC automatically switches through each selected channel. Further digital processing functions include offset and gain calibration registers, configurable on a per channel basis.

The device operates with a 5 V AVDD1 − AVSS supply, or with ±2.5 V AVDD1/AVSS, and 2 V to 5 V AVDD2 and IOVDD nominal supplies. The specified operating temperature range is −40°C to +105°C. The AD7175-8 is available in a 40-lead LFCSP package.

FUNCTIONAL BLOCK DIAGRAM

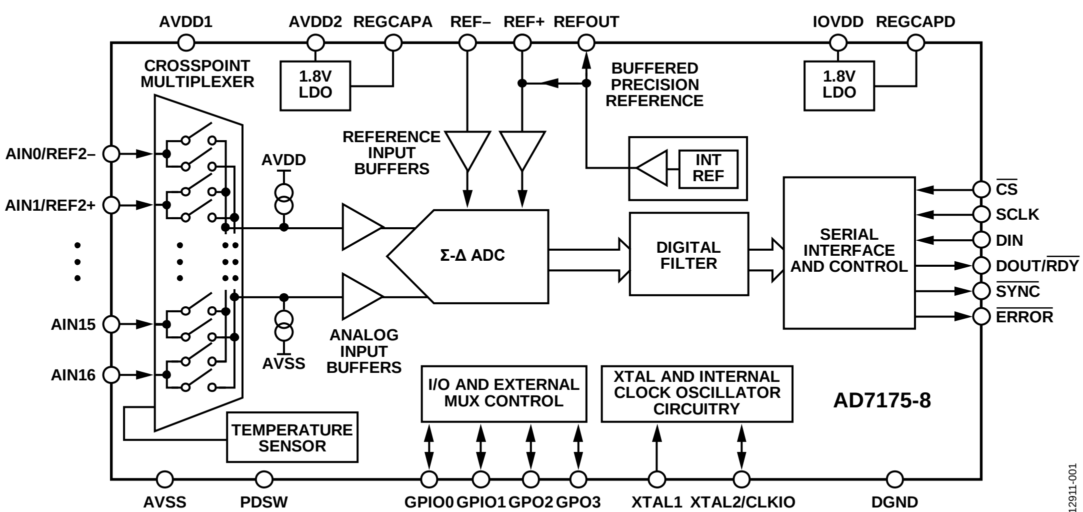

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Figure 1.

Rev. 0

Document Feedback

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- AD7175-8 Evaluation Board

Documentation

Data Sheet

- AD7175-8: 24-Bit, 8-/16-Channel, 250 kSPS, Sigma- Delta ADC with True Rail-to-Rail Buffers Preliminary Data Sheet

User Guides

- UG-901: Evaluating the AD7175-8 24-Bit, 250 kSPS, Sigma-Delta ADC with 20 µs Settling and Integrated Analog Input Buffers

Software and Systems Requirements

- AD7175 Microcontroller Renesas Driver
- AD717x Microcontroller No-OS
- AD717x Eval+ Software

Reference Designs

- CN0292

Design Resources

- AD7175-8 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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TABLE OF CONTENTS

REVISION HISTORY

10/15—Revision 0: Initial Version

SPECIFICATIONS

AVDD1 = 4.5 V to 5.5 V, AVDD2 = 2 V to 5.5 V, IOVDD = 2 V to 5.5 V, AVSS = DGND = 0 V, REF+ = 2.5 V, REF− = AVSS, internal master clock (MCLK) = 16 MHz, $T_A = T_{MIN}$ to T_{MAX} (−40°C to +105°C), unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ADC SPEED AND PERFORMANCE					
Output Data Rate (ODR)		5		250,000	SPS
No Missing Codes[1]	Excluding sinc3 filter ≥ 125 kSPS	24			Bits
Resolution	See Table 19 to Table 23				
Noise	See Table 19 to Table 23				
ACCURACY					
Integral Nonlinearity (INL)	All input buffers enabled		±4.5	10	ppm of FSR
	All input buffers disabled		±1	±4.5	ppm of FSR
Offset Error[2]	Internal short		±60		µV
Offset Drift	Internal short		±150		nV/°C
Gain Error[2]			±80	±110	ppm of FSR
Gain Drift[1]			±0.5	±0.75	ppm/°C
REJECTION					
Power Supply Rejection	AVDD1, AVDD2, for V_{IN} = 1 V		90		dB
Common-Mode Rejection	V_{IN} = 0.1 V				
At DC		95			dB
At 50 Hz, 60 Hz[1]	20 Hz output data rate (post filter), 50 Hz ± 1 Hz and 60 Hz ± 1 Hz	120			dB
Normal Mode Rejection[1]	50 Hz ± 1 Hz and 60 Hz ± 1 Hz				
	Internal clock, 20 SPS ODR (postfilter)	71	90		dB
	External clock, 20 SPS ODR (postfilter)	85	90		dB
ANALOG INPUTS					
Differential Input Range	V_{REF} = (REF+) − (REF−)		$\pm V_{REF}$		V
Absolute Voltage Limits[1]					
Input Buffers Disabled		AVSS − 0.05		AVDD1 + 0.05	V
Input Buffers Enabled		AVSS		AVDD1	V
Analog Input Current					
Input Buffers Disabled					
Input Current			±48		µA/V
Input Current Drift	External clock		±0.75		nA/V/°C
	Internal clock		±4		nA/V/°C
Input Buffers Enabled					
Input Current			±30		nA
Input Current Drift	AVDD1 − 0.2 V to AVSS + 0.2 V		±75		pA/°C
	AVDD1 to AVSS		±1		nA/°C
Crosstalk	1 kHz input		−120		dB
INTERNAL REFERENCE	100 nF external capacitor to AVSS				
Output Voltage	REFOUT, with respect to AVSS		2.5		V
Initial Accuracy[3]	REFOUT, T_A = 25°C	−0.12		+0.12	% of V
Temperature Coefficient[1]					
0°C to 105°C			±2	±5	ppm/°C
−40°C to +105°C			±3	±10	ppm/°C
Reference Load Current, I_{LOAD}		−10		+10	mA
Power Supply Rejection	AVDD1, AVDD2 (line regulation)		95		dB
Load Regulation	$\Delta V_{OUT}/\Delta I_{LOAD}$		32		ppm/mA
Voltage Noise	e_N, 0.1 Hz to 10 Hz, 2.5 V reference		4.5		µV rms
Voltage Noise Density	e_N, 1 kHz, 2.5 V reference		215		nV/√Hz

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Turn-On Settling Time	100 nF REFOUT capacitor		200		µs
Short-Circuit Current, I_{SC}			25		mA
EXTERNAL REFERENCE INPUTS					
Differential Input Range	V_{REF} = (REF+) − (REF−)	1	2.5	AVDD1	V
Absolute Voltage Limits[1]					
Input Buffers Disabled		AVSS − 0.05		AVDD1 + 0.05	V
Input Buffers Enabled		AVSS		AVDD1	V
REF+/REF− Input Current					
Input Buffers Disabled					
Input Current			±72		µA/V
Input Current Drift	External clock		±1.2		nA/V/°C
	Internal clock		±6		nA/V/°C
Input Buffers Enabled					
Input Current			±800		nA
Input Current Drift			1.2		nA/°C
Normal Mode Rejection[1]	See the Rejection parameter				
Common-Mode Rejection			95		dB
TEMPERATURE SENSOR					
Accuracy	After user calibration at 25°C		±2		°C
Sensitivity			470		µV/K
BURNOUT CURRENTS					
Source/Sink Current	Analog input buffers must be enabled		±10		µA
POWER-DOWN SWITCH					
R_{ON}			24		Ω
Allowable Currents				16	mA
GENERAL-PURPOSE INPUTS/OUTPUTS (GPIO0, GPIO1, GPO2, GPO3)	With respect to AVSS				
Input Mode Leakage Current[1]		−10		+10	µA
Floating State Output Capacitance			5		pF
Output High Voltage, V_{OH}[1]	I_{SOURCE} = 200 µA	AVSS + 4			V
Output Low Voltage, V_{OL}[1]	I_{SINK} = 800 µA			AVSS + 0.4	V
Input High Voltage, V_{INH}[1]		AVSS + 3			V
Input Low Voltage, V_{INL}[1]				AVSS + 0.7	V
CLOCK					
Internal Clock					
Frequency			16		MHz
Accuracy		−2.5%		+2.5%	%
Duty Cycle			50		%
Output Low Voltage, V_{OL}				0.4	V
Output High Voltage, V_{OH}		0.8 × IOVDD			V
Crystal					
Frequency		14	16	16.384	MHz
Start-Up Time			10		µs
External Clock (CLKIO)			16	16.384	MHz
Duty Cycle[1]		30	50	70	%

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
LOGIC INPUTS					
Input High Voltage, V_{INH}[1]	2 V ≤ IOVDD < 2.3 V	0.65 × IOVDD			V
	2.3 V ≤ IOVDD ≤ 5.5 V	0.7 × IOVDD			V
Input Low Voltage, V_{INL}[1]	2 V ≤ IOVDD < 2.3 V			0.35 × IOVDD	V
	2.3 V ≤ IOVDD ≤ 5.5 V			0.7	V
Hysteresis[1]	IOVDD ≥ 2.7 V	0.08		0.25	V
	IOVDD < 2.7 V	0.04		0.2	V
Leakage Current		−10		+10	µA
LOGIC OUTPUT (DOUT/$\overline{RDY}$)					
Output High Voltage, V_{OH}[1]	IOVDD ≥ 4.5 V, I_{SOURCE} = 1 mA	0.8 × IOVDD			V
	2.7 V ≤ IOVDD < 4.5 V, I_{SOURCE} = 500 µA	0.8 × IOVDD			V
	IOVDD < 2.7 V, I_{SOURCE} = 200 µA	0.8 × IOVDD			V
Output Low Voltage, V_{OL}[1]	IOVDD ≥ 4.5 V, I_{SINK} = 2 mA			0.4	V
	2.7 V ≤ IOVDD < 4.5 V, I_{SINK} = 1 mA			0.4	V
	IOVDD < 2.7 V, I_{SINK} = 400 µA			0.4	V
Leakage Current	Floating state	−10		+10	µA
Output Capacitance	Floating state		10		pF
SYSTEM CALIBRATION[1]					
Full-Scale (FS) Calibration Limit				1.05 × FS	V
Zero-Scale Calibration Limit		−1.05 × FS			V
Input Span		0.8 × FS		2.1 × FS	V
POWER REQUIREMENTS					
Power Supply Voltage					
AVDD1 to AVSS		4.5	5	5.5	V
AVDD2 to AVSS[4]		2	2.5 to 5	5.5	V
AVSS to DGND		−2.75		0	V
IOVDD to DGND[4]		2	2.5 to 5	5.5	V
IOVDD to AVSS	For AVSS < DGND			6.35	V
POWER SUPPLY CURRENTS[5]	All outputs unloaded, digital inputs connected to IOVDD or DGND				
Full Operating Mode					
AVDD1 Current	Analog input and reference input buffers (AIN±, REF±) disabled, external reference		1.4	1.65	mA
	Analog input and reference input buffers disabled, internal reference		1.75	2	mA
	Analog input and reference input buffers enabled, external reference		13	16	mA
	Each buffer: AIN+, AIN−, REF+, REF−		2.9		mA
AVDD2 Current	External reference		4.5	5	mA
	Internal reference		4.75	5.2	mA
IOVDD Current	External clock		2.5	2.8	mA
	Internal clock		2.75	3.1	mA
	External crystal		3		mA
Standby Mode (LDO On)	Internal reference off, total current consumption		30		µA
	Internal reference on, total current consumption		425		µA
Power-Down Mode	Full power-down (including LDO and internal reference)		5	10	µA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER DISSIPATION[5]					
Full Operating Mode	All buffers disabled, external clock and reference, AVDD2 = 2 V, IOVDD = 2 V		21		mW
	All buffers disabled, external clock and reference, all supplies = 5 V		42		mW
	All buffers disabled, external clock and reference, all supplies = 5.5 V			52	mW
	All buffers enabled, internal clock and reference, AVDD2 = 2 V, IOVDD = 2 V		82		mW
	All buffers enabled, internal clock and reference, all supplies = 5 V		105		mW
	All buffers enabled, internal clock and reference, all supplies = 5.5 V			136	mW
Standby Mode	Internal reference off, all supplies = 5 V		150		μW
	Internal reference on, all supplies = 5 V		2.2		mW
Power-Down Mode	Full power-down, all supplies = 5 V		25	50	μW

[1] This specification is not production tested but is supported by characterization data at the initial product release.
[2] Following a system or internal zero-scale calibration, the offset error is in the order of the noise for the programmed output data rate selected. A system full-scale calibration reduces the gain error to the order of the noise for the programmed output data rate.
[3] This specification includes moisture sensitivity level (MSL) preconditioning effects.
[4] The nominal range is 2 V to 5 V.
[5] This specification is with no load on the REFOUT and digital output pins.

TIMING CHARACTERISTICS

IOVDD = 2 V to 5.5 V, DGND = 0 V, Input Logic 0 = 0 V, Input Logic 1 = IOVDD, C_{LOAD} = 20 pF, unless otherwise noted.

Table 2.

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Description[1, 2]
SCLK			
t_3	25	ns min	SCLK high pulse width
t_4	25	ns min	SCLK low pulse width
READ OPERATION			
t_1	0	ns min	$\overline{CS}$ falling edge to DOUT/$\overline{RDY}$ active time
	15	ns max	IOVDD = 4.75 V to 5.5 V
	40	ns max	IOVDD = 2 V to 3.6 V
t_2[3]	0	ns min	SCLK active edge to data valid delay[4]
	12.5	ns max	IOVDD = 4.75 V to 5.5 V
	25	ns max	IOVDD = 2 V to 3.6 V
t_5[5]	2.5	ns min	Bus relinquish time after $\overline{CS}$ inactive edge
	20	ns max	
t_6	0	ns min	SCLK inactive edge to $\overline{CS}$ inactive edge
t_7	10	ns min	SCLK inactive edge to DOUT/$\overline{RDY}$ high/low
WRITE OPERATION			
t_8	0	ns min	$\overline{CS}$ falling edge to SCLK active edge setup time[4]
t_9	8	ns min	Data valid to SCLK edge setup time
t_{10}	8	ns min	Data valid to SCLK edge hold time
t_{11}	5	ns min	$\overline{CS}$ rising edge to SCLK edge hold time

[1] Sample tested during initial release to ensure compliance.
[2] See Figure 2 and Figure 3.
[3] This parameter is defined as the time required for the output to cross the V_{OL} or V_{OH} limits.
[4] The SCLK active edge is the falling edge of SCLK.
[5] DOUT/$\overline{RDY}$ returns high after a read of the data register. In single conversion mode and continuous conversion mode, the same data can be read again, if required, while DOUT/$\overline{RDY}$ is high, although care must be taken to ensure that subsequent reads do not occur close to the next output update. If the continuous read feature is enabled, the digital word can be read only once.

Timing Diagrams

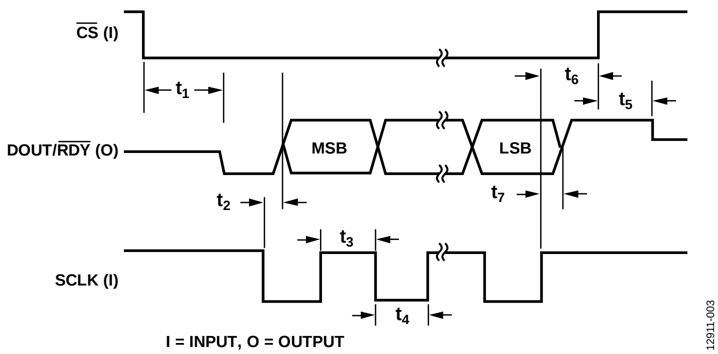


Figure 2. Read Cycle Timing Diagram

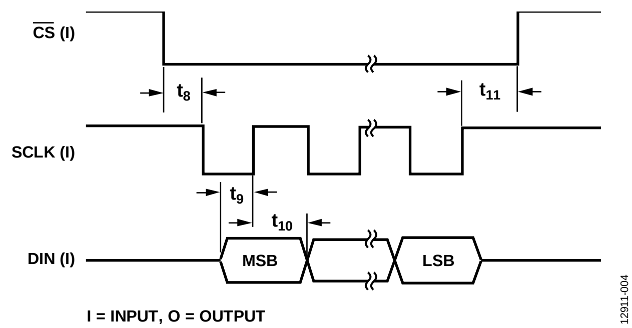


Figure 3. Write Cycle Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
AVDD1, AVDD2 to AVSS	−0.3 V to +6.5 V
AVDD1 to DGND	−0.3 V to +6.5 V
IOVDD to DGND	−0.3 V to +6.5 V
IOVDD to AVSS	−0.3 V to +7.5 V
AVSS to DGND	−3.25 V to +0.3 V
Analog Input Voltage to AVSS	−0.3 V to AVDD1 + 0.3 V
Reference Input Voltage to AVSS	−0.3 V to AVDD1 + 0.3 V
Digital Input Voltage to DGND	−0.3 V to IOVDD + 0.3 V
Digital Output Voltage to DGND	−0.3 V to IOVDD + 0.3 V
Analog Input/Digital Input Current	10 mA
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
Lead Soldering, Reflow Temperature	260°C
ESD Rating (Human Body Model)	4 kV

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for a device soldered on a JEDEC test board for surface-mount packages.

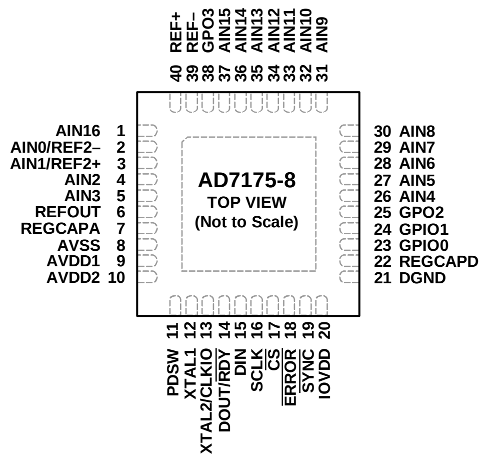
Table 4. Thermal Resistance

Package Type	θ_{JA}	Unit
40-Lead, 6 mm × 6 mm LFCSP		
1-Layer JEDEC Board	114	°C/W
4-Layer JEDEC Board	54	°C/W
4-Layer JEDEC Board with 16 Thermal Vias	34	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. SOLDER THE EXPOSED PAD TO A SIMILAR PAD ON THE PCB UNDER THE EXPOSED PAD TO CONFER MECHANICAL STRENGTH AND FOR HEAT DISSIPATION. THE EXPOSED PAD MUST BE CONNECTED TO AVSS THROUGH THIS PAD ON THE PCB.

12911-005

Figure 4. Pin Configuration

Table 5. Pin Function Descriptions[1]

Pin No.	Mnemonic	Type[2]	Description
1	AIN16	AI	Analog Input 16. This pin is selectable through the crosspoint multiplexer.
2	AIN0/REF2−	AI	Analog Input 0 (AIN0)/Reference 2, Negative Input (REF2−). An external reference can be applied between REF2+ and REF2−. REF2− can span from AVSS to AVDD1 − 1 V. Analog Input 0 is selectable through the crosspoint multiplexer. Reference 2 can be selected through the REF_SELx bits in the setup configuration registers.
3	AIN1/REF2+	AI	Analog Input 1 (AIN0)/Reference 2, Positive Input (REF2+). An external reference can be applied between REF2+ and REF2−. REF2+ spans from AVDD1 to AVSS + 1 V. Analog Input 1 is selectable through the crosspoint multiplexer. Reference 2 can be selected through the REF_SELx bits in the setup configuration registers.
4	AIN2	AI	Analog Input 2. This pin is selectable through the crosspoint multiplexer.
5	AIN3	AI	Analog Input 3. This pin is selectable through the crosspoint multiplexer.
6	REFOUT	AO	Buffered Output of Internal Reference. The output is 2.5 V with respect to AVSS.
7	REGCAPA	AO	Analog Low Dropout (LDO) Regulator Output. Decouple this pin to AVSS using a 1 µF capacitor.
8	AVSS	P	Negative Analog Supply. This supply ranges from 0 V to −2.75 V and is nominally set to 0 V.
9	AVDD1	P	Analog Supply Voltage 1. This voltage is 5 V ± 10% with respect to AVSS. AVDD1 − AVSS can be a single 5 V supply or a ±2.5 V split supply.
10	AVDD2	P	Analog Supply Voltage 2. This voltage ranges from 2 V to AVDD1 with respect to AVSS.
11	PDSW	AO	Power-Down Switch Connected to AVSS. This pin is controlled by the PDSW bit in the GPIOCON register.
12	XTAL1	AI	Input 1 for Crystal.
13	XTAL2/CLKIO	AI/DI	Input 2 for Crystal (XTAL2)/Clock Input or Output (CLKIO). See the CLOCKSEL bit settings in the ADCMODE register for more information.
14	DOUT/$\overline{\text{RDY}}$	DO	Serial Data Output (DOUT)/Data Ready Output ($\overline{\text{RDY}}$). This pin serves a dual purpose. It functions as a serial data output pin to access the output shift register of the ADC. The output shift register can contain data from any of the on-chip data or control registers. The data-word/control word information is placed on the DOUT/$\overline{\text{RDY}}$ pin on the SCLK falling edge and is valid on the SCLK rising edge. When $\overline{\text{CS}}$ is high, the DOUT/$\overline{\text{RDY}}$ output is tristated. When $\overline{\text{CS}}$ is low, and a register is not being read, DOUT/$\overline{\text{RDY}}$ operates as a data ready pin, going low to indicate the completion of a conversion. If the data is not read after the conversion, the pin goes high before the next update occurs. The DOUT/$\overline{\text{RDY}}$ falling edge can be used as an interrupt to a processor, indicating that valid data is available.

Pin No.	Mnemonic	Type[2]	Description
15	DIN	DI	Serial Data Input to the Input Shift Register on the ADC. Data in this shift register is transferred to the control registers in the ADC, with the register address (RA) bits of the communications register identifying the appropriate register. Data is clocked in on the rising edge of SCLK.
16	SCLK	DI	Serial Clock Input. This serial clock input is for data transfers to and from the ADC. SCLK has a Schmitt triggered input, making the interface suitable for opto-isolated applications.
17	$\overline{CS}$	DI	Chip Select Input. This pin is an active low logic input used to select the ADC. Use $\overline{CS}$ to select the ADC in systems with more than one device on the serial bus. $\overline{CS}$ can be hardwired low, allowing the ADC to operate in 3-wire mode with SCLK, DIN, and DOUT/$\overline{RDY}$ used to interface with the device. When $\overline{CS}$ is high, the DOUT/$\overline{RDY}$ output is tristated.
18	$\overline{ERROR}$	DI/O	Error input/output or General-Purpose Output. This pin can be used in one of the following three modes: Active low error input mode. This mode sets the ADC_ERROR bit in the STATUS register. Active low, open-drain error output mode. The status register error bits are mapped to the $\overline{ERROR}$ pin. The $\overline{ERROR}$ pins of multiple devices can be wired together to a common pull-up resistor so that an error on any device can be observed. General-purpose output mode. The status of the pin is controlled by the ERR_DAT bit in the GPIOCON register. The pin is referenced between IOVDD and DGND, as opposed to the AVDD1 and AVSS levels used by the GPIO1 and GPIO2 pins. The $\overline{ERROR}$ pin has an active pull-up circuit in this case.
19	$\overline{SYNC}$	DI	Synchronization Input. Allows synchronization of the digital filters and analog modulators when using multiple AD7175-8 devices.
20	IOVDD	P	Digital I/O Supply Voltage. The IOVDD voltage ranges from 2 V to 5 V (nominal). IOVDD is independent of AVDD1 and AVDD2. For example, IOVDD can be operated at 3.3 V when AVDD1 or AVDD2 equals 5 V, or vice versa. If AVSS is set to −2.5 V, the voltage on IOVDD must not exceed 3.6 V.
21	DGND	P	Digital Ground.
22	REGCAPD	AO	Digital LDO Regulator Output. This pin is for decoupling purposes only. Decouple this pin to DGND using a 1 µF capacitor.
23	GPIO0	DI/O	General-Purpose Input/Output 0. Logic input/output on this this pin is referred to the AVDD1 and AVSS supplies.
24	GPIO1	DI/O	General-Purpose Input/Output 2. Logic input/output on this this pin is referred to the AVDD1 and AVSS supplies.
25	GPO2	DO	General-Purpose Output 2. Logic output on this this pin is referred to the AVDD1 and AVSS supplies.
26	AIN4	AI	Analog Input 4. This pin is selectable through the crosspoint multiplexer.
27	AIN5	AI	Analog Input 5. This pin is selectable through the crosspoint multiplexer.
28	AIN6	AI	Analog Input 6. This pin is selectable through the crosspoint multiplexer.
29	AIN7	AI	Analog Input 7. This pin is selectable through the crosspoint multiplexer.
30	AIN8	AI	Analog Input 8. This pin is selectable through the crosspoint multiplexer.
31	AIN9	AI	Analog Input 9. This pin is selectable through the crosspoint multiplexer.
32	AIN10	AI	Analog Input 10. This pin is selectable through the crosspoint multiplexer.
33	AIN11	AI	Analog Input 11. This pin is selectable through the crosspoint multiplexer.
34	AIN12	AI	Analog Input 12. This pin is selectable through the crosspoint multiplexer.
35	AIN13	AI	Analog Input 13. This pin is selectable through the crosspoint multiplexer.
36	AIN14	AI	Analog Input 14. This pin is selectable through the crosspoint multiplexer.
37	AIN15	AI	Analog Input 15. This pin is selectable through the crosspoint multiplexer.
38	GPO3	DO	General-Purpose Output 3. Logic output on this this pin is referred to the AVDD1 and AVSS supplies.
39	REF−	AI	Reference 1 Input Negative Terminal. REF− can span from AVSS to AVDD1 − 1 V. Reference 1 can be selected through the REF_SELx bits in the setup configuration registers.
40	REF+	AI	Reference 1 Input Positive Terminal. An external reference can be applied between REF+ and REF−. REF+ can span from AVDD1 to AVSS + 1 V. Reference 1 can be selected through the REF_SELx bits in the setup configuration registers.
	EP	P	Exposed Pad. Solder the exposed pad to a similar pad on the PCB under the exposed pad to confer mechanical strength to the package and for heat dissipation. The exposed pad must be connected to AVSS through this pad on the PCB.

[1] Note that, throughout this data sheet, the dual function pin names are referenced by the relevant function only.
[2] AI = analog input, AO = analog output, P = power supply, DI = digital input, DO = digital output, and DI/O = bidirectional digital input/output.

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD1 = 5 V, AVDD2 = 5 V, IOVDD = 3.3 V, T_A = 25°C, unless otherwise noted.

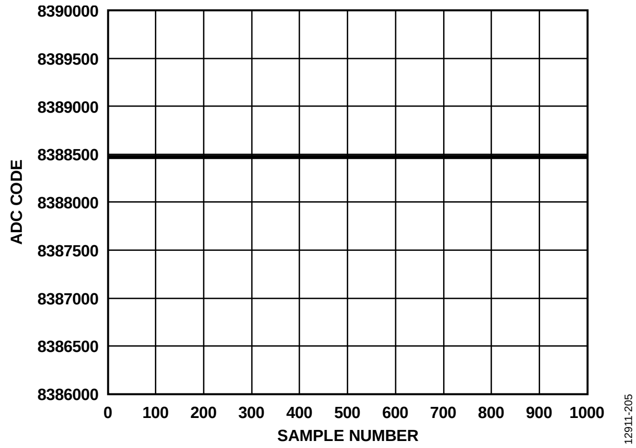


Figure 5. Noise (Analog Input Buffers Disabled, V_{REF} = 5 V, Output Data Rate = 5 SPS)

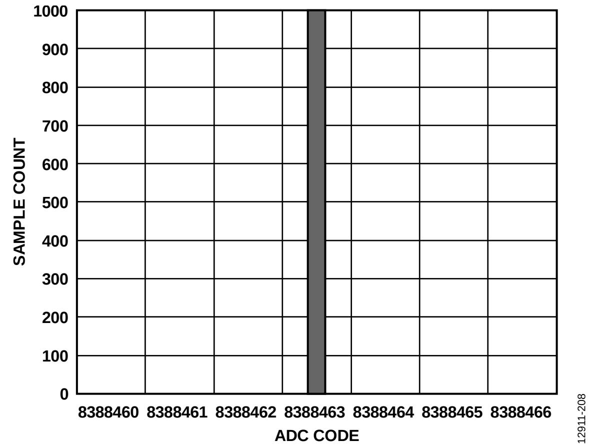


Figure 8. Histogram (Analog Input Buffers Disabled, V_{REF} = 5 V, Output Data Rate = 5 SPS)

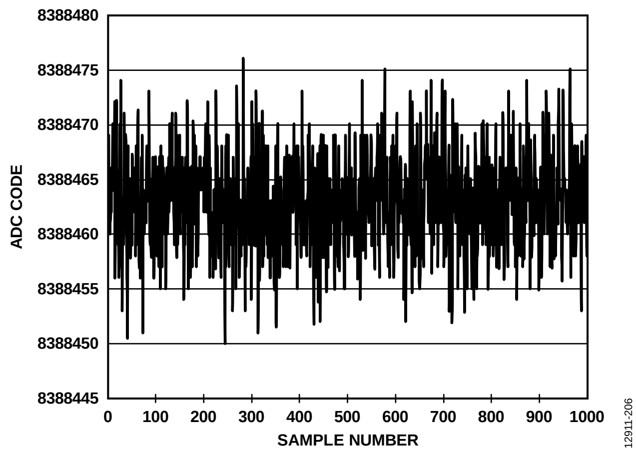


Figure 6. Noise (Analog Input Buffers Disabled, V_{REF} = 5 V, Output Data Rate = 10 kSPS)

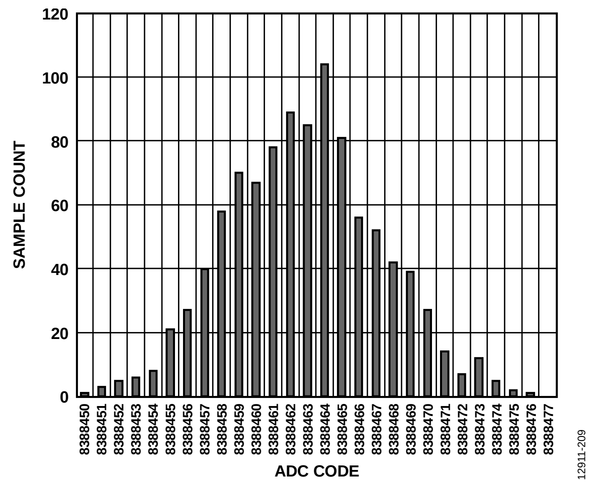


Figure 9. Histogram (Analog Input Buffers Disabled, V_{REF} = 5 V, Output Data Rate = 10 kSPS)

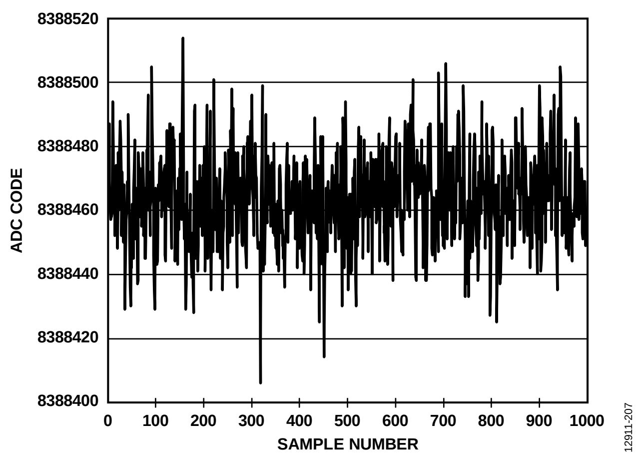


Figure 7. Noise (Analog Input Buffers Disabled, V_{REF} = 5 V, Output Data Rate = 250 kSPS)

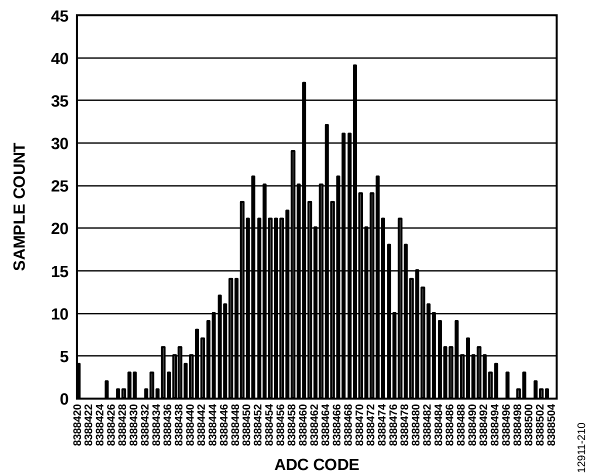


Figure 10. Histogram (Analog Input Buffers Disabled, V_{REF} = 5 V, Output Data Rate = 250 kSPS)

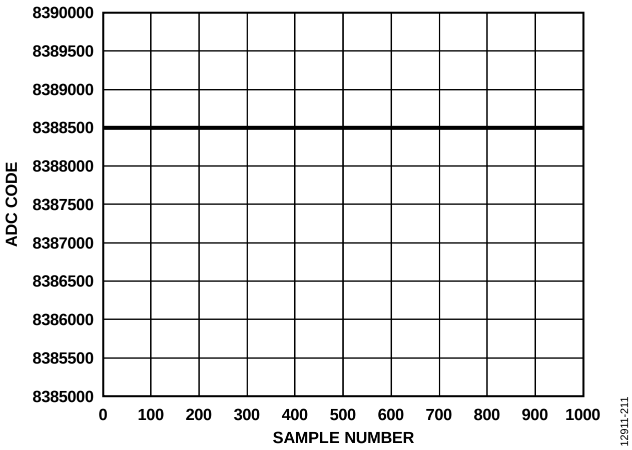


Figure 11. Noise (Analog Input Buffers Enabled, V_{REF} = 5 V, Output Data Rate = 5 SPS)

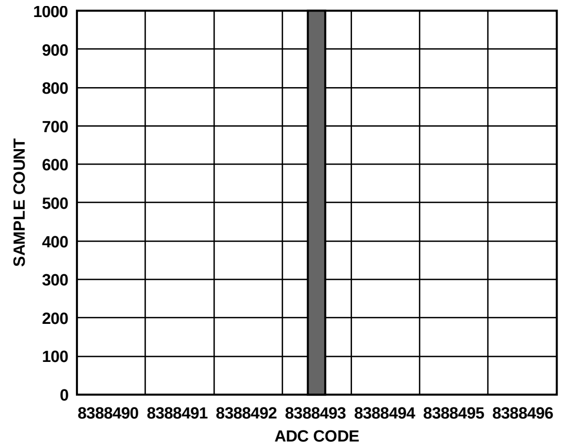


Figure 14. Histogram (Analog Input Buffers Enabled, V_{REF} = 5 V, Output Data Rate = 5 SPS)

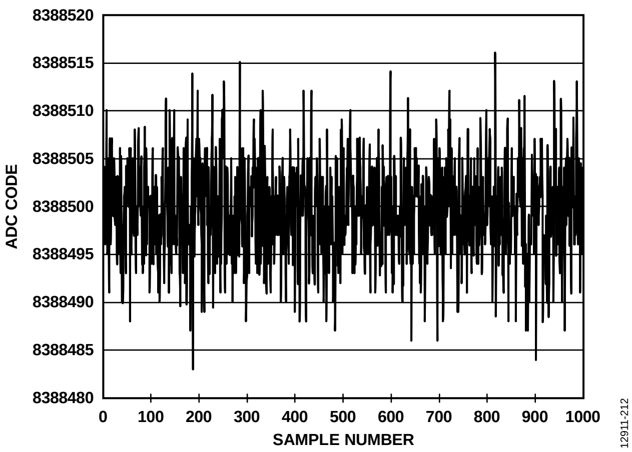


Figure 12. Noise (Analog Input Buffers Enabled, V_{REF} = 5 V, Output Data Rate = 10 kSPS)

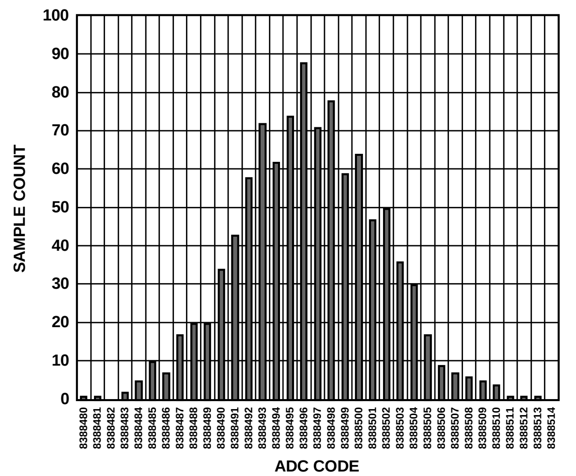


Figure 15. Histogram (Analog Input Buffers Enabled, V_{REF} = 5 V, Output Data Rate = 10 kSPS)

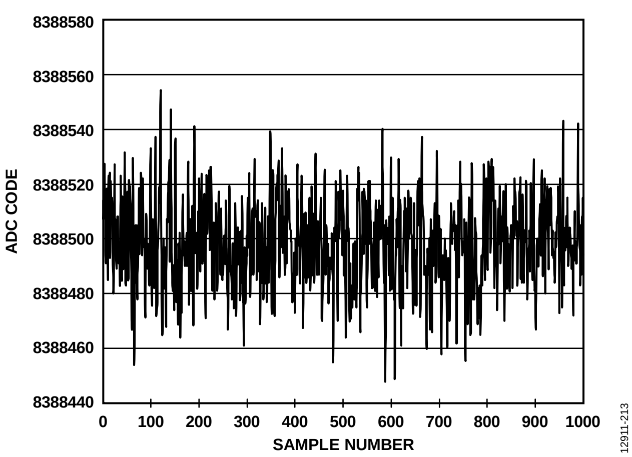


Figure 13. Noise (Analog Input Buffers Enabled, V_{REF} = 5 V, Output Data Rate = 250 kSPS)

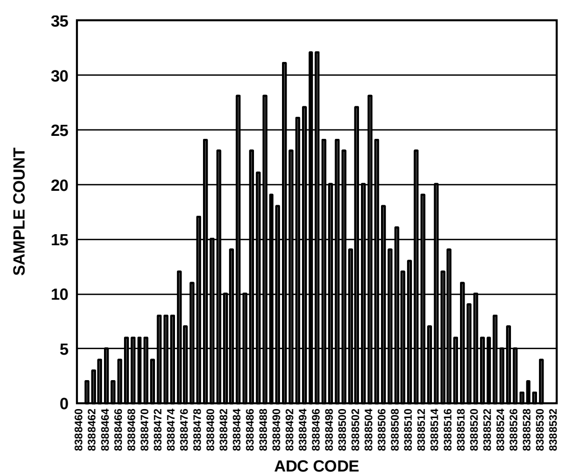


Figure 16. Histogram (Analog Input Buffers Enabled, V_{REF} = 5 V, Output Data Rate = 250 kSPS)

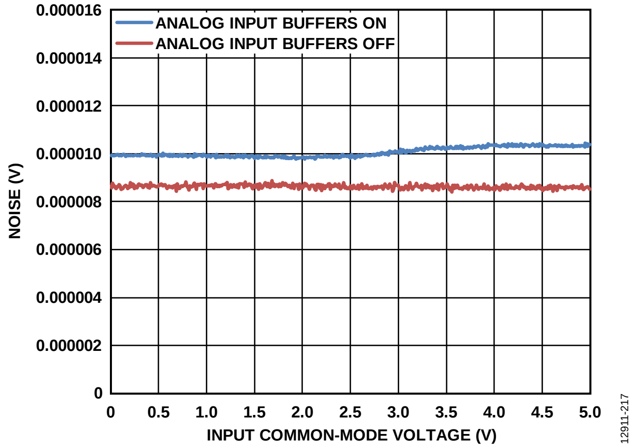


Figure 17. Noise vs. Input Common-Mode Voltage, Analog Input Buffers On and Off

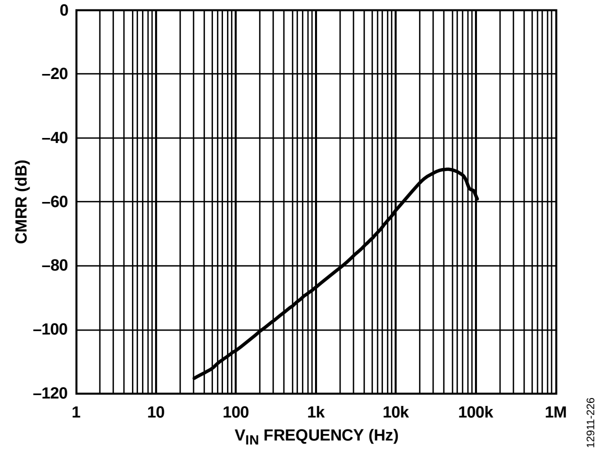


Figure 20. Common-Mode Rejection Ratio (CMRR) vs. V_{IN} Frequency (V_{IN} = 0.1 V, Output Data Rate = 250 kSPS)

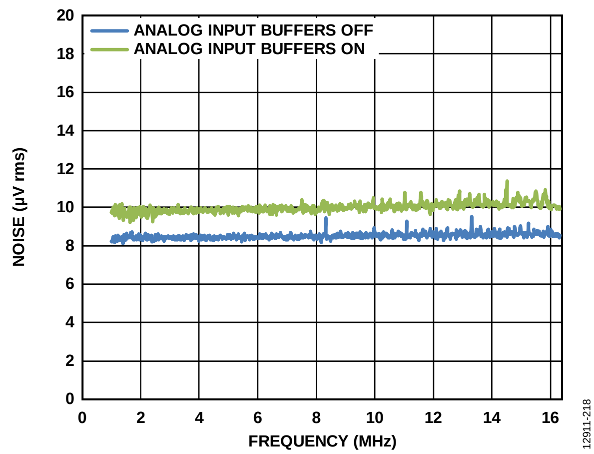


Figure 18. Noise vs. External Master Clock Frequency, Analog Input Buffers On and Off

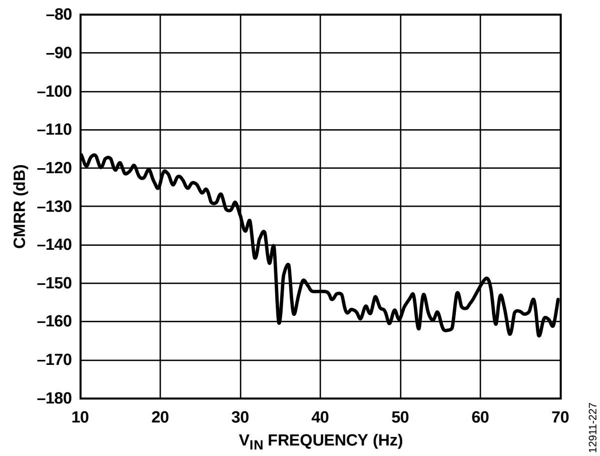


Figure 21. Common-Mode Rejection Ratio (CMRR) vs. V_{IN} Frequency (V_{IN} = 0.1 V, 10 Hz to 70 Hz, Output Data Rate = 20 SPS, Enhanced Filter)

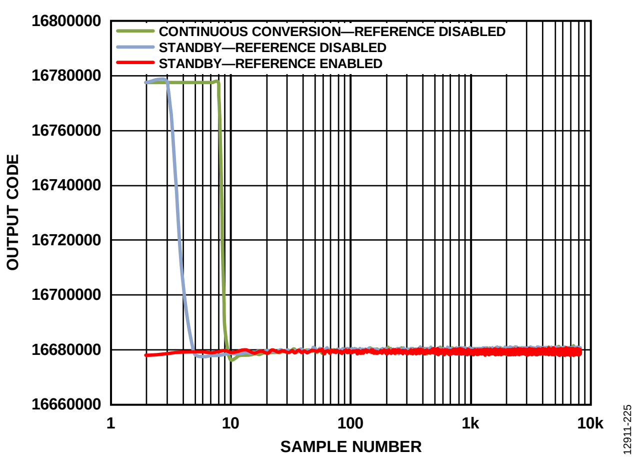


Figure 19. Internal Reference Settling Time

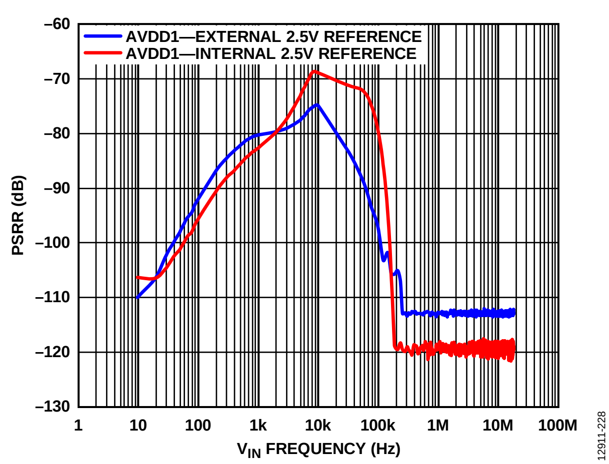


Figure 22. Power Supply Rejection Ratio (PSRR) vs. V_{IN} Frequency

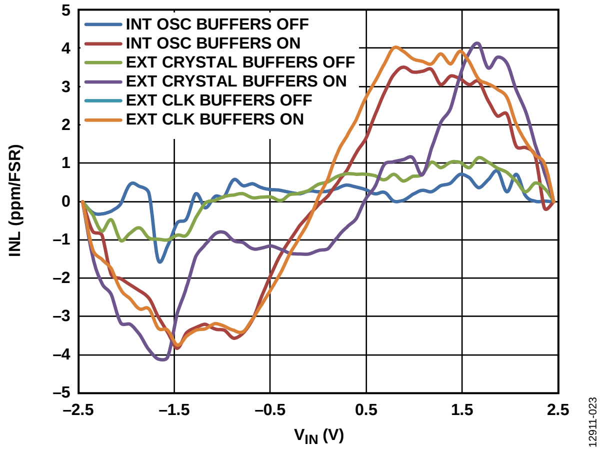


Figure 23. Integral Nonlinearity (INL) vs. V_{IN} (Differential Input, External 2.5 V Reference)

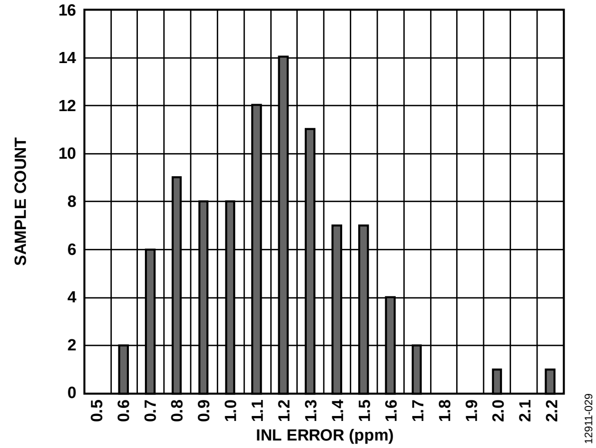


Figure 26. Integral Nonlinearity (INL) Distribution Histogram (All Input Buffers Disabled, Differential Input, V_{REF} = 5 V External, 92 Units)

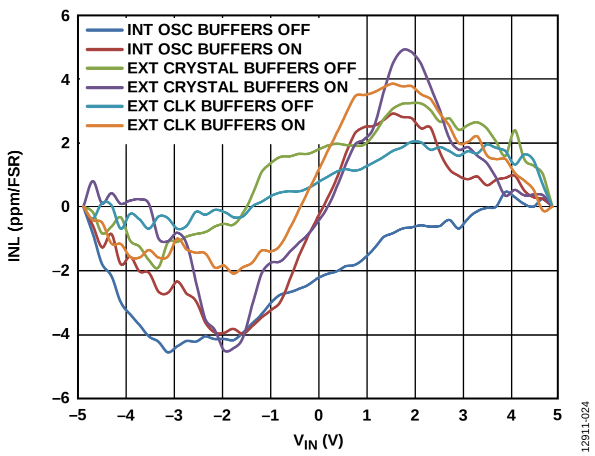


Figure 24. Integral Nonlinearity (INL) vs. V_{IN} (Differential Input, External 5 V Reference)

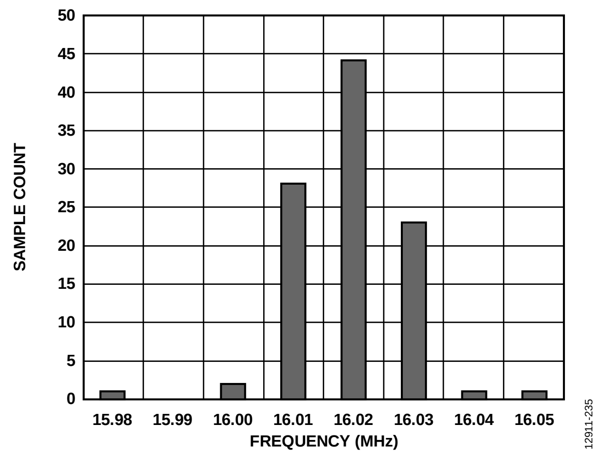


Figure 27. Internal Oscillator Frequency/Accuracy Distribution Histogram (100 Units)

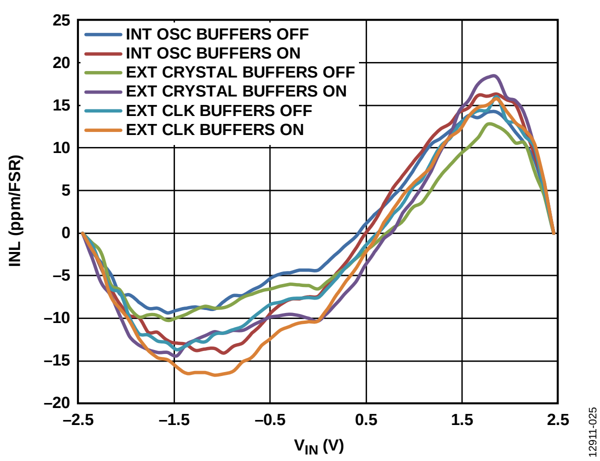


Figure 25. Integral Nonlinearity (INL) vs. V_{IN} (Differential Input, Internal 2.5 V Reference)

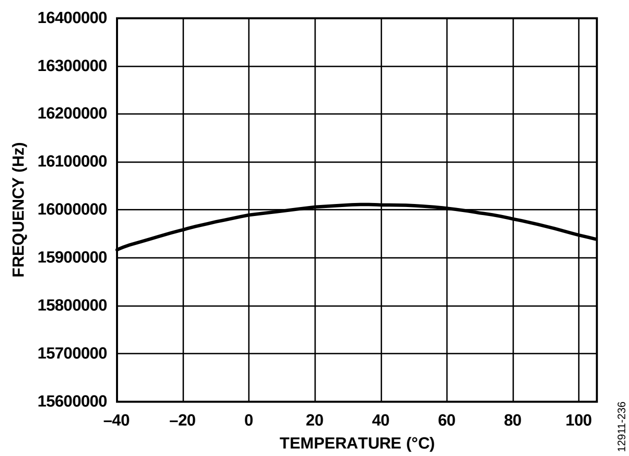


Figure 28. Internal Oscillator Frequency vs. Temperature

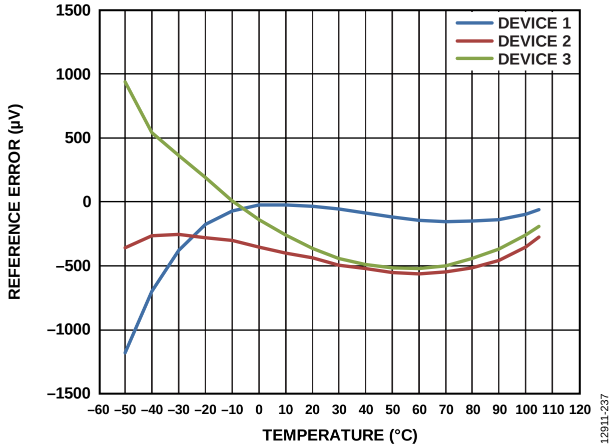


Figure 29. Absolute Reference Error vs. Temperature

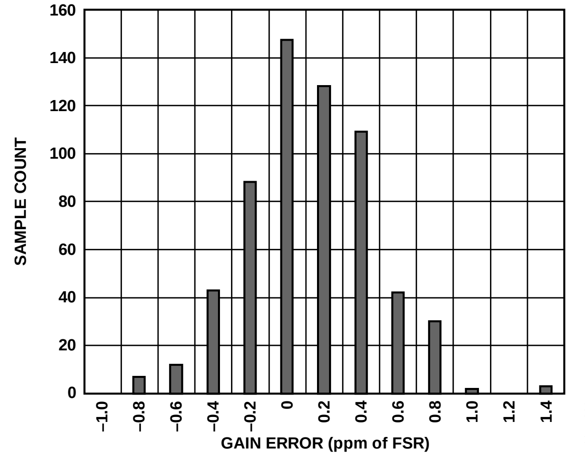


Figure 32. Gain Error Distribution Histogram (All Input Buffers Enabled, 611 Units)

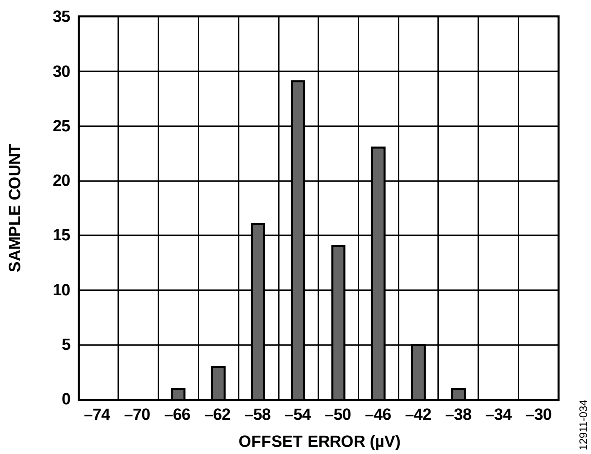


Figure 30. Offset Error Distribution Histogram (Internal Short, 92 Units)

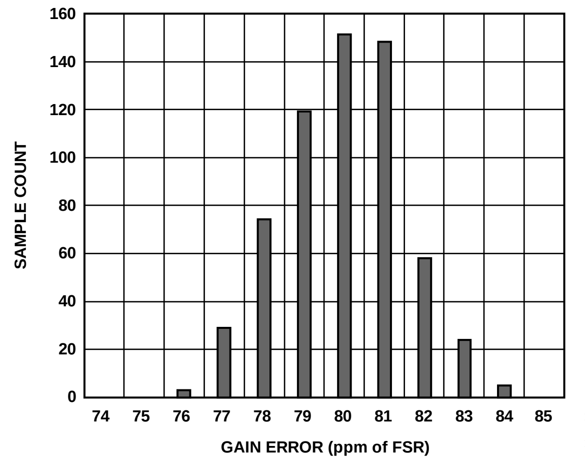


Figure 33. Gain Error Distribution Histogram (All Input Buffers Disabled, 647 Units)

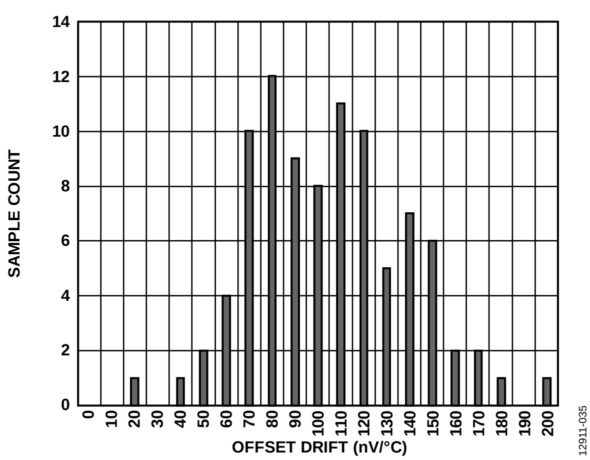


Figure 31. Offset Error Drift Distribution Histogram (Internal Short, 92 Units)

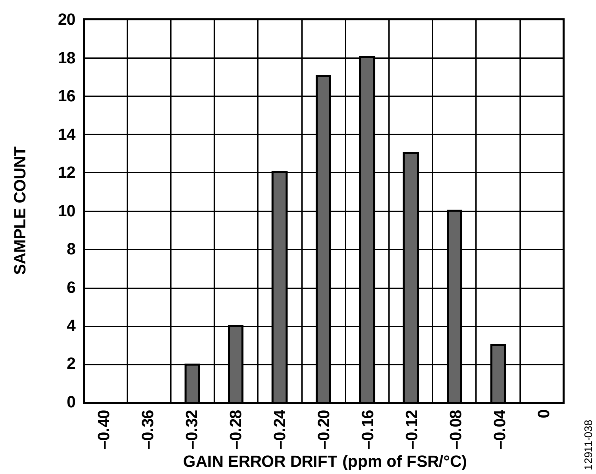


Figure 34. Gain Error Drift Distribution Histogram (All Input Buffers Enabled, 79 Units)

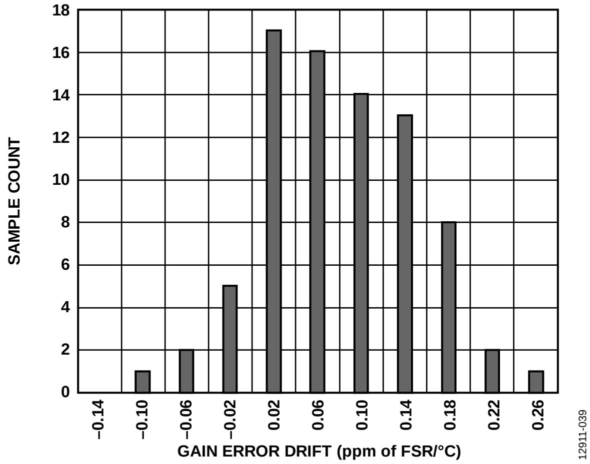


Figure 35. Gain Error Drift over Temperature Distribution Histogram (All Input Buffers Disabled, 79 Units)

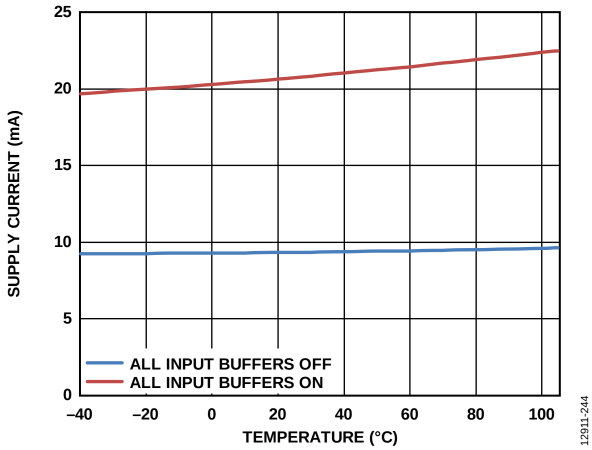


Figure 36. Supply Current vs. Temperature (Continuous Conversion Mode)

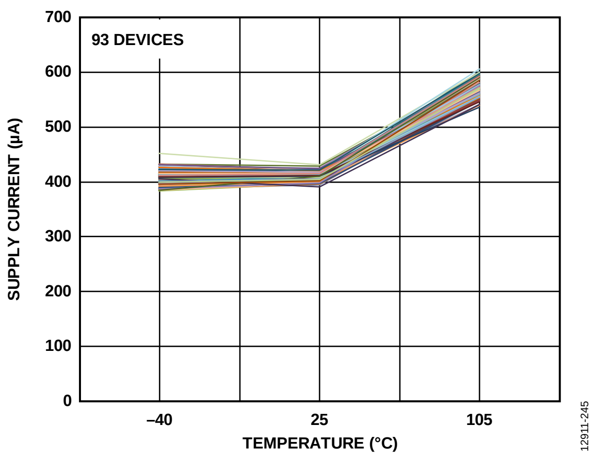


Figure 37. Supply Current vs. Temperature (Standby Mode with Reference Enabled)

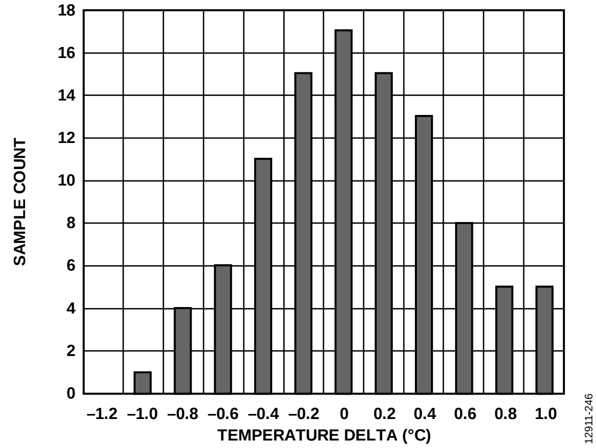


Figure 38. Temperature Sensor Distribution Histogram (Uncalibrated, 100 Units)

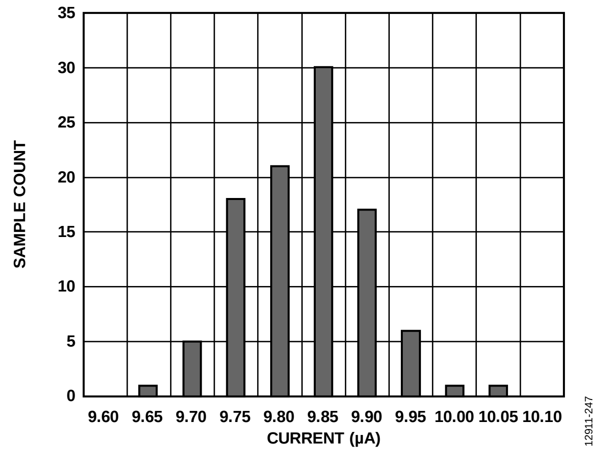


Figure 39. Burnout Current Distribution Histogram (100 Units)

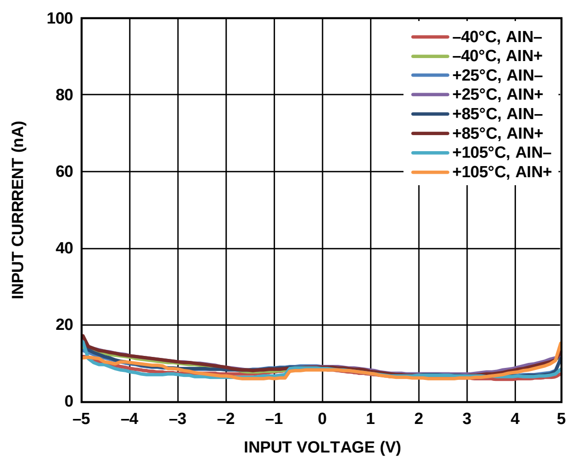


Figure 40. Analog Input Current vs. Input Voltage (V_{CM} = 2.5 V)

NOISE PERFORMANCE AND RESOLUTION

Table 6 and Table 7 show the rms noise, peak-to-peak noise, effective resolution, and the noise free (peak-to-peak) resolution of the AD7175-8 for various output data rates and filters. The numbers given are for the bipolar input range with an external 5 V reference. These numbers are typical and are generated with a differential input voltage of 0 V when the ADC is continuously converting on a single channel. It is important to note that the peak-to-peak resolution is calculated based on the peak-to-peak noise. The peak-to-peak resolution represents the resolution for which there is no code flicker.

Table 6. RMS Noise and Peak-to-Peak Resolution vs. Output Data Rate Using a Sinc5 + Sinc1 Filter (Default)[1]

Output Data Rate (SPS)	RMS Noise (µV rms)	Effective Resolution (Bits)	Peak-to-Peak Noise (µV p-p)	Peak-to-Peak Resolution (Bits)
Input Buffers Disabled				
250,000	8.7	20.1	65	17.2
62,500	5.5	20.8	43	17.8
10,000	2.5	21.9	18.3	19.1
1000	0.77	23.6	5.2	20.9
59.92	0.19	24	1.1	23.1
49.96	0.18	24	0.95	23.3
16.66	0.1	24	0.45	24
5	0.07	24	0.34	24
Input Buffers Enabled				
250,000	9.8	20	85	16.8
62,500	6.4	20.6	55	17.5
10,000	3	21.7	23	18.7
1000	0.92	23.4	5.7	20.7
59.98	0.23	24	1.2	23.0
49.96	0.2	24	1	23.3
16.66	0.13	24	0.66	23.9
5	0.07	24	0.32	24

[1] Selected rates only, 1000 samples.

Table 7. RMS Noise and Peak-to-Peak Resolution vs. Output Data Rate Using a Sinc3 Filter[1]

Output Data Rate (SPS)	RMS Noise (µV rms)	Effective Resolution (Bits)	Peak-to-Peak Noise (µV p-p)	Peak-to-Peak Resolution (Bits)
Input Buffers Disabled				
250,000	210	15.5	1600	12.6
62,500	5.2	20.9	40	17.9
10,000	1.8	22.4	14	19.4
1000	0.56	24	3.9	21.3
60	0.13	24	0.8	23.6
50	0.13	24	0.7	23.8
16.66	0.07	24	0.37	24
5	0.05	24	0.21	24
Input Buffers Enabled				
250,000	210	15.5	1600	12.6
62,500	5.8	20.7	48	17.7
10,000	2.1	22.2	16	19.3
1000	0.71	23.7	4.5	21.1
60	0.17	24	1.1	23.1
50	0.15	24	0.83	23.5
16.66	0.12	24	0.6	24
5	0.08	24	0.35	24

[1] Selected rates only, 1000 samples.

GETTING STARTED

The AD7175-8 offers the user a fast settling, high resolution, multiplexed ADC with high levels of configurability. The AD7175-8 includes the following features:

- Eight fully differential or 16 single-ended analog inputs.
- A crosspoint multiplexer selects any analog input combination as the input signals to be converted, routing it to the modulator positive or negative input.
- True rail-to-rail buffered analog and reference inputs.
- Fully differential input or single-ended input relative to any analog input.
- Per channel configurability—up to eight different setups can be defined. A separate setup can be mapped to each of the channels. Each setup allows the user to configure whether the buffers are enabled or disabled, gain and offset correction, filter type, output data rate, and reference source selection (internal/external).

The AD7175-8 includes a precision 2.5 V low drift (±2 ppm/°C) band gap internal reference. This reference can used for the ADC conversions, reducing the external component count. Alternatively, the reference can be output to the REFOUT pin to be used as a low noise biasing voltage for external circuitry. An example of this is using the REFOUT signal to set the input common mode for an external amplifier.

The AD7175-8 includes two separate linear regulator blocks for both the analog and digital circuitry. The analog LDO regulates the AVDD2 supply to 1.8 V, supplying the ADC core. The user can tie the AVDD1 and AVDD2 supplies together for the easiest connection. If there is already a clean analog supply rail in the system in the range of 2 V (minimum) to 5.5 V (maximum), the user can also choose to connect this to the AVDD2 input, allowing lower power dissipation.

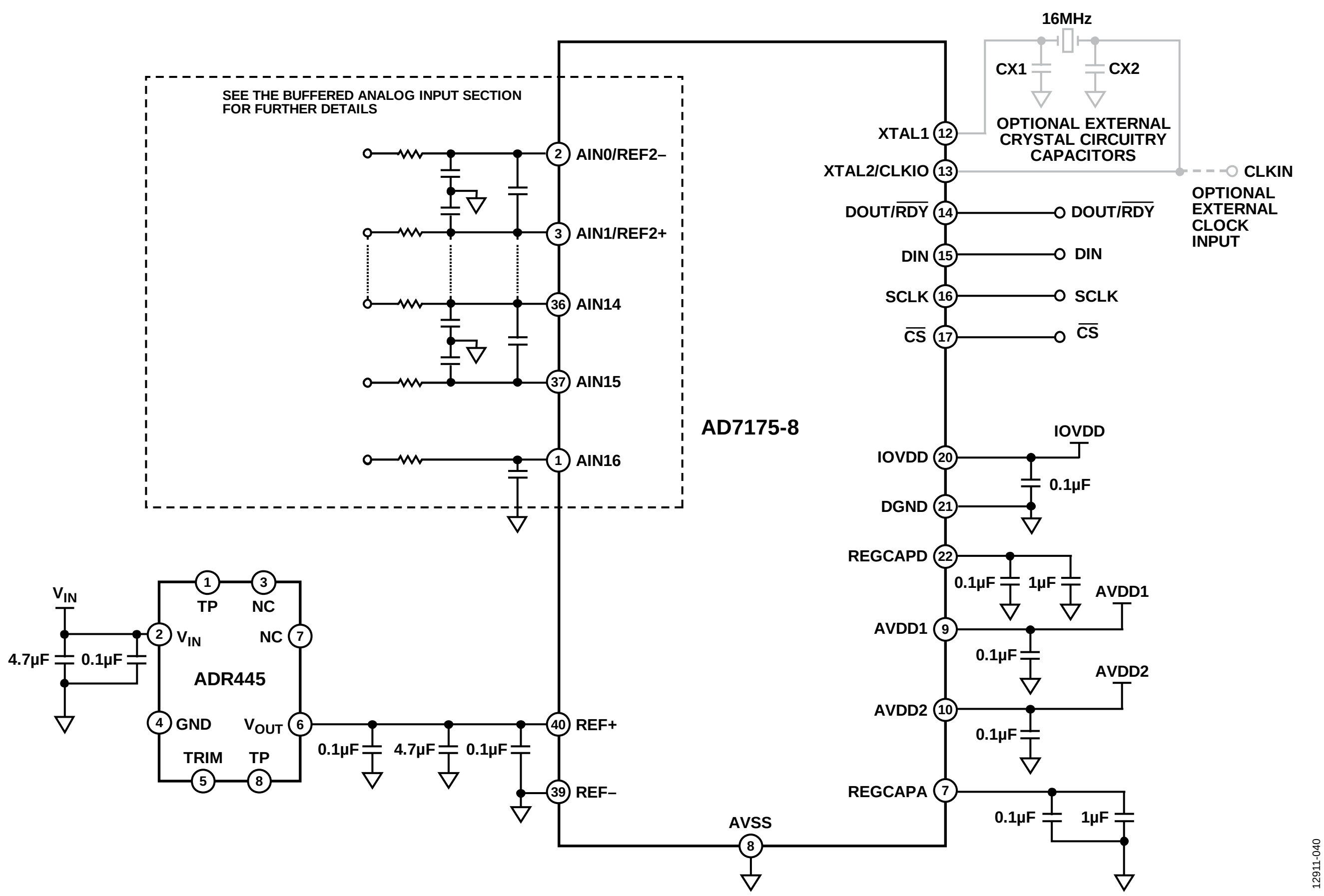


Figure 41. Typical Connection Diagram

The linear regulator for the digital IOVDD supply performs a similar function, regulating the input voltage applied at the IOVDD pin to 1.8 V for the internal digital filtering. The serial interface signals always operate from the IOVDD supply seen at the pin. This means that if 3.3 V is applied to the IOVDD pin, the interface logic inputs and outputs operate at this level.

The AD7175-8 can be used across a wide variety of applications, providing high resolution and accuracy. A sample of these scenarios is as follows:

- Fast scanning of analog input channels using the internal multiplexer
- Fast scanning of analog input channels using an external multiplexer with automatic control from the GPIOs.
- High resolution at lower speeds in either channel scanning or ADC per channel applications
- High resolution applications requiring a highly integrated solution to save printed circuit board (PCB) area

POWER SUPPLIES

The AD7175-8 has three independent power supplies: AVDD1, AVDD2, and IOVDD.

AVDD1 powers the crosspoint multiplexer and integrated analog and reference input buffers. AVDD1 is referenced to AVSS, and AVDD1 − AVSS = 5 V only. AVDD1 − AVSS can be a single 5 V supply or a ±2.5 V split supply. The split supply operation allows true bipolar inputs. When using split supplies, consider the absolute maximum ratings (see the Absolute Maximum Ratings section).

AVDD2 powers the internal 1.8 V analog LDO regulator. This regulator powers the ADC core. AVDD2 is referenced to AVSS, and AVDD2 − AVSS can range from 2 V (minimum) to 5.5 V (maximum).

IOVDD powers the internal 1.8 V digital LDO regulator. This regulator powers the digital logic of the ADC. IOVDD sets the voltage levels for the SPI interface of the ADC. IOVDD is referenced to DGND, and IOVDD − DGND can vary from 2 V (minimum) to 5.5 V (maximum).

There is no specific requirement for a power supply sequence on the AD7175-8. When all power supplies are stable, a device reset is required; see the AD7175-8 Reset section for details on how to reset the device.

DIGITAL COMMUNICATION

The AD7175-8 has a 3- or 4-wire SPI interface that is compatible with QSPI™, MICROWIRE®, and DSPs. The interface operates in SPI Mode 3 and can be operated with $\overline{\text{CS}}$ tied low. In SPI Mode 3, SCLK idles high, the falling edge of SCLK is the drive edge, and the rising edge of SCLK is the sample edge. This means that data is clocked out on the falling/drive edge and data is clocked in on the rising/sample edge.

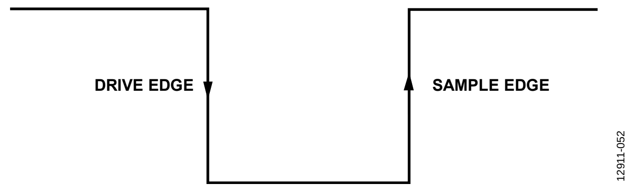


Figure 42. SPI Mode 3 SCLK Edges

Accessing the ADC Register Map

The communications register controls access to the full register map of the ADC. This register is an 8-bit write only register. On power-up or after a reset, the digital interface defaults to a state where it is expecting a write to the communications register; therefore, all communication begins by writing to the communications register.

The data written to the communications register determines which register is being accessed and if the next operation is a read or write. The register address bits (RA[5:0]) determine the specific register to which the read or write operation applies.

When the read or write operation to the selected register is complete, the interface returns to its default state, where it expects a write operation to the communications register.

Figure 43 and Figure 44 illustrate writing to and reading from a register by first writing the 8-bit command to the communications register, followed by the data for that register.

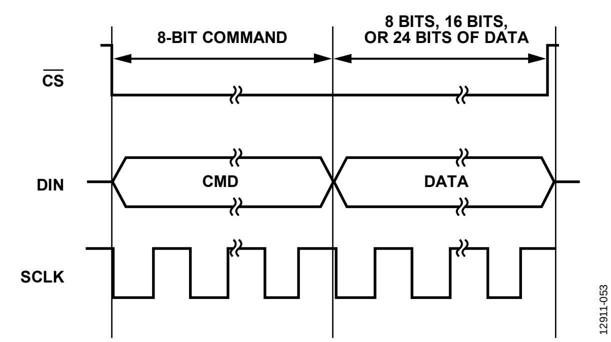


Figure 43. Writing to a Register
(8-Bit Command with Register Address Followed by Data of 8, 16, or 24 Bits; Data Length on DIN Is Dependent on the Register Selected)

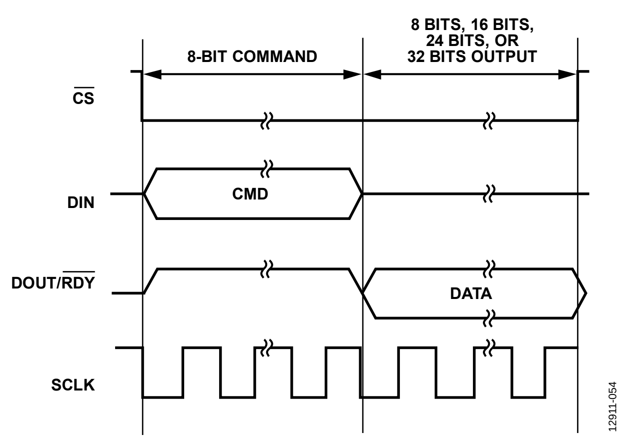


Figure 44. Reading from a Register
(8-Bit Command with Register Address Followed by Data of 8, 16, or 24 Bits; Data Length on DOUT Is Dependent on the Register Selected)

Reading the ID register is the recommended method for verifying correct communication with the device. The ID register is a read only register and contains the value 0x3CDx for the AD7175-8. The communications register and the ID register details are described in Table 8 and Table 9, respectively.

AD7175-8 RESET

In situations where interface synchronization is lost, a write operation of at least 64 serial clock cycles with DIN high returns the ADC to its default state by resetting the entire device, including the register contents. Alternatively, if $\overline{CS}$ is being used with the digital interface, returning $\overline{CS}$ high sets the digital interface to its default state and halts any serial interface operation.

CONFIGURATION OVERVIEW

After power-on or reset, the AD7175-8 default configuration are as follows. Note that only a few of the register setting options are shown; this list is just an example. For full register information, see the Register Details section.

- Channel configuration. CH0 is enabled, AIN0 is selected as the positive input, and AIN1 is selected as the negative input. Setup 0 is selected.
- Setup configuration. The internal reference and the analog input buffers are enabled. The reference input buffers are disabled.
- Filter configuration. The sinc5 + sinc 1 filter is selected and the maximum output data rate is selected.
- ADC mode. Continuous conversion mode and the internal oscillator are enabled.
- Interface mode. CRC and the data + status output are disabled.

Figure 45 shows an overview of the suggested flow for changing the ADC configuration, divided into the following three blocks:

- Channel configuration (see Box A in Figure 45)
- Setup configuration (see Box B in Figure 45)
- ADC mode and interface mode configuration (see Box C in Figure 45)

Channel Configuration

The AD7175-8 has 16 independent channels and 8 independent setups. The user can select any of the analog input pairs on any channel, as well as any of the eight setups for any channel, giving the user full flexibility in the channel configuration. This also allows per channel configuration for up to eight channels when using differential inputs or single-ended inputs. Channel configuration can be shared across multiple channels.

Channel Registers

The channel registers are used to select which of the 17 analog input pins (AIN0 to AIN16) are used as either the positive analog input (AIN+) or the negative analog input (AIN−) for that channel. This register also contains a channel enable/disable bit and the setup selection bits, which are used to select from the eight available setups for this channel.

When the AD7175-8 is operating with more than one channel enabled, the channel sequencer cycles through the enabled channels in sequential order, from Channel 0 to Channel 15. If a channel is disabled, it is skipped by the sequencer. Details of the channel register for Channel 0 are shown in Table 10.

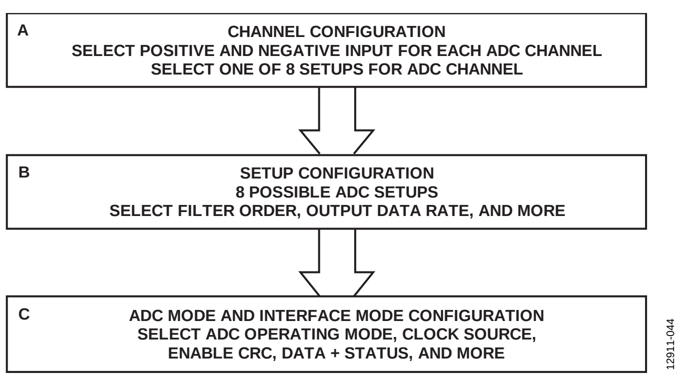


Figure 45. Suggested ADC Configuration Flow

Table 8. Communications Register

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x00	COMMS	[7:0]	$\overline{WEN}$	R/$\overline{W}$	RA						0x00	W

Table 9. ID Register

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x07	ID	[15:8]	ID[15:8]								0x3CDx	R
		[7:0]	ID[7:0]									

Table 10. Channel 0 Register

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x10	CH0	[15:8]	CH_EN0	Reserved	SETUP_SEL[2:0]		Reserved		AINPOS0[4:3]		0x8001	RW
		[7:0]	AINPOS0[2:0]			AINNEG0						

ADC Setups

The AD7175-8 has eight independent setups. Each setup consists of the following four registers:

- Setup configuration register
- Filter configuration register
- Gain register
- Offset register

For example, Setup 0 consists of Setup Configuration Register 0, Filter Configuration Register 0, Gain Register 0, and Offset Register 0. Figure 46 shows the grouping of these registers. The setup is selectable from the channel registers (see the Channel Configuration section), which allows each channel to be assigned to one of eight separate setups. Table 11 through Table 14 show the four registers associated with Setup 0. This structure is repeated for Setup 1 to Setup 3.

Setup Configuration Registers

The setup configuration registers allow the user to select the output coding of the ADC by selecting between bipolar mode and unipolar mode. In bipolar mode, the ADC accepts negative differential input voltages, and the output coding is offset binary. In unipolar mode, the ADC accepts only positive differential voltages, and the coding is straight binary. In either case, the input voltage must be within the AVDD1/ AVSS supply voltages. The user can select the reference source using these registers. Three options are available: an internal 2.5 V reference, an external reference connected between the REF+ and REF− pins, or AVDD1 − AVSS. The analog input and reference input buffers can also be enabled or disabled using this register.

Filter Configuration Registers

The filter configuration registers select which digital filter is used at the output of the ADC modulator. The order of the filter and the output data rate is selected by setting the bits in this register. For more information, see the Digital Filters section.

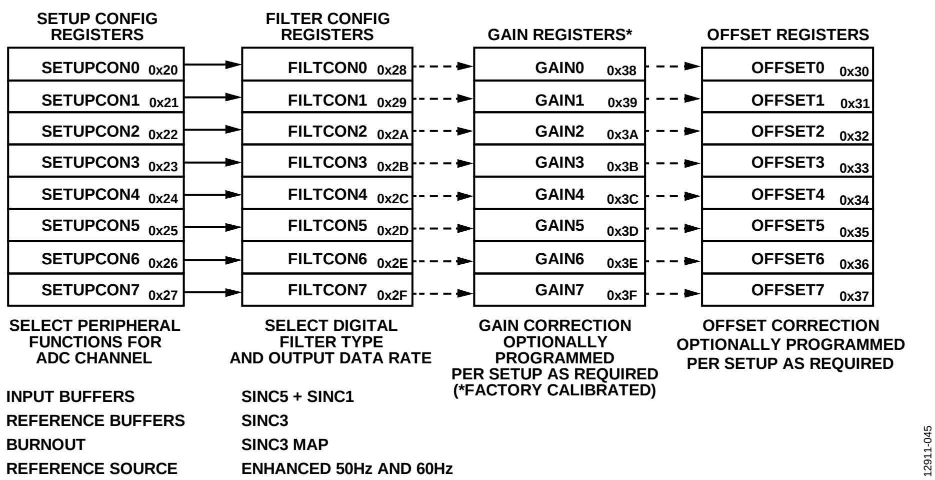


Figure 46. ADC Setup Register Grouping

Table 11. Setup Configuration 0 Register

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x20	SETUPCON0	[15:8]	Reserved			BI_UNIPOLAR0	REFBUF0+	REFBUF0−	AINBUF0+	AINBUF0−	0x1320	RW
		[7:0]	BURNOUT_EN0	Reserved	REF_SEL0		Reserved					

Table 12. Filter Configuration 0 Register

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x28	FILTCON0	[15:8]	SINC3_MAP0	Reserved			ENHFILTEN0	ENHFILT0			0x0500	RW
		[7:0]	Reserved	ORDER0		ODR0						

Table 13. Gain Configuration 0 Register

Reg.	Name	Bits	Bit[23:0]	Reset	RW
0x38	GAIN0	[23:0]	GAIN0[23:0]	0x5XXXX0	RW

Table 14. Offset Configuration 0 Register

Reg.	Name	Bits	Bit[23:0]	Reset	RW
0x30	OFFSET0	[23:0]	OFFSET0[23:0]	0x800000	RW

Gain Registers

The gain registers are 24-bit registers that hold the gain calibration coefficient for the ADC. The gain registers are read/write registers. These registers are configured at power-on with factory calibrated coefficients. Therefore, every device has different default coefficients. The default value is automatically overwritten if a system full-scale calibration is initiated by the user or if the gain register is written to by the user. For more information on calibration, see the Operating Modes section.

Offset Registers

The offset registers hold the offset calibration coefficient for the ADC. The power-on reset value of the offset registers is 0x800000. The offset registers are 24-bit read/write registers. The power-on reset value is automatically overwritten if an internal or system zero-scale calibration is initiated by the user or if the offset registers are written to by the user.

ADC Mode and Interface Mode Configuration

The ADC mode register and the interface mode register configure the core peripherals for use by the AD7175-8 and the mode for the digital interface.

ADC Mode Register

The ADC mode register primarily sets the conversion mode of the ADC to either continuous or single conversion. The user can also select the standby and power-down modes, as well as any of the calibration modes. In addition, this register contains the clock source select bits and the internal reference enable bits. The reference select bits are contained in the setup configuration registers (see the ADC Setups section for more information).

Interface Mode Register

The interface mode register configures the digital interface operation. This register allows the user to control data-word length, CRC enable, data + status read, and continuous read mode. The details of the ADC mode and interface mode registers are shown in Table 15 and Table 16, respectively. For more information, see the Digital Interface section.

Table 15. ADC Mode Register

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x01	ADCMODE	[15:8]	REF_EN	HIDE_DELAY	SING_CYC	Reserved		Delay			0xA000	RW
		[7:0]	Reserved	Mode			CLOCKSEL		Reserved			

Table 16. Interface Mode Register

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x02	IFMODE	[15:8]	Reserved			ALT_SYNC	IOSTRENGTH	Reserved		DOUT_RESET	0x0000	RW
		[7:0]	CONTREAD	DATA_STAT	REG_CHECK	Reserved	CRC_EN		Reserved	WL16		

Understanding Configuration Flexibility

The most straightforward implementation of the AD7175-8 is to use eight differential inputs with adjacent analog inputs and run all of them with the same setup, gain correction, and offset correction register. In this case, the user selects the following differential inputs: AIN0/AIN1, AIN2/AIN3, AIN4/AIN5, AIN6/AIN7, AIN8/AIN9, AIN10/AIN11, AIN12/AIN13, and AIN14/AIN15. In Figure 47, the registers shown in black font must be programmed for such a configuration. The registers shown in gray font are redundant in this configuration.

Programming the gain and offset registers is optional for any use case, as indicated by the dashed lines between the register blocks.

An alternative way to implement these eight fully differential inputs is by taking advantage of the eight available setups. Motivation for doing this includes having a different speed/noise requirement on some of the eight differential inputs vs. other inputs, or there may be a specific offset or gain correction for particular channels. Figure 48 shows how each of the differential inputs may use a separate setup, allowing full flexibility in the configuration of each channel.

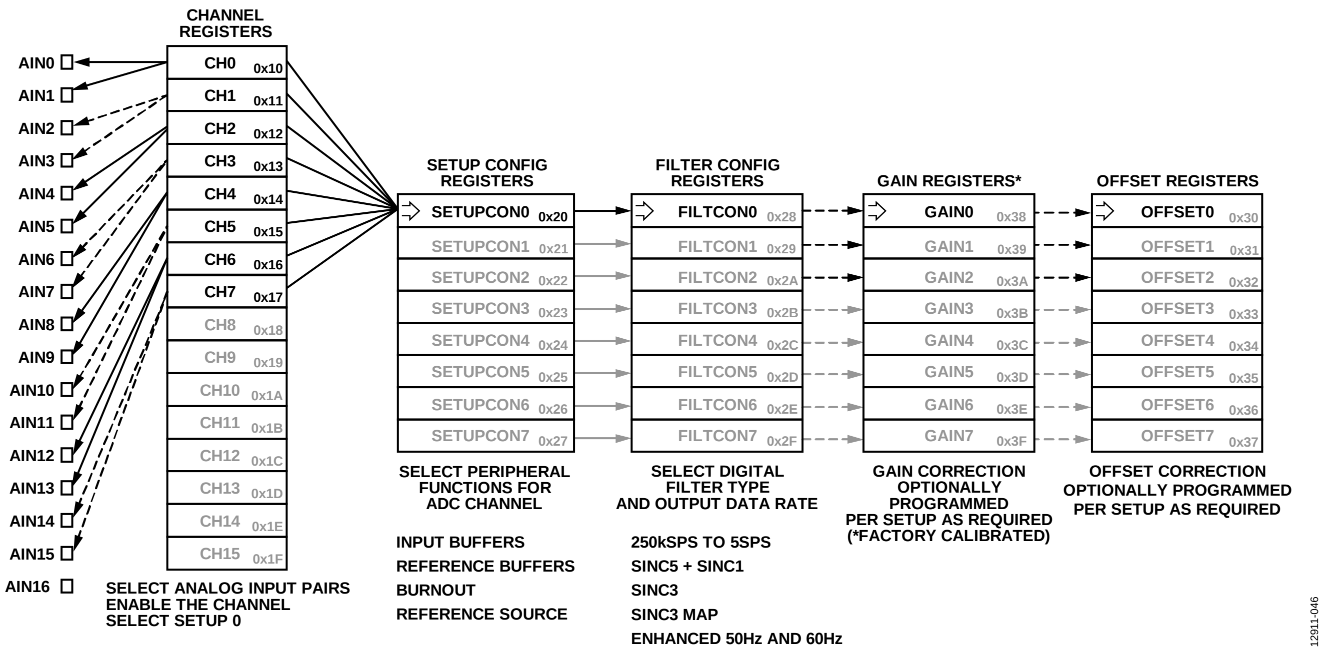


Figure 47. Eight Fully Differential Inputs, All Using a Single Setup (SETUPCON0; FILTCON0; GAIN0; OFFSET0)

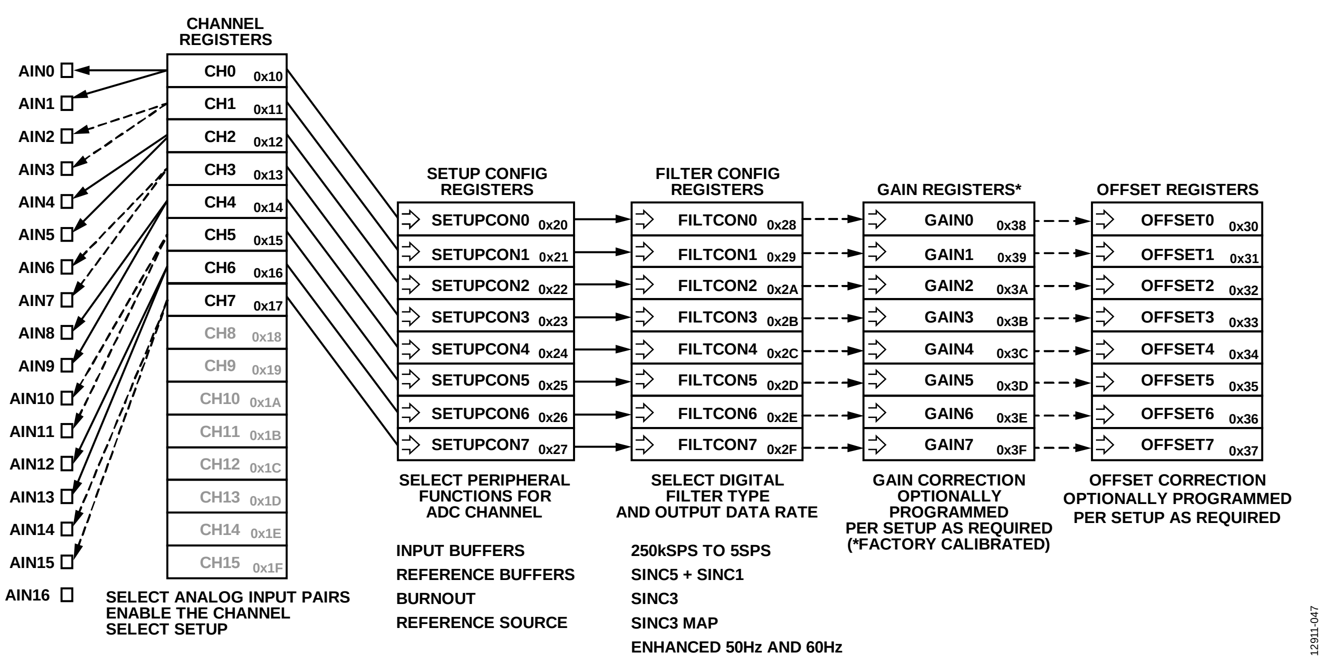


Figure 48. Eight Fully Differential Inputs with a Setup per Channel

Figure 49 shows an example of how the channel registers span between the analog input pins and the setup configurations downstream. In this random example, seven differential inputs and two single-ended inputs are required. The single-ended inputs are the AIN8/AIN16 and AIN15/AIN16 combinations. The first five differential input pairs (AIN0/AIN1, AIN2/AIN3, AIN4/AIN5, AIN6/AIN7, and AIN9/AIN10) use the same setup: SETUPCON0. The two single-ended input pairs (AIN8/AIN16 and AIN15/ AIN16) are set up as a diagnostics; therefore, use a separate setup: SETUPCON1. The final two differential inputs (AIN11/AIN12 and AIN13/AIN14) also use a separate setup: SETUPCON2. Given that three setups are selected for use, the SETUPCON0, SETUPCON1, and SETUPCON2 registers are programmed as required, and the FILTCON0, FILTCON1, and FILTCON2 registers are also programmed as required. Optional gain and offset correction can be employed on a per setup basis by programming the GAIN0, GAIN1, and GAIN2 registers and the OFFSET0, OFFSET1, and OFFSET2 registers.

In the example shown in Figure 49, the CH0 to CH8 registers are used. Setting the MSB in each of these registers, the CH_EN0 to CH_EN8 bits, enables the nine combinations via the crosspoint multiplexer. When the AD7175-8 converts, the sequencer transitions in ascending sequential order from CH0 to CH1 to CH2, and then on to CH8 before looping back to CH0 to repeat the sequence.

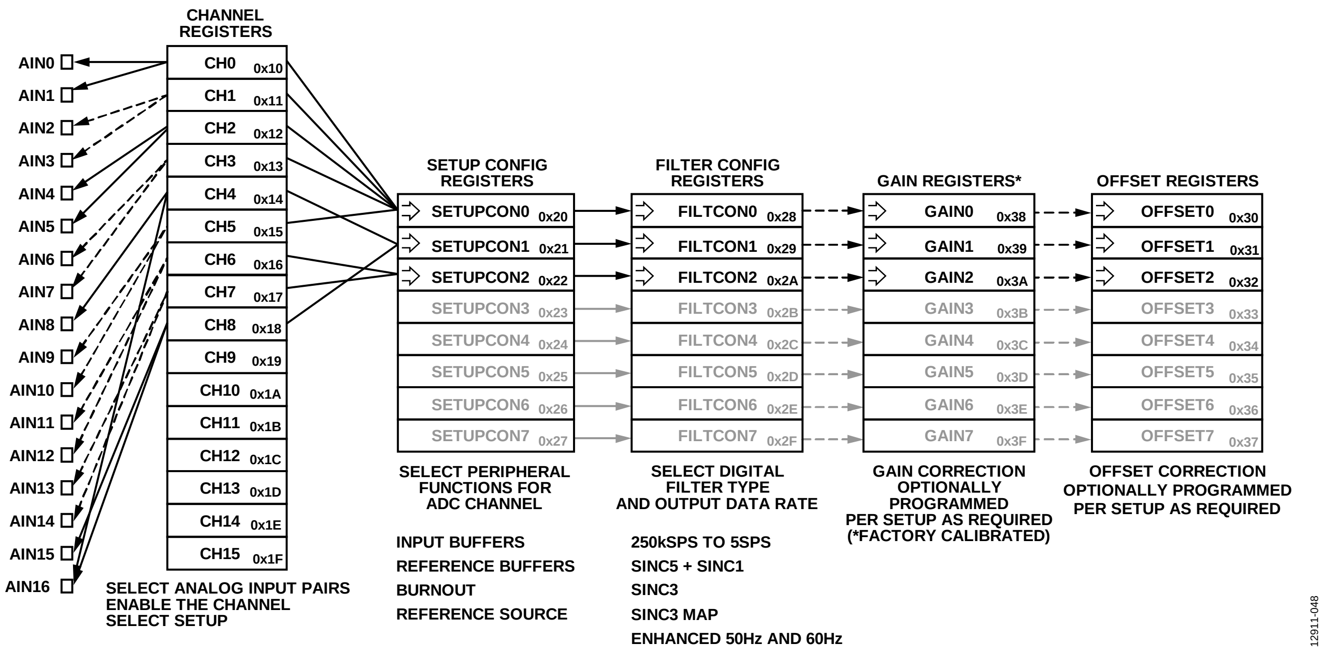


Figure 49. Mixed Differential and Single-Ended Configuration Using Multiple Shared Setups

CIRCUIT DESCRIPTION

BUFFERED ANALOG INPUT

The AD7175-8 has true rail-to-rail, integrated, precision unity-gain buffers on both ADC analog inputs. The buffers provide the benefit of giving the user high input impedance with only ±30 nA typical input current, allowing high impedance sources to be connected directly to the analog inputs. The buffers fully drive the internal ADC switch capacitor sampling network, simplifying the analog front-end circuit requirements while consuming a very efficient 2.9 mA typical per buffer. Each analog input buffer amplifier is fully chopped, meaning that it minimizes the offset error drift and 1/f noise of the buffer. The 1/f noise profile of the ADC and buffer combined is shown in Figure 50.

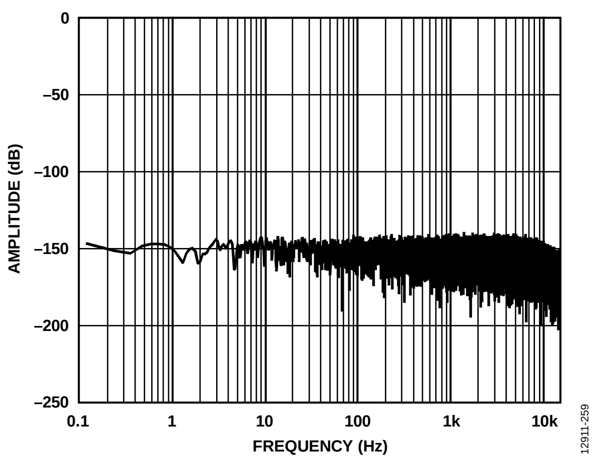


Figure 50. Shorted Input FFT (Analog Input Buffers Enabled)

The analog input buffers do not suffer from linearity degradation when operating at the rails, unlike many discrete amplifiers. When operating at or close to the AVDD1 and AVSS supply rails, there is an increase in input current. This increase is most notable at higher temperatures. Figure 40 shows the analog input current for various conditions. With the analog input buffers disabled, the average input current to the AD7175-8 changes linearly with the differential input voltage at a rate of ±48 μA/V.

CROSSPOINT MULTIPLEXER

There are 17 analog input pins: AIN0 to AIN16. Each of these pins connects to the internal crosspoint multiplexer. The crosspoint multiplexer enables any of these inputs to be configured as an input pair, either single-ended or fully differential. The AD7175-8 can have up to 16 active channels. When more than one channel is enabled, the channels are automatically sequenced in order from the lowest enabled channel number to the highest enabled channel number. The output of the multiplexer is connected to the input of the integrated true rail-to-rail buffers. These can be bypassed and the multiplexer output can be directly connected to the switched-capacitor input of the ADC. The simplified analog input circuit is shown in Figure 51.

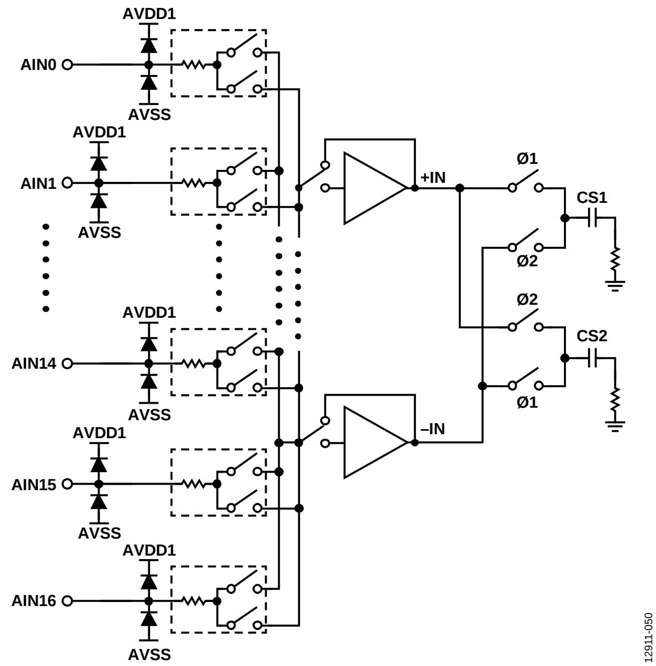


Figure 51. Simplified Analog Input Circuit

The CS1 and CS2 capacitors each have a magnitude in the order of a number of picofarads. This capacitance is the combination of both the sampling capacitance and the parasitic capacitance.

Fully Differential Inputs

Because the AIN0 to AIN16 analog inputs are connected to a crosspoint multiplexer, any combination of signals can be used to create an analog input pair. This crosspoint multiplexer allows the user to select eight fully differential inputs or 16 single-ended inputs.

If eight fully differential input paths are connected to the AD7175-8, using adjacent analog input pins such as AIN0/AIN1 for the differential input pair is recommended. This is due to the relative locations of these pins to each other. Decouple all analog inputs to AVSS.

Single-Ended Inputs

The user can also choose to measure 16 different single-ended analog inputs. In this case, each of the analog inputs is converted as the difference between the single-ended input to be measured and a set analog input common pin. Because there is a crosspoint multiplexer, the user can set any of the analog inputs as the common pin. An example of such a scenario is to connect the AIN8 pin to AVSS or to the REFOUT voltage (that is, AVSS + 2.5 V) and select this input when configuring the crosspoint multiplexer. When using the AD7175-8 with single-ended inputs.

AD7175-8 REFERENCE

The AD7175-8 offers the user the option of either supplying an external reference to the REF+ and REF− or REF2+ and REF2- pins of the device or allowing the use of the internal 2.5 V, low noise, low drift reference. Select the reference source to be used by the analog input by setting the REF_SELx bits (Bits[5:4]) in the setup configuration registers appropriately. The structure of the Setup Configuration 0 register is shown in Table 17. The AD7175-8 defaults on power-up to use the internal 2.5 V reference.

External Reference

The AD7175-8 has a fully differential reference input applied through the REF+ and REF− or REF2+ and REF2 pins. Standard low noise, low drift voltage references, such as the ADR445, ADR444, and ADR441, are recommended for use. Apply the external reference to the AD7175-8 reference pins as shown in Figure 52. Decouple the output of any external reference to AVSS. As shown in Figure 52, the ADR445 output is decoupled with a 0.1 µF capacitor at its output for stability purposes. The output is then connected to a 4.7 µF capacitor, which acts as a reservoir for any dynamic charge required by the ADC, and followed by a 0.1 µF decoupling capacitor at the REF+ or REF2+ input. This capacitor is placed as close as possible to the REF+/REF2+ and REF−/REF2− pins. The REF−/REF2− pin is connected directly to the AVSS potential. On power-up of the AD7175-8, the internal reference is enabled by default and is output on the REFOUT pin. When an external reference is used instead of the internal reference to supply the AD7175-8, attention must be paid to the output of the REFOUT pin. If the internal reference is not being used elsewhere in the application, ensure that the REFOUT pin is not hardwired to AVSS because this draws a large current on power-up. On power-up, if the internal reference is not being used, write to the ADC mode register, disabling the internal reference. This is controlled by the REF_EN bit (Bit 15) in the ADC mode register, which is shown in Table 18.

Internal Reference

The AD7175-8 includes its own low noise, low drift voltage reference. The internal reference has a 2.5 V output. The internal reference is output on the REFOUT pin after the REF_EN bit in the ADC mode register is set and is decoupled to AVSS with a 0.1 µF capacitor. The AD7175-8 internal reference is enabled by default on power-up and is selected as the reference source for the ADC. When using the internal reference, the INL performance degrades as shown in Figure 23.

The REFOUT signal is buffered before being output to the pin. The signal can be used externally in the circuit as a common-mode source for external amplifier configurations.

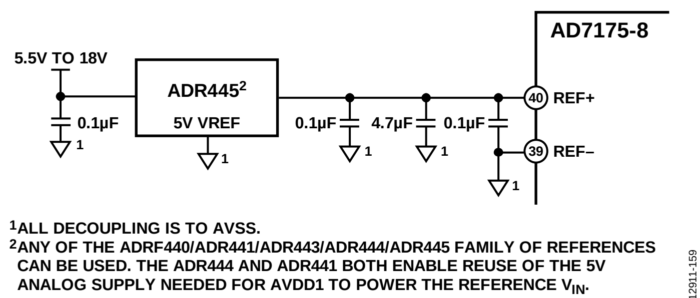


Figure 52. External Reference ADR445 Connected to the AD7175-8 Reference Pins

Table 17. Setup Configuration 0 Register

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x20	SETUPCON0	[15:8]	Reserved			BI_UNIPOLAR0	REFBUF0+	REFBUF0−	AINBUF0+	AINBUF0−	0x1320	RW
		[7:0]	BURNOUT_EN0	Reserved	REF_SEL0		Reserved					

Table 18. ADC Mode Register

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x01	ADCMODE	[15:8]	REF_EN	HIDE_DELAY	SING_CYC	Reserved		Delay			0xA000	RW
		[7:0]	Reserved	Mode			CLOCKSEL		Reserved			

BUFFERED REFERENCE INPUT

The AD7175-8 has true rail-to-rail, integrated, precision unity gain buffers on both ADC reference inputs. The buffers provide the benefit of giving the user high input impedance and allow high impedance external sources to be directly connected to the reference inputs. The integrated reference buffers can fully drive the internal reference switch capacitor sampling network, simplifying the reference circuit requirements while consuming a very efficient 2.9 mA typical per buffer. Each reference input buffer amplifier is fully chopped, meaning that it minimizes the offset error drift and 1/f noise of the buffer. When using an external reference, such as the ADR445, ADR444, and ADR441, these buffers are not required because these references, with proper decoupling, can drive the reference inputs directly.

CLOCK SOURCE

The AD7175-8 uses a nominal master clock of 16 MHz. The AD7175-8 sources its sampling clock from one of three sources:

- Internal oscillator
- External crystal
- External clock source

All output data rates listed in the data sheet relate to a master clock rate of 16 MHz. Using a lower clock frequency from, for instance, an external source scales any listed data rate proportionally. To achieve the specified data rates, particularly rates for the rejection of 50 Hz and 60 Hz, use a 16 MHz clock. The source of the master clock is selected by setting the CLOCKSEL bits (Bits[3:2]) in the ADC mode register as shown in Table 18. The default operation on power-up and reset of the AD7175-8 is to operate with the internal oscillator. It is possible to fine tune the output data rate and filter notch at low output data rates using the SINC3_MAPx bit. See the Sinc3 Filter section for more information.

Internal Oscillator

The internal oscillator runs at 16 MHz and can be used as the ADC master clock. It is the default clock source for the AD7175-8 and is specified with an accuracy of ±2.5%.

There is an option to allow the internal clock oscillator to be output on the XTAL2/CLKIO pin. The clock output is driven to the IOVDD logic level. Use of this option can affect the dc performance of the AD7175-8 due to the disturbance introduced by the output driver. The extent to which the performance is affected depends on the IOVDD voltage supply. Higher IOVDD voltages create a wider logic output swing from the driver and affect performance to a greater extent. This effect is further exaggerated if the IOSTRENGTH bit is set at higher IOVDD levels (see Table 28 for more information).

External Crystal

If higher precision, lower jitter clock sources are required, the AD7175-8 can use an external crystal to generate the master clock. The crystal is connected to the XTAL1 and XTAL2/CLKIO pins. A recommended crystal for use is the FA-20H—a 16 MHz, 10 ppm, 9 pF crystal from Epson-Toyocom—which is available in a surface-mount package. As shown in Figure 53, insert two capacitors from the traces connecting the crystal to the XTAL1 and XTAL2/CLKIO pins. These capacitors allow for circuit tuning. Connect these capacitors to the DGND pin. The value for these capacitors depends on the length and capacitance of the trace connections between the crystal and the XTAL1 and XTAL2/CLKIO pins. Therefore, the values of these capacitors differ depending on the PCB layout and the crystal employed.

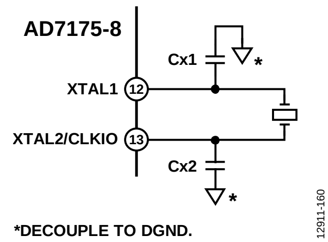


Figure 53. External Crystal Connections

The external crystal circuitry can be sensitive to the SCLK edges, depending on SCLK frequency, IOVDD voltage, crystal circuitry layout, and the crystal used. During crystal startup, any disturbances caused by the SLCK edges may cause double edges on the crystal input, resulting in invalid conversions until the crystal voltage has reached a high enough level such that any interference from the SCLK edges is insufficient to cause double clocking. This double clocking can be avoided by ensuring that the crystal circuitry has reached a sufficient voltage level after startup before applying any SCLK signal.

Due to the nature of the crystal circuitry, it is recommended that empirical testing of the circuit be performed under the required conditions, with the final PCB layout and crystal, to ensure correct operation.

External Clock

The AD7175-8 can also use an externally supplied clock. In systems where this is desirable, the external clock is routed to the XTAL2/CLKIO pin. In this configuration, the XTAL2/CLKIO pin accepts the externally sourced clock and routes it to the modulator. The logic level of this clock input is defined by the voltage applied to the IOVDD pin.

DIGITAL FILTERS

The AD7175-8 has three flexible filter options to allow optimization of noise, settling time, and rejection.

- Sinc5 + sinc1 filter
- Sinc3 filter
- Enhanced 50 Hz and 60 Hz rejection filters

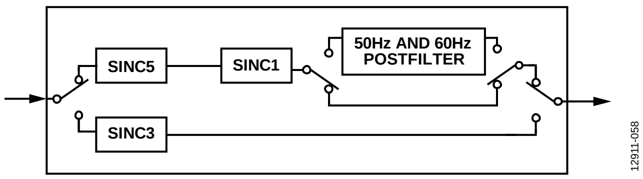


Figure 54. Digital Filter Block Diagram

The filter and output data rate are configured by setting the appropriate bits in the filter configuration register for the selected setup. Each channel can use a different setup and therefore, a different filter and output data rate. See the Register Details section for more information.

SINC5 + SINC1 FILTER

The sinc5 + sinc1 filter is targeted at multiplexed applications and achieves single cycle settling at output data rates of 10 kSPS and lower. The sinc5 block output is fixed at the maximum rate of 250 kSPS, and the sinc1 block output data rate can be varied to control the final ADC output data rate. Figure 55 shows the frequency domain response of the sinc5 + sinc1 filter at a 50 SPS ODR. The sinc5 + sinc1 filter has a slow roll-off over frequency and narrow notches.

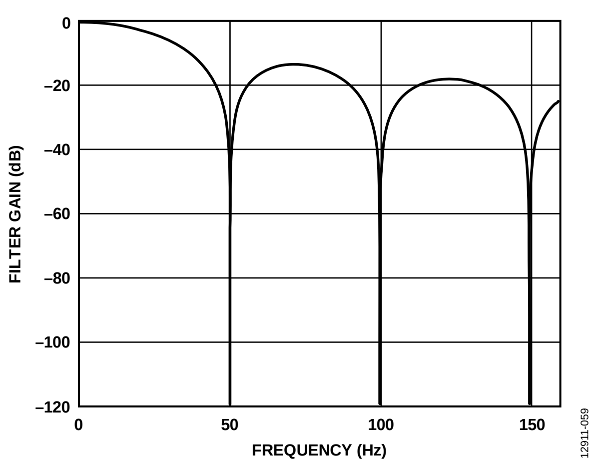


Figure 55. Sinc5 + Sinc1 Filter Response at 50 SPS ODR

The ODRs with the accompanying settling time and rms noise for the sinc5 + sinc1 filter are shown in Table 19 and Table 20.

SINC3 FILTER

The sinc3 filter achieves the best single-channel noise performance at lower rates and is, therefore, most suitable for single-channel applications. The sinc3 filter always has a settling time, t_{SETTLE}, equal to

$$t_{SETTLE} = 3/Output\ Data\ Rate$$

Figure 56 shows the frequency domain filter response for the sinc3 filter. The sinc3 filter has good roll-off over frequency and has wide notches for good notch frequency rejection.

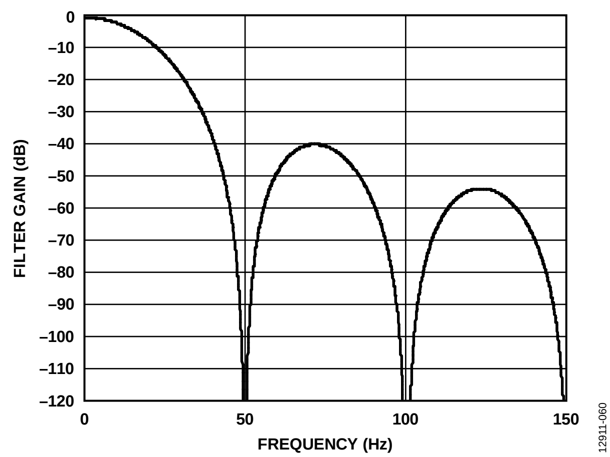


Figure 56. Sinc3 Filter Response

The ODRs with the accompanying settling time and rms noise for the sinc3 filter are shown in Table 21 and Table 22. It is possible to finely tune the output data rate for the sinc3 filter by setting the SINC3_MAPx bits in the filter configuration registers. If this bit is set, the mapping of the filter register changes to directly program the decimation rate of the sinc3 filter. All other options are eliminated. The data rate when on a single channel can be calculated using the following equation:

$$Output\ Data\ Rate = \frac{f_{MOD}}{32 \times FILTCONx[14{:}0]}$$

where:
f_{MOD} is the modulator rate (MCLK/2) and is 8 MHz for a 16 MHz MCLK.
FILTCONx[14:0] are the contents on the filter configuration registers excluding the MSB.

For example, an output data rate of 50 SPS can be achieved with SINC3_MAPx enabled by setting the FILTCONx[14:0] bits to a value of 5000.

SINGLE CYCLE SETTLING

By default, the AD7175-8 is configured with the SING_CYC bit in the ADC mode register set so that only fully settled data is output, effectively putting the ADC into a single cycle settling mode. This mode achieves single cycle settling by reducing the output data rate to be equal to the settling time of the ADC for the selected output data rate. This bit has no effect with the sinc5 + sinc1 filter at output data rates of 10 kSPS and lower.

Figure 57 shows a step on the analog input with this mode disabled and the sinc3 filter selected. The analog input requires at least three cycles after the step change for the output to reach the final settled value.

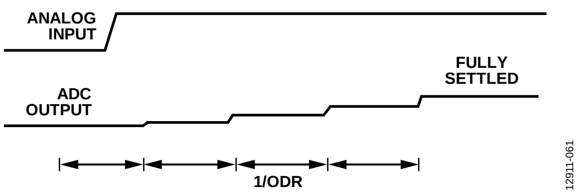


Figure 57. Step Input Without Single Cycle Settling

Figure 58 shows the same step on the analog input but with single cycle settling enabled. The analog input requires at least a single cycle for the output to be fully settled. The output data rate, as indicated by the $\overline{RDY}$ signal, is now reduced to equal the settling time of the filter at the selected output data rate.

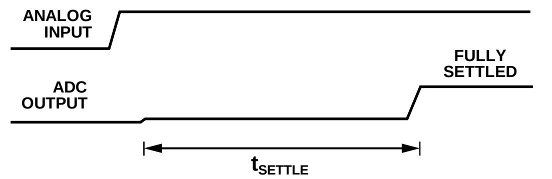


Figure 58. Step Input with Single Cycle Settling

Table 19. Output Data Rate, Settling Time, and Noise Using the Sinc5 + Sinc1 Filter with Input Buffers Disabled

Default Output Data Rate (SPS/Channel); SING_CYC = 1 or with Multiple Channels Enabled[1]	Output Data Rate (SPS); SING_CYC = 0 and Single Channel Enabled[1]	Settling Time[1]	Notch Frequency (Hz)	Noise (µV rms)	Effective Resolution with 5 V Reference (Bits)	Noise (µV p-p)[2]	Peak-to-Peak Resolution with 5 V Reference (Bits)
50,000	250,000	20 µs	250,000	8.7	20.1	65	17.2
41,667	125,000	24 µs	125,000	7.2	20.4	60	17.3
31,250	62,500	32 µs	62,500	5.5	20.8	43	17.8
27,778	50,000	36 µs	50,000	5	20.9	41	17.9
20,833	31,250	48 µs	31,250	4	21.3	32	18.3
17,857	25,000	56 µs	25,000	3.6	21.4	29	18.4
12,500	15,625	80 µs	15,625	2.9	21.7	22	18.8
10,000	10,000	100 µs	11,905	2.5	21.9	18.3	19.1
5000	5000	200 µs	5435	1.7	22.5	12	19.7
2500	2500	400 µs	2604	1.2	23.0	8.2	20.2
1000	1000	1.0 ms	1016	0.77	23.6	5.2	20.9
500.0	500	2.0 ms	504	0.57	24	3.2	21.6
397.5	397.5	2.516 ms	400.00	0.5	24	3	21.7
200.0	200	5.0 ms	200.64	0.36	24	2	22.3
100	100	10 ms	100.16	0.25	24	1.3	22.9
59.92	59.92	16.67 ms	59.98	0.19	24	1.1	23.1
49.96	49.96	20.016 ms	50.00	0.18	24	0.95	23.3
20.00	20	50.0 ms	20.01	0.11	24	0.6	24
16.66	16.66	60.02 ms	16.66	0.1	24	0.45	24
10.00	10	100 ms	10.00	0.08	24	0.4	24
5.00	5	200 ms	5.00	0.07	24	0.34	24

[1] The settling time is rounded to the nearest microsecond. This is reflected in the output data rate and channel switching rate. Channel switching rate = 1 ÷ settling time.
[2] Measurement taken using 1000 samples.

Table 20. Output Data Rate, Settling Time, and Noise Using the Sinc5 + Sinc1 Filter with Input Buffers Enabled

Default Output Data Rate (SPS/Channel); SING_CYC = 1 or with Multiple Channels Enabled[1]	Output Data Rate (SPS); SING_CYC = 0 and Single Channel Enabled[1]	Settling Time[1]	Notch Frequency (Hz)	Noise (µV rms)	Effective Resolution with 5 V Reference (Bits)	Noise (µV p-p)[2]	Peak-to-Peak Resolution with 5 V Reference (Bits)
50,000	250,000	20 µs	250,000	9.8	20	85	16.8
41,667	125,000	24 µs	125,000	8.4	20.2	66	17.2
31,250	62,500	32 µs	62,500	6.4	20.6	55	17.5
27,778	50,000	36 µs	50,000	5.9	20.7	49	17.6
20,833	31,250	48 µs	31,250	4.8	21	39	18.0
17,857	25,000	56 µs	25,000	4.3	21.1	33	18.2
12,500	15,625	80 µs	15,625	3.4	21.5	26	18.6
10,000	10,000	100 µs	11,905	3	21.7	23	18.7
5000	5000	200 µs	5435	2.1	22.2	16	19.3
2500	2500	400 µs	2604	1.5	22.7	10	19.9
1000	1000	1.0 ms	1016	0.92	23.4	5.7	20.7
500.0	500	2.0 ms	504	0.68	23.8	3.9	21.3
397.5	397.5	2.516 ms	400.00	0.6	24	3.7	21.4
200.0	200	5.0 ms	200.64	0.43	24	2.2	22.1
100	100	10 ms	100.16	0.32	24	1.7	22.5
59.92	59.92	16.67 ms	59.98	0.23	24	1.2	23
49.96	49.96	20.016 ms	50.00	0.2	24	1	23.3
20.00	20	50.0 ms	20.01	0.14	24	0.75	23.7
16.66	16.66	60.02 ms	16.66	0.13	24	0.66	23.9
10.00	10	100 ms	10.00	0.1	24	0.47	24
5.00	5	200 ms	5.00	0.07	24	0.32	24

[1] The settling time is rounded to the nearest microsecond. This is reflected in the output data rate and channel switching rate. Channel switching rate = 1 ÷ settling time.
[2] Measurement taken using 1000 samples.

Table 21. Output Data Rate, Settling Time, and Noise Using the Sinc3 Filter with Input Buffers Disabled

Default Output Data Rate (SPS/Channel); SING_CYC = 1 or with Multiple Channels Enabled[1]	Output Data Rate (SPS); SING_CYC = 0 and Single Channel Enabled[1]	Settling Time[1]	Notch Frequency (Hz)	Noise (µV rms)	Effective Resolution with 5 V Reference (Bits)	Noise (µV p-p)[2]	Peak-to-Peak Resolution with 5 V Reference (Bits)
83,333	250,000	12 µs	250,000	210	15.5	1600	12.6
41,667	125,000	24 µs	125,000	28	18.4	200	15.6
20,833	62,500	48 µs	62,500	5.2	20.9	40	17.9
16,667	50,000	60 µs	50,000	4.2	21.2	34	18.2
10,417	31,250	96 µs	31,250	3.2	21.6	26	18.6
8333	25,000	120 µs	25,000	2.9	21.7	23	18.7
5208	15,625	192 µs	15,625	2.2	22.1	17	19.2
3333	10,000	300 µs	10,000	1.8	22.4	14	19.4
1667	5000	6 µs	5000	1.3	22.9	9.5	20
833	2500	1.2 ms	2500	0.91	23.4	6	20.7
333.3	1000	3 ms	1000	0.56	24	3.9	21.3
166.7	500	6 ms	500	0.44	24	2.5	21.9
133.3	400	7.5 ms	400	0.4	24	2.3	22.1
66.7	200	15 ms	200	0.25	24	1.4	22.8
33.33	100	30 ms	100	0.2	24	1	23.3
19.99	60	50.02 ms	59.98	0.13	24	0.8	23.6
16.67	50	60 ms	50	0.13	24	0.7	23.8
6.67	20	150 ms	20	0.08	24	0.42	24
5.56	16.67	180 ms	16.67	0.07	24	0.37	24
3.33	10	300 ms	10	0.06	24	0.28	24
1.67	5	600 ms	5	0.05	24	0.21	24

[1] The settling time is rounded to the nearest microsecond. This is reflected in the output data rate and channel switching rate. Channel switching rate = 1 ÷ settling time.
[2] Measurement taken using 1000 samples.

Table 22. Output Data Rate, Settling Time, and Noise Using the Sinc3 Filter with Input Buffers Enabled

Default Output Data Rate (SPS/Channel); SING_CYC = 1 or with Multiple Channels Enabled[1]	Output Data Rate (SPS); SING_CYC = 0 and Single Channel Enabled[1]	Settling Time[1]	Notch Frequency (Hz)	Noise (µV rms)	Effective Resolution with 5 V Reference (Bits)	Noise (µV p-p)[2]	Peak-to-Peak Resolution with 5 V Reference (Bits)
83,333	250,000	12 µs	250,000	210	15.5	1600	12.6
41,667	125,000	24 µs	125,000	28	18.4	210	15.5
20,833	62,500	48 µs	62,500	5.8	20.7	48	17.7
16,667	50,000	60 µs	50,000	4.9	21	41	17.9
10,417	31,250	96 µs	31,250	3.8	21.3	30	18.3
8333	25,000	120 µs	25,000	3.4	21.5	26	18.6
5208	15,625	192 µs	15,625	2.6	21.9	18	19.1
3333	10,000	300 µs	10,000	2.1	22.2	16	19.3
1667	5000	6 µs	5000	1.5	22.7	11	19.8
833	2500	1.2 ms	2500	1.1	23.1	7	20.4
333.3	1000	3 ms	1000	0.71	23.7	4.5	21.1
166.7	500	6 ms	500	0.52	24	3	21.7
133.3	400	7.5 ms	400	0.41	24	2.7	21.8
66.7	200	15 ms	200	0.32	24	1.8	22.4
33.33	100	30 ms	100	0.2	24	1.2	23
19.99	60	50.02ms	59.98	0.17	24	1.1	23.1
16.67	50	60 ms	50	0.15	24	0.83	23.5
6.67	20	150 ms	20	0.13	24	0.61	24
5.56	16.67	180 ms	16.67	0.12	24	0.6	24
3.33	10	300 ms	10	0.1	24	0.55	24
1.67	5	600 ms	5	0.08	24	0.35	24

[1] The settling time is rounded to the nearest microsecond. This is reflected in the output data rate and channel switching rate. Channel switching rate = 1 ÷ settling time.
[2] Measurement taken using 1000 samples.

ENHANCED 50 HZ AND 60 HZ REJECTION FILTERS

The enhanced filters are designed to provide rejection of 50 Hz and 60 Hz simultaneously and to allow the user to trade off settling time and rejection. These filters can operate at up to 27.27 SPS or can reject up to 90 dB of 50 Hz ± 1 Hz and 60 Hz ± 1 Hz interference. These filters are realized by postfiltering the output of the sinc5 + sinc1 filter. For this reason, the sinc5 + sinc1 filter must be selected when using the enhanced filters to achieve the specified settling time and noise performance. Table 23 shows the output data rates with the accompanying settling time, rejection, and rms noise. Figure 59 to Figure 66 show the frequency domain plots of the responses from the enhanced filters.

Table 23. Enhanced Filters Output Data Rate, Noise, Settling Time, and Rejection Using the Enhanced Filters

Output Data Rate (SPS)	Settling Time (ms)	Simultaneous Rejection of 50 Hz ± 1 Hz and 60 Hz ± 1 Hz (dB)[1]	Noise (µV rms)	Peak-to-Peak Resolution (Bits)	Comments
Input Buffers Disabled					
27.27	36.67	47	0.22	22.7	See Figure 59 and Figure 62
25	40.0	62	0.2	22.9	See Figure 60 and Figure 63
20	50.0	85	0.2	22.9	See Figure 61 and Figure 64
16.667	60.0	90	0.17	23	See Figure 65 and Figure 66
Input Buffers Enabled					
27.27	36.67	47	0.22	22.7	See Figure 59 and Figure 62
25	40.0	62	0.22	22.7	See Figure 60 and Figure 63
20	50.0	85	0.21	22.8	See Figure 61 and Figure 64
16.667	60.0	90	0.21	22.8	See Figure 65 and Figure 66

[1] Master clock = 16 MHz.

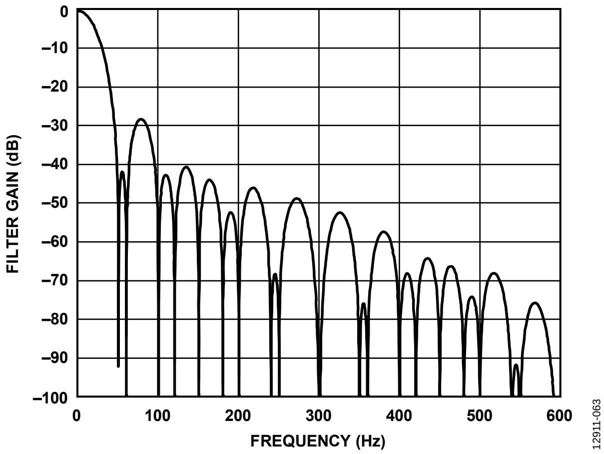


Figure 59. 27.27 SPS ODR, 36.67 ms Settling Time

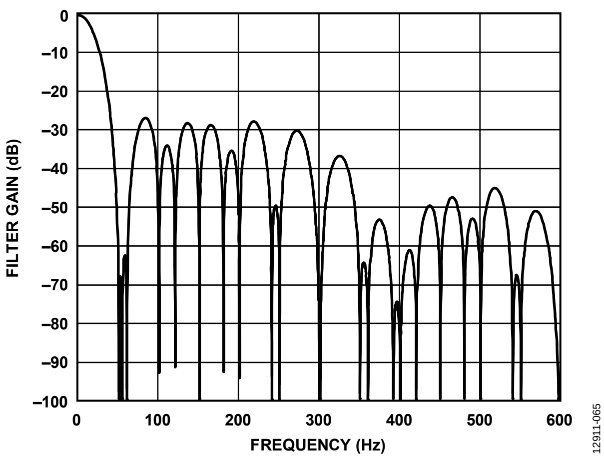


Figure 60. 25 SPS ODR, 40 ms Settling Time

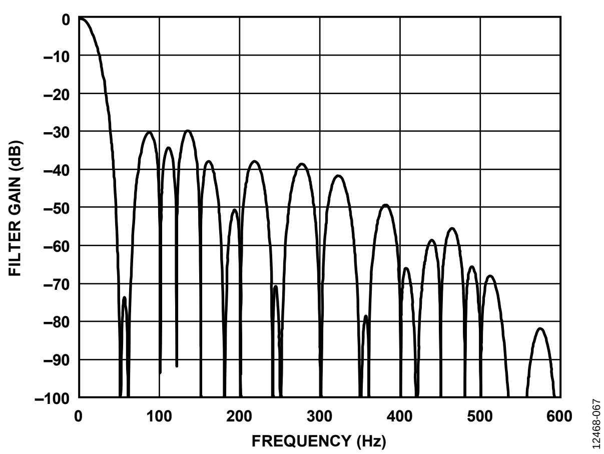


Figure 61. 20 SPS ODR, 50 ms Settling Time

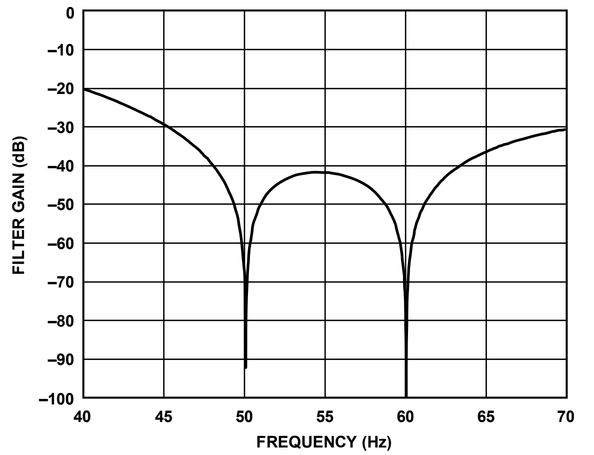


Figure 62. 27.27 SPS ODR, 36.67 ms Settling Time at 50 Hz/60 Hz

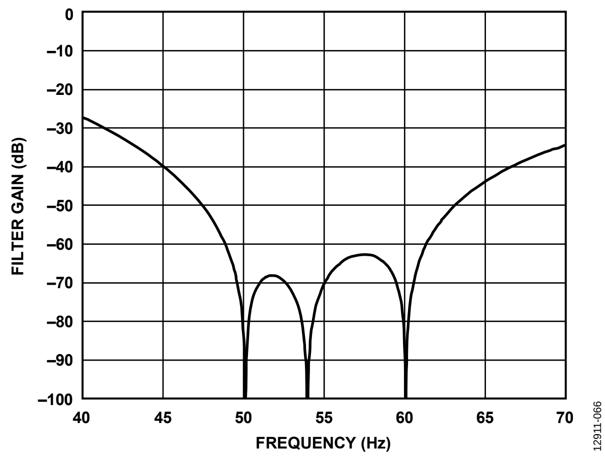


Figure 63. 25 SPS ODR, 40 ms Settling Time at 50 Hz/60 Hz

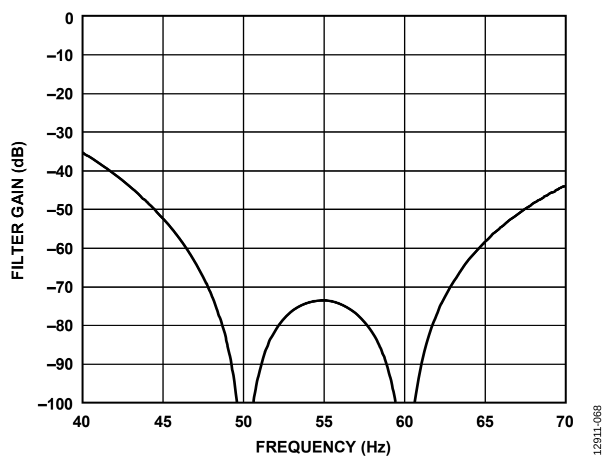


Figure 64. 20 SPS ODR, 50 ms Settling Time at 50 Hz/60 Hz

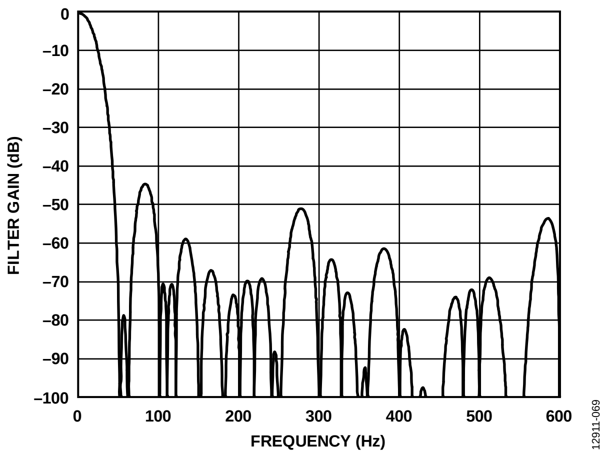


Figure 65. 16.667 SPS ODR, 60 ms Settling Time

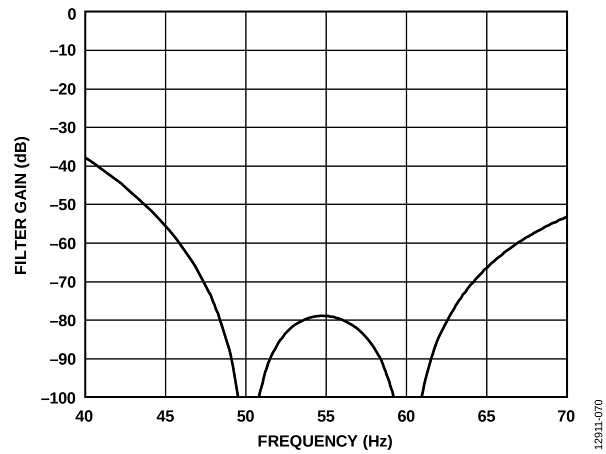


Figure 66. 16.667 SPS ODR, 60 ms Settling Time at 50 Hz/60 Hz

OPERATING MODES

The AD7175-8 has a number of operating modes that can be set from the ADC mode register and interface mode register (see Table 27 and Table 28). These modes are as follows and are described in the following sections:

- Continuous conversion mode
- Continuous read mode
- Single conversion mode
- Standby mode
- Power-down mode
- Calibration modes (three modes)

CONTINUOUS CONVERSION MODE

Continuous conversion is the default power-up mode. The AD7175-8 converts continuously, and the $\overline{\text{RDY}}$ bit in the status register goes low each time a conversion is complete. If $\overline{\text{CS}}$ is low, the $\overline{\text{RDY}}$ output also goes low when a conversion is complete. To read a conversion, the user writes to the communications register, indicating that the next operation is a read of the data register. When the data-word has been read from the data register, the DOUT/$\overline{\text{RDY}}$ pin goes high. The user can read this register additional times, if required. However, the user must ensure that the data register is not being accessed at the completion of the next conversion; otherwise, the new conversion word is lost.

When several channels are enabled, the ADC automatically sequences through the enabled channels, performing one conversion on each channel. When all channels have been converted, the sequence starts again with the first channel. The channels are converted in order from lowest enabled channel to highest enabled channel. The data register is updated as soon as each conversion is available. The $\overline{\text{RDY}}$ output pulses low each time a conversion is available. The user can then read the conversion while the ADC converts the next enabled channel.

If the DATA_STAT bit in the interface mode register is set to 1, the contents of the status register, along with the conversion data, are output each time the data register is read. The status register indicates the channel to which the conversion corresponds.

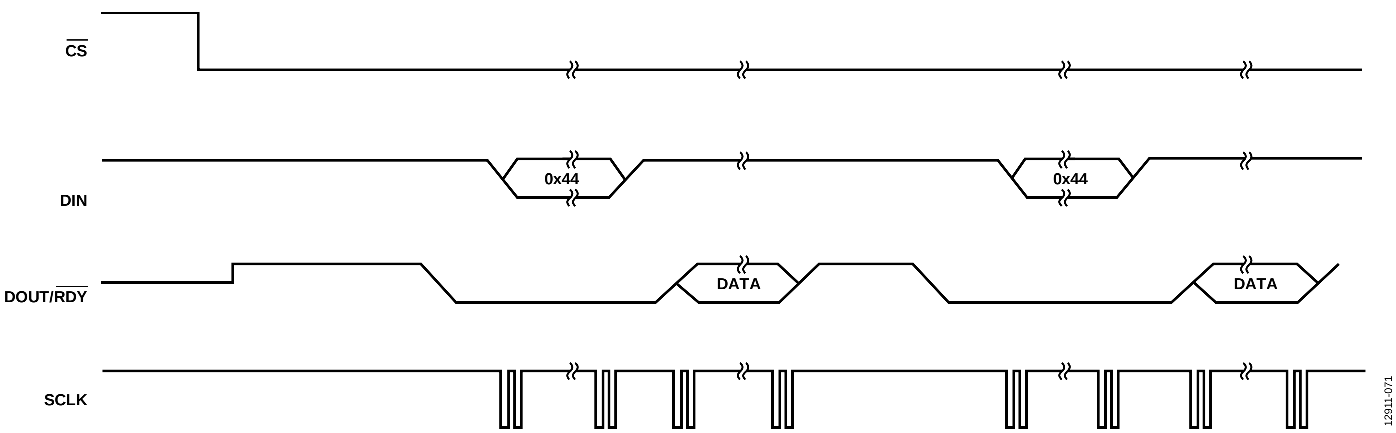


Figure 67. Continuous Conversion Mode

CONTINUOUS READ MODE

In continuous read mode, it is not required to write to the communications register before reading ADC data; apply only the required number of SCLK pulses after $\overline{RDY}$ goes low to indicate the end of a conversion. When the conversion is read, $\overline{RDY}$ returns high until the next conversion is available. In this mode, the data can be read only once. The user must also ensure that the data-word is read before the next conversion is complete. If the user has not read the conversion before the completion of the next conversion or if insufficient serial clocks are applied to the AD7175-8 to read the data-word, the serial output register is reset shortly before the next conversion is complete, and the new conversion is placed in the output serial register. The ADC must be configured for continuous conversion mode to use continuous read mode.

To enable continuous read mode, set the CONTREAD bit in the interface mode register. When this bit is set, the only serial interface operations possible are reads from the data register. To exit continuous read mode, issue a dummy read of the ADC data register command (0x44) while the $\overline{RDY}$ output is low. Alternatively, apply a software reset, that is, 64 SCLK pulses with $\overline{CS}$ = 0 and DIN = 1. This resets the ADC and all register contents. These are the only commands that the interface recognizes after it is placed in continuous read mode. Hold DIN low in continuous read mode until an instruction is to be written to the device.

If multiple ADC channels are enabled, each channel is output in turn, with the status bits being appended to the data if DATA_STAT is set in the interface mode register. The status register indicates the channel to which the conversion corresponds.

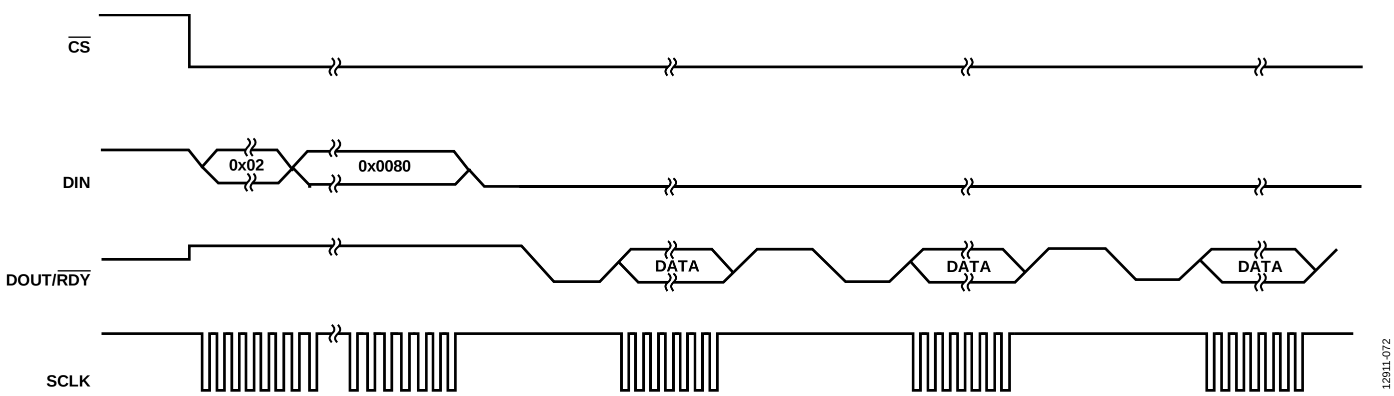


Figure 68. Continuous Read Mode

SINGLE CONVERSION MODE

In single conversion mode, the AD7175-8 performs a single conversion and is placed in standby mode after the conversion is complete. The $\overline{RDY}$ output goes low to indicate the completion of a conversion. When the data-word has been read from the data register, the DOUT/$\overline{RDY}$ pin goes high. The data register can be read several times, if required, even when the DOUT/$\overline{RDY}$ pin has gone high.

If several channels are enabled, the ADC automatically sequences through the enabled channels and performs a conversion on each channel. When a conversion is started, the DOUT/$\overline{RDY}$ pin goes high and remains high until a valid conversion is available and $\overline{CS}$ is low. As soon as the conversion is available, the $\overline{RDY}$ output goes low. The ADC then selects the next channel and begins a conversion. The user can read the present conversion while the next conversion is being performed. As soon as the next conversion is complete, the data register is updated; therefore, the user has a limited period in which to read the conversion. When the ADC has performed a single conversion on each of the selected channels, it returns to standby mode.

If the DATA_STAT bit in the interface mode register is set to 1, the contents of the status register, along with the conversion, are output each time the data register is read. The two LSBs of the status register indicate the channel to which the conversion corresponds.

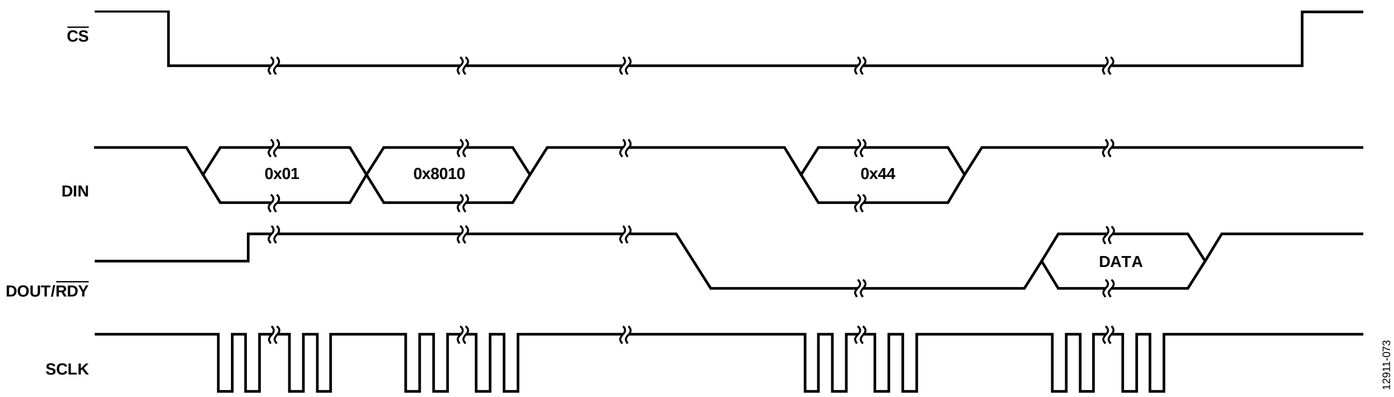


Figure 69. Single Conversion Mode

STANDBY AND POWER-DOWN MODES

In standby mode, most blocks are powered down. The LDOs remain active so that registers maintain their contents. The internal reference remains active if enabled, and the crystal oscillator remains active if selected. To power down the reference in standby mode, set the REF_EN bit in the ADC mode register to 0. To power down the clock in standby mode, set the CLOCKSEL bits in the ADC mode register to 00 (internal oscillator).

In power-down mode, all blocks are powered down, including the LDOs. All registers lose their contents, and the GPIOx outputs are placed in three-state. To prevent accidental entry to power-down mode, the ADC must first be placed in standby mode. Exiting power-down mode requires 64 SCLK pulses with $\overline{CS}$ = 0 and DIN = 1, that is, a serial interface reset. A delay of 500 µs is recommended before issuing a subsequent serial interface command to allow the LDO to power up.

Figure 19 shows the internal reference settling time after returning from standby mode (setting REF_EN = 0 and then 1) and returning from power down.

CALIBRATION

The AD7175-8 allows a two-point calibration to be performed to eliminate any offset and gain errors. Three calibration modes eliminate these offset and gain errors on a per setup basis:

- Internal zero-scale calibration mode
- System zero-scale calibration mode
- System full-scale calibration mode

There is no internal full-scale calibration mode because this is calibrated in the factory at the time of production.

Only one channel can be active during calibration. After each conversion, the ADC conversion result is scaled using the ADC calibration registers before being written to the data register.

The default value of the offset register is 0x800000, and the nominal value of the gain register is 0x555555. The calibration range of the ADC gain is from 0.4 × V_{REF} to 1.05 × V_{REF}. The following equations show the calculations that are used. In unipolar mode, the ideal relationship—that is, not taking into account the ADC gain error and offset error—is as follows:

$$Data = \left(\frac{0.75 \times V_{IN}}{V_{REF}} \times 2^{23} - (Offset - 0x800000)\right) \times \frac{Gain}{0x400000} \times 2$$

In bipolar mode, the ideal relationship—that is, not taking into account the ADC gain error and offset error—is as follows:

$$Data = \left(\frac{0.75 \times V_{IN}}{V_{REF}} \times 2^{23} - (Offset - 0x800000)\right) \times \frac{Gain}{0x400000} + 0x800000$$

To start a calibration, write the relevant value to the mode bits in the ADC mode register. The DOUT/$\overline{RDY}$ pin and the $\overline{RDY}$ bit in the status register go high when the calibration initiates. When the calibration is complete, the contents of the corresponding offset or gain register are updated, the $\overline{RDY}$ bit in the status register is reset and the $\overline{RDY}$ output pin returns low (if $\overline{CS}$ is low), and the AD7175-8 reverts to standby mode.

During an internal offset calibration, the selected positive analog input pin is disconnected, and both modulator inputs are connected internally to the selected negative analog input pin. For this reason, it is necessary to ensure that the voltage on the selected negative analog input pin does not exceed the allowed limits and is free from excessive noise and interference.

System calibrations, however, expect the system zero-scale (offset) and system full-scale (gain) voltages to be applied to the ADC pins before initiating the calibration modes. As a result, errors external to the ADC are removed.

From an operational point of view, treat a calibration like another ADC conversion. An offset calibration, if required, must always be performed before a full-scale calibration. Set the system software to monitor the $\overline{RDY}$ bit in the status register or the $\overline{RDY}$ output to determine the end of a calibration via a polling sequence or an interrupt driven routine. All calibrations require a time equal to the settling time of the selected filter and output data rate to be completed.

An internal offset calibration, system zero-scale calibration, and system full-scale calibration can be performed at any output data rate. Using lower output data rates results in better calibration accuracy and is accurate for all output data rates. A new offset calibration is required for a given channel if the reference source for that channel is changed.

The offset error is typically ±60 µV and an offset calibration reduces the offset error to the order of the noise. The gain error is factory calibrated at ambient temperature. Following this calibration, the gain error is typically ±80 ppm of FSR.

The AD7175-8 provides the user with access to the on-chip calibration registers, allowing the microprocessor to read the calibration coefficients of the device and to write its own calibration coefficients. A read or write of the offset and gain registers can be performed at any time except during an internal or self calibration.

DIGITAL INTERFACE

The programmable functions of the AD7175-8 are controlled via the SPI serial interface. The serial interface of the AD7175-8 consists of four signals: $\overline{\text{CS}}$, DIN, SCLK, and DOUT/$\overline{\text{RDY}}$. The DIN input is used to transfer data into the on-chip registers, and the DOUT output is used to access data from the on-chip registers. SCLK is the serial clock input for the device, and all data transfers (either on the DIN input or on the DOUT output) occur with respect to the SCLK signal.

The DOUT/$\overline{\text{RDY}}$ pin also functions as a data ready signal, with the output going low if $\overline{\text{CS}}$ is low when a new data-word is available in the data register. The $\overline{\text{RDY}}$ output is reset high when a read operation from the data register is complete. The $\overline{\text{RDY}}$ output also goes high before updating the data register to indicate when not to read from the device to ensure that a data read is not attempted while the register is being updated. Take care to avoid reading from the data register when the $\overline{\text{RDY}}$ output is about to go low. The best method to ensure that no data read occurs is to always monitor the $\overline{\text{RDY}}$ output; start reading the data register as soon as the $\overline{\text{RDY}}$ output goes low; and ensure a sufficient SCLK rate, such that the read is complete before the next conversion result. $\overline{\text{CS}}$ is used to select a device. It can be used to decode the AD7175-8 in systems where several components are connected to the serial bus.

Figure 2 and Figure 3 show timing diagrams for interfacing to the AD7175-8 using $\overline{\text{CS}}$ to decode the device. Figure 2 shows the timing for a read operation from the AD7175-8, and Figure 3 shows the timing for a write operation to the AD7175-8. It is possible to read from the data register several times even though the $\overline{\text{RDY}}$ output returns high after the first read operation. However, care must be taken to ensure that the read operations are completed before the next output update occurs. In continuous read mode, the data register can be read only once.

The serial interface can operate in 3-wire mode by tying $\overline{\text{CS}}$ low. In this case, the SCLK, DIN, and DOUT/$\overline{\text{RDY}}$ pins are used to communicate with the AD7175-8. The end of the conversion can also be monitored using the $\overline{\text{RDY}}$ bit in the status register.

The AD7175-8 can be reset by writing 64 SCLKs with $\overline{\text{CS}}$ = 0 and DIN = 1. A reset returns the interface to the state in which it expects a write to the communications register. This operation resets the contents of all registers to their power-on values. Following a reset, allow a period of 500 µs before addressing the serial interface.

CHECKSUM PROTECTION

The AD7175-8 has a checksum mode that can be used to improve interface robustness. Using the checksum ensures that only valid data is written to a register and allows data read from a register to be validated. If an error occurs during a register write, the CRC_ERROR bit is set in the status register. However, to ensure that the register write is successful, read back the register and verify the checksum.

For CRC checksum calculations during a write operation, the following polynomial is always used:

$$x^8 + x^2 + x + 1$$

During read operations, the user can select between this polynomial and a simpler exclusive OR (XOR) function. The XOR function requires less time to process on the host microcontroller than the polynomial-based checksum. The CRC_EN bits in the interface mode register enable and disable the checksum and allow the user to select between the polynomial check and the simple XOR check.

The checksum is appended to the end of each read and write transaction. The checksum calculation for the write transaction is calculated using the 8-bit command word and the 8-bit to 24-bit data. For a read transaction, the checksum is calculated using the command word and the 8-bit to 32-bit data output. Figure 70 and Figure 71 show SPI write and read transactions, respectively.

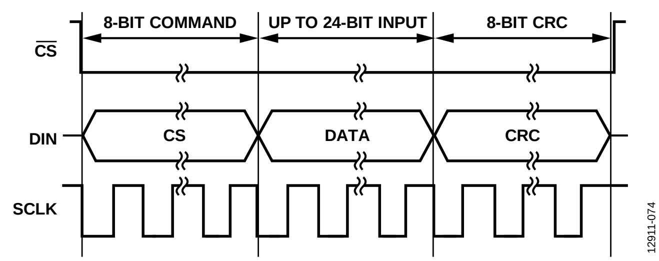


Figure 70. SPI Write Transaction with CRC

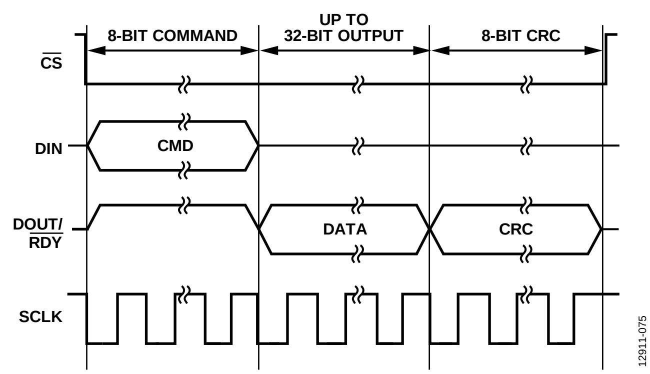


Figure 71. SPI Read Transaction with CRC

If checksum protection is enabled when continuous read mode is active, an implied read data command of 0x44 before every data transmission must be accounted for when calculating the checksum value. This implied read data command ensures a nonzero checksum value even if the ADC data equals 0x000000.

CRC CALCULATION

Polynomial

The checksum, which is eight bits wide, is generated using the polynomial

$$x^8 + x^2 + x + 1$$

To generate the checksum, the data is left shifted by eight bits to create a number ending in eight Logic 0s. The polynomial is aligned so that its MSB is adjacent to the leftmost Logic 1 of the data. An XOR function is applied to the data to produce a new, shorter number. The polynomial is again aligned so that its MSB is adjacent to the leftmost Logic 1 of the new result, and the procedure is repeated. This process repeats until the original data is reduced to a value less than the polynomial. This is the 8-bit checksum.

Example of a Polynomial CRC Calculation—24-Bit Word: 0x654321 (Eight Command Bits and 16-Bit Data)

An example of generating the 8-bit checksum using the polynomial based checksum is as follows:

```
Initial value     011001010100001100100001
                  01100101010000110010000100000000     left shifted eight bits
x^8 + x^2 + x + 1 =        100000111                   polynomial
  10010010000011001000010000000               XOR result
  100000111                           polynomial
     1000110001100100001000000000             XOR result
     100000111                        polynomial
        111111100100001000000000              XOR result
        100000111                     polynomial value
         11111011100001000000000              XOR result
         100000111                    polynomial value
          1111000000001000000000              XOR result
          100000111                   polynomial value
           111001110001000000000              XOR result
           100000111                  polynomial value
            11001001001000000000              XOR result
            100000111                 polynomial value
             1001010101000000000              XOR result
             100000111                polynomial value
                101101100000000               XOR result
                100000111             polynomial value
                  1101011000000               XOR result
                  100000111           polynomial value
                   101010110000               XOR result
                   100000111          polynomial value
                     1010001000               XOR result
                     100000111        polynomial value
                       10000110       checksum = 0x86
```

XOR Calculation

The checksum, which is 8 bits wide, is generated by splitting the data into bytes and then performing an XOR of the bytes.

Example of an XOR Calculation—24-Bit Word: 0x654321 (Eight Command Bits and 16-Bit Data)

Using the previous example of a polynomial CRC calculation, divide the data into three bytes: 0x65, 0x43, and 0x21

01100101	0x65
01000011	0x43
00100110	XOR result
00100001	0x21
00000111	CRC

INTEGRATED FUNCTIONS

The AD7175-8 has integrated functions that improve the usefulness of a number of applications as well as serve diagnostic purposes in safety conscious applications.

GENERAL-PURPOSE I/O

The AD7175-8 has two general-purpose digital input/output pins (GPIO0, GPIO1) and two general-purpose digital output pins (GPO2, GPO3). As the naming convention suggests, the GPIO0 and GPIO1 pins can be configured as inputs or outputs, but GPO2 and GPO3 are outputs only. The GPIOx and GPOx pins are enabled using the following bits in the GPIOCON register: IP_EN0, IP_EN1 (or OP_EN0, OP_EN1) for GPIO0 and GPIO1, and OP_EN2_3 for GPO2 and GPO3.

When the GPIO0 or GPIO1 pin is enabled as an input, the logic level at the pin is contained in the GP_DATA0 or GP_DATA1 bit, respectively. When the GPIO0, GPIO1, GPO2, or GPO3 pin is enabled as an output, the GP_DATA0, GP_DATA1, GP_DATA2, or GP_DATA3 bit, respectively, determines the logic level output at the pin. The logic levels for these pins are referenced to AVDD1 and AVSS; therefore, outputs have an amplitude of 5 V.

The $\overline{\text{ERROR}}$ pin can also be used as a general-purpose output. When the ERR_EN bits in the GPIOCON register are set to 11, the $\overline{\text{ERROR}}$ pin operates as a general-purpose output. In this configuration, the ERR_DAT bit in the GPIOCON register determines the logic level output at the pin. The logic level for the pin is referenced to IOVDD and DGND.

Both GPIOs and the $\overline{\text{ERROR}}$ pin, when set as general-purpose outputs, have an active pull-up circuit.

EXTERNAL MULTIPLEXER CONTROL

If an external multiplexer is used to increase the channel count, the multiplexer logic pins can be controlled via the AD7175-8 GPIOx pins. With the MUX_IO bit, the GPIOx timing is controlled by the ADC; therefore, the channel change is synchronized with the ADC, eliminating any need for external synchronization.

DELAY

It is possible to insert a programmable delay before the AD7175-8 begins to take samples. This delay allows an external amplifier or multiplexer to settle and can alleviate the specification requirements for the external amplifier or multiplexer. Eight programmable settings, ranging from 0 µs to 1 ms, can be set using the delay bits in the ADC mode register (Register 0x01, Bits[10:8]).

If a delay greater than 0 µs is selected and the HIDE_DELAY bit in the ADC mode register is set to 0, this delay is added to the conversion time, regardless of the selected output data rate.

When using the sinc5 + sinc1 filter, it is possible to hide this delay such that the output data rate remains the same as the output data rate without the delay enabled. If the HIDE_DELAY bit is set to 1 and the selected delay is less than half of the conversion time, the delay can be absorbed by reducing the number of averages the digital filter performs, which keeps the conversion time the same but can affect the noise performance.

The effect on the noise performance depends on the delay time compared to the conversion time. It is possible to absorb the delay only for output data rates less than 10 kSPS with the exception of the following four rates, which cannot absorb any delay: 397.5 SPS, 59.92 SPS, 49.96 SPS, and 16.66 SPS.

16-BIT/24-BIT CONVERSIONS

By default, the AD7175-8 generates 24-bit conversions. However, the width of the conversions can be reduced to 16 bits. Setting the WL16 bit in the interface mode register to 1 rounds all data conversions to 16 bits. Clearing this bit sets the width of the data conversions to 24 bits.

DOUT_RESET

The serial interface uses a shared DOUT/$\overline{\text{RDY}}$ pin. By default, this pin outputs the $\overline{\text{RDY}}$ signal. During a data read, this pin outputs the data from the register being read. After the read is complete, the pin reverts to outputting the $\overline{\text{RDY}}$ signal after a short fixed period of time (t_7). However, this time may be too short for some microcontrollers and can be extended until the $\overline{\text{CS}}$ pin is brought high by setting the DOUT_RESET bit in the interface mode register to 1. This means that $\overline{\text{CS}}$ must be used to frame each read operation and compete the serial interface transaction.

SYNCHRONIZATION

Normal Synchronization

When the SYNC_EN bit in the GPIOCON register is set to 1, the $\overline{\text{SYNC}}$ pin functions as a synchronization input. The $\overline{\text{SYNC}}$ input lets the user reset the modulator and the digital filter without affecting any of the setup conditions on the device. This feature lets the user start to gather samples of the analog input from a known point, the rising edge of the $\overline{\text{SYNC}}$ input. The $\overline{\text{SYNC}}$ input must be low for at least one master clock cycle to ensure that synchronization occurs.

If multiple AD7175-8 devices are operated from a common master clock, they can be synchronized so that their analog inputs are sampled simultaneously. This synchronization is normally done after each AD7175-8 device has performed its own calibration or has calibration coefficients loaded into its calibration registers. A falling edge on the $\overline{\text{SYNC}}$ input resets the digital filter and the analog modulator and places the AD7175-8 into a consistent known state. While the $\overline{\text{SYNC}}$ input is low, the AD7175-8 is maintained in this known state. On the $\overline{\text{SYNC}}$ input rising edge, the modulator and filter are taken out of this reset state, and on the next master clock edge, the device starts to gather input samples again.

The device is taken out of reset on the master clock falling edge following the $\overline{\text{SYNC}}$ input low to high transition. Therefore, when multiple devices are being synchronized, take the SYNC input high on the master clock rising edge to ensure that all devices are released on the master clock falling edge. If the SYNC input is not taken high in sufficient time, a difference of one master clock cycle between the devices is possible; that is, the instant at which conversions are available differs from device to device by a maximum of one master clock cycle.

The SYNC input can also be used as a start conversion command for a single channel when in normal synchronization mode. In this mode, the rising edge of the SYNC input starts a conversion, and the falling edge of the RDY output indicates when the conversion is complete. The settling time of the filter is required for each data register update. After the conversion is complete, bring the SYNC input low in preparation for the next conversion start signal.

Alternate Synchronization

In alternate synchronization mode, the SYNC input operates as a start conversion command when several channels of the AD7175-8 are enabled. Setting the ALT_SYNC bit in the interface mode register to 1 enables an alternate synchronization scheme. When the SYNC input is taken low, the ADC completes the conversion on the current channel, selects the next channel in the sequence, and then waits until the SYNC input is taken high to commence the conversion. The RDY output goes low when the conversion is complete on the current channel, and the data register is updated with the corresponding conversion. Therefore, the SYNC input does not interfere with the sampling on the currently selected channel but allows the user to control the instant at which the conversion begins on the next channel in the sequence.

Alternate synchronization mode can be used only when several channels are enabled. It is not recommended to use this mode when a single channel is enabled.

ERROR FLAGS

The status register contains three error bits—ADC_ERROR, CRC_ERROR, and REG_ERROR—that flag errors with the ADC conversion, errors with the CRC check, and errors caused by changes in the registers, respectively. In addition, the ERROR output can indicate that an error has occurred.

ADC_ERROR

The ADC_ERROR bit in the status register flags any errors that occur during the conversion process. The flag is set when an overrange or underrange result is output from the ADC. The ADC also outputs all 0s or all 1s when an undervoltage or overvoltage occurs. This flag is reset only when the overvoltage or undervoltage is removed. It is not reset by a read of the data register.

CRC_ERROR

If the CRC value that accompanies a write operation does not correspond with the information sent, the CRC_ERROR flag is set. The flag is reset as soon as the status register is explicitly read.

REG_ERROR

The REG_ERROR flag is used in conjunction with the REG_CHECK bit in the interface mode register. When the REG_CHECK bit is set, the AD7175-8 monitors the values in the on-chip registers. If a bit changes, the REG_ERROR bit is set. Therefore, for writes to the on-chip registers, set REG_CHECK to 0. When the registers have been updated, the REG_CHECK bit can be set to 1. The AD7175-8 calculates a checksum of the on-chip registers. If one of the register values has changed, the REG_ERROR bit is set. If an error is flagged, set REG_CHECK to 0 to clear the REG_ERROR bit in the status register. The register check function does not monitor the data register, status register, or interface mode register.

ERROR Input/Output

The ERROR pin functions as an error input/output pin or a general-purpose output pin. The ERR_EN bits in the GPIOCON register determine the function of the pin.

When ERR_EN is set to 10, the ERROR pin functions as an open-drain error output, ERROR. The three error bits in the status register (ADC_ERROR, CRC_ERROR, and REG_ERROR) are OR'ed, inverted, and mapped to the ERROR output. Therefore, the ERROR output indicates that an error has occurred. The status register must be read to identify the error source.

When ERR_EN is set to 01, the ERROR pin functions as an error input, ERROR. The error output of another component can be connected to the AD7175-8 ERROR input so that the AD7175-8 indicates when an error occurs on either itself or the external component. The value on the ERROR input is inverted and OR'ed with the errors from the ADC conversion, and the result is indicated via the ADC_ERROR bit in the status register. The value of the ERROR input is reflected in the ERR_DAT bit in the GPIO configuration register.

The ERROR input/output is disabled when ERR_EN is set to 00. When the ERR_EN bits are set to 11, the ERROR pin operates as a general-purpose output.

DATA_STAT

The contents of the status register can be appended to each conversion on the AD7175-8. This function is useful if several channels are enabled. Each time a conversion is output, the contents of the status register are appended. The two LSBs of the status register indicate to which channel the conversion corresponds. In addition, the user can determine if any errors are being flagged by the error bits.

IOSTRENGTH

The serial interface can operate with a power supply as low as 2 V. However, at this low voltage, the DOUT/RDY pin may not have sufficient drive strength if there is moderate parasitic capacitance on the board or the SCLK frequency is high. The

IOSTRENGTH bit in the interface mode register increases the drive strength of the DOUT/$\overline{\text{RDY}}$ pin.

POWER-DOWN SWITCH

Setting the PDSW bit in the GPIO configuration register allows the PDSW pin to sink current. This function can be used in applications where the switch controls the power-up/power-down of the analog front-end sensor, for example, a bridge sensor. The PDSW pin can sink 16 mA maximum.

INTERNAL TEMPERATURE SENSOR

The AD7175-8 has an integrated temperature sensor. The temperature sensor can be used as a guide for the ambient temperature at which the device is operating. This can be used for diagnostic purposes or as an indicator of when the application circuit needs to rerun a calibration routine to take into account a shift in operating temperature. The temperature sensor is selected using the crosspoint multiplexer and is selected in the same way as an analog input channel. The temperature sensor requires that the analog input buffers be enabled on both analog inputs. If the buffers are not enabled, selecting the temperature sensor as an input forces the buffers to be enabled during the conversion.

To use the temperature sensor, the first step is to calibrate the device in a known temperature (25°C) and take a conversion as a reference point. The temperature sensor has a nominal sensitivity of 470 μV/K; use the difference in this ideal slope and the slope measured to calibrate the temperature sensor. The temperature sensor is specified with a ±2°C typical accuracy after calibration at 25°C. The temperature can be calculated as follows:

$$Temperature\ (°C) = \left(\frac{Conversion\ Result}{470\ \mu V}\right) - 273.15$$

GROUNDING AND LAYOUT

The analog inputs and reference inputs are differential and, therefore, most of the voltages in the analog modulator are common-mode voltages. The high common-mode rejection of the device removes common-mode noise on these inputs. The analog and digital supplies to the AD7175-8 are independent and connected to separate pins to minimize coupling between the analog and digital sections of the device. The digital filter provides rejection of broadband noise on the power supplies, except at integer multiples of the master clock frequency.

The digital filter also removes noise from the analog and reference inputs, provided that these noise sources do not saturate the analog modulator. As a result, the AD7175-8 is more immune to noise interference than a conventional high resolution converter. However, because the resolution of the AD7175-8 is high and the noise levels from the converter are so low, take care with regard to grounding and layout.

The PCB that houses the ADC must be designed such that the analog and digital sections are separated and confined to certain areas of the board. A minimum etch technique is generally best for ground planes because it results in the best shielding.

In any layout, the user must consider the flow of currents in the system, ensuring that the paths for all return currents are as close as possible to the paths the currents took to reach their destinations.

Avoid running digital lines under the device because this couples noise onto the die and allows the analog ground plane to run under the AD7175-8 to prevent noise coupling. The power supply lines to the AD7175-8 must use as wide a trace as possible to provide low impedance paths and reduce glitches on the power supply line. Shield fast switching signals like clocks with digital ground to prevent radiating noise to other sections of the board and never run clock signals near the analog inputs. Avoid crossover of digital and analog signals. Run traces on opposite sides of the board at right angles to each other. This technique reduces the effects of feedthrough on the board. A microstrip technique is by far the best method but is not always possible with a double sided board.

Good decoupling is important when using high resolution ADCs. The AD7175-8 has three power supply pins—AVDD1, AVDD2, and IOVDD. The AVDD1 and AVDD2 pins are referenced to AVSS, and the IOVDD pin is referenced to DGND. Decouple AVDD1 and AVDD2 with a 10 μF capacitor in parallel with a 0.1 μF capacitor to AVSS on each pin. Place the 0.1 μF capacitor as close as possible to the device on each supply, ideally right up against the device. Decouple IOVDD with a 10 μF capacitor in parallel with a 0.1 μF capacitor to DGND. Decouple all analog inputs to AVSS. If an external reference is used, decouple the REF+ and REF− pins to AVSS.

The AD7175-8 also has two on-board LDO regulators—one that regulates the AVDD2 supply and one that regulates the IOVDD supply. For the REGCAPA pin, it is recommended that 1 μF and 0.1 μF capacitors to AVSS be used. Similarly, for the REGCAPD pin, it is recommended that 1 μF and 0.1 μF capacitors to DGND be used.

If using the AD7175-8 for split supply operation, a separate plane must be used for AVSS.

REGISTER SUMMARY

Table 24. Register Summary

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x00	COMMS	[7:0]	$\overline{WEN}$	$R/\overline{W}$	RA						0x00	W
0x00	STATUS	[7:0]	$\overline{RDY}$	ADC_ERROR	CRC_ERROR	REG_ERROR	CHANNEL				0x80	R
0x01	ADCMODE	[15:8]	REF_EN	HIDE_DELAY	SING_CYC	RESERVED		DELAY			0xA000	RW
		[7:0]	RESERVED	MODE			CLOCKSEL		RESERVED			
0x02	IFMODE	[15:8]	RESERVED			ALT_SYNC	IOSTRENGTH	RESERVED		DOUT_RESET	0x0000	RW
		[7:0]	CONTREAD	DATA_STAT	REG_CHECK	RESERVED	CRC_EN		RESERVED	WL16		
0x03	REGCHECK	[23:16]	REGISTER_CHECK[23:16]								0x000000	R
		[15:8]	REGISTER_CHECK[15:8]									
		[7:0]	REGISTER_CHECK[7:0]									
0x04	DATA	[23:16]	DATA[23:16]								0x000000	R
		[15:8]	DATA[15:8]									
		[7:0]	DATA[7:0]									
0x06	GPIOCON	[15:8]	RESERVED	PDSW	OP_EN2_3	MUX_IO	SYNC_EN	ERR_EN		ERR_DAT	0x0800	RW
		[7:0]	GP_DATA3	GP_DATA2	IP_EN1	IP_EN0	OP_EN1	OP_EN0	GP_DATA1	GP_DATA0		
0x07	ID	[15:8]	ID[15:8]								0x3CDx	R
		[7:0]	ID[7:0]									
0x10	CH0	[15:8]	CH_EN0	SETUP_SEL0			RESERVED		AINPOS0[4:3]		0x8001	RW
		[7:0]	AINPOS0[2:0]			AINNEG0						
0x11	CH1	[15:8]	CH_EN1	SETUP_SEL1			RESERVED		AINPOS1[4:3]		0x0001	RW
		[7:0]	AINPOS1[2:0]			AINNEG1						
0x12	CH2	[15:8]	CH_EN2	SETUP_SEL2			RESERVED		AINPOS2[4:3]		0x0001	RW
		[7:0]	AINPOS2[2:0]			AINNEG2						
0x13	CH3	[15:8]	CH_EN3	SETUP_SEL3			RESERVED		AINPOS3[4:3]		0x0001	RW
		[7:0]	AINPOS3[2:0]			AINNEG3						
0x14	CH4	[15:8]	CH_EN4	SETUP_SEL4			RESERVED		AINPOS4[4:3]		0x0001	RW
		[7:0]	AINPOS4[2:0]			AINNEG4						
0x15	CH5	[15:8]	CH_EN5	SETUP_SEL5			RESERVED		AINPOS5[4:3]		0x0001	RW
		[7:0]	AINPOS5[2:0]			AINNEG5						
0x16	CH6	[15:8]	CH_EN6	SETUP_SEL6			RESERVED		AINPOS6[4:3]		0x0001	RW
		[7:0]	AINPOS6[2:0]			AINNEG6						
0x17	CH7	[15:8]	CH_EN7	SETUP_SEL7			RESERVED		AINPOS7[4:3]		0x0001	RW
		[7:0]	AINPOS7[2:0]			AINNEG7						
0x18	CH8	[15:8]	CH_EN8	SETUP_SEL8			RESERVED		AINPOS8[4:3]		0x0001	RW
		[7:0]	AINPOS8[2:0]			AINNEG8						
0x19	CH9	[15:8]	CH_EN9	SETUP_SEL9			RESERVED		AINPOS9[4:3]		0x0001	RW
		[7:0]	AINPOS9[2:0]			AINNEG9						
0x1A	CH10	[15:8]	CH_EN10	SETUP_SEL10			RESERVED		AINPOS10[4:3]		0x0001	RW
		[7:0]	AINPOS10[2:0]			AINNEG10						
0x1B	CH11	[15:8]	CH_EN11	SETUP_SEL11			RESERVED		AINPOS11[4:3]		0x0001	RW
		[7:0]	AINPOS11[2:0]			AINNEG11						
0x1C	CH12	[15:8]	CH_EN12	SETUP_SEL12			RESERVED		AINPOS12[4:3]		0x0001	RW
		[7:0]	AINPOS12[2:0]			AINNEG12						
0x1D	CH13	[15:8]	CH_EN13	SETUP_SEL13			RESERVED		AINPOS13[4:3]		0x0001	RW
		[7:0]	AINPOS13[2:0]			AINNEG13						
0x1E	CH14	[15:8]	CH_EN14	SETUP_SEL14			RESERVED		AINPOS14[4:3]		0x0001	RW
		[7:0]	AINPOS14[2:0]			AINNEG14						
0x1F	CH15	[15:8]	CH_EN15	SETUP_SEL15			RESERVED		AINPOS15[4:3]		0x0001	RW
		[7:0]	AINPOS15[2:0]			AINNEG15						
0x20	SETUPCON0	[15:8]	RESERVED			BI_UNIPOLAR0	REFBUF0+	REFBUF0−	AINBUF0+	AINBUF0−	0x1320	RW
		[7:0]	BURNOUT_EN0	RESERVED	REF_SEL0		RESERVED					
0x21	SETUPCON1	[15:8]	RESERVED			BI_UNIPOLAR1	REFBUF1+	REFBUF1−	AINBUF1+	AINBUF1−	0x1320	RW
		[7:0]	BURNOUT_EN1	RESERVED	REF_SEL1		RESERVED					
0x22	SETUPCON2	[15:8]	RESERVED			BI_UNIPOLAR2	REFBUF2+	REFBUF2−	AINBUF2+	AINBUF2−	0x1320	RW
		[7:0]	BURNOUT_EN2	RESERVED	REF_SEL2		RESERVED					
0x23	SETUPCON3	[15:8]	RESERVED			BI_UNIPOLAR3	REFBUF3+	REFBUF3−	AINBUF3+	AINBUF3−	0x1320	RW
		[7:0]	BURNOUT_EN3	RESERVED	REF_SEL3		RESERVED					
0x24	SETUPCON4	[15:8]	RESERVED			BI_UNIPOLAR4	REFBUF4+	REFBUF4−	AINBUF4+	AINBUF4−	0x1320	RW
		[7:0]	BURNOUT_EN4	RESERVED	REF_SEL4		RESERVED					

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x25	SETUPCON5	[15:8]	RESERVED			BI_UNIPOLAR5	REFBUF5+	REFBUF5−	AINBUF5+	AINBUF5−	0x1320	RW
		[7:0]	BURNOUT_EN5	RESERVED	REF_SEL5		RESERVED					
0x26	SETUPCON6	[15:8]	RESERVED			BI_UNIPOLAR6	REFBUF6+	REFBUF6−	AINBUF6+	AINBUF6−	0x1320	RW
		[7:0]	BURNOUT_EN6	RESERVED	REF_SEL6		RESERVED					
0x27	SETUPCON7	[15:8]	RESERVED			BI_UNIPOLAR7	REFBUF7+	REFBUF7−	AINBUF7+	AINBUF7−	0x1320	RW
		[7:0]	BURNOUT_EN7	RESERVED	REF_SEL7		RESERVED					
0x28	FILTCON0	[15:8]	SINC3_MAP0	RESERVED			ENHFILTEN0	ENHFILT0			0x0500	RW
		[7:0]	RESERVED	ORDER0		ODR0						
0x29	FILTCON1	[15:8]	SINC3_MAP1	RESERVED			ENHFILTEN1	ENHFILT1			0x0500	RW
		[7:0]	RESERVED	ORDER1		ODR1						
0x2A	FILTCON2	[15:8]	SINC3_MAP2	RESERVED			ENHFILTEN2	ENHFILT2			0x0500	RW
		[7:0]	RESERVED	ORDER2		ODR2						
0x2B	FILTCON3	[15:8]	SINC3_MAP3	RESERVED			ENHFILTEN3	ENHFILT3			0x0500	RW
		[7:0]	RESERVED	ORDER3		ODR3						
0x2C	FILTCON4	[15:8]	SINC3_MAP4	RESERVED			ENHFILTEN4	ENHFILT4			0x0500	RW
		[7:0]	RESERVED	ORDER4		ODR4						
0x2D	FILTCON5	[15:8]	SINC3_MAP5	RESERVED			ENHFILTEN5	ENHFILT5			0x0500	RW
		[7:0]	RESERVED	ORDER5		ODR5						
0x2E	FILTCON6	[15:8]	SINC3_MAP6	RESERVED			ENHFILTEN6	ENHFILT6			0x0500	RW
		[7:0]	RESERVED	ORDER6		ODR6						
0x2F	FILTCON7	[15:8]	SINC3_MAP7	RESERVED			ENHFILTEN7	ENHFILT7			0x0500	RW
		[7:0]	RESERVED	ORDER7		ODR7						
0x30	OFFSET0	[23:0]	OFFSET0[23:0]								0x800000	RW
0x31	OFFSET1	[23:0]	OFFSET1[23:0]								0x800000	RW
0x32	OFFSET2	[23:0]	OFFSET2[23:0]								0x800000	RW
0x33	OFFSET3	[23:0]	OFFSET3[23:0]								0x800000	RW
0x34	OFFSET4	[23:0]	OFFSET4[23:0]								0x800000	RW
0x35	OFFSET5	[23:0]	OFFSET5[23:0]								0x800000	RW
0x36	OFFSET6	[23:0]	OFFSET6[23:0]								0x800000	RW
0x37	OFFSET7	[23:0]	OFFSET7[23:0]								0x800000	RW
0x38	GAIN0	[23:0]	GAIN0[23:0]								0x5XXXX0	RW
0x39	GAIN1	[23:0]	GAIN1[23:0]								0x5XXXX0	RW
0x3A	GAIN2	[23:0]	GAIN2[23:0]								0x5XXXX0	RW
0x3B	GAIN3	[23:0]	GAIN3[23:0]								0x5XXXX0	RW
0x3C	GAIN4	[23:0]	GAIN4[23:0]								0x5XXXX0	RW
0x3D	GAIN5	[23:0]	GAIN5[23:0]								0x5XXXX0	RW
0x3E	GAIN6	[23:0]	GAIN6[23:0]								0x5XXXX0	RW
0x3F	GAIN7	[23:0]	GAIN7[23:0]								0x5XXXX0	RW

REGISTER DETAILS

COMMUNICATIONS REGISTER

Address: 0x00, Reset: 0x00, Name: COMMS

All access to the on-chip registers must start with a write to the communications register. This write determines what register is accessed next and whether that operation is a write or a read.

Table 25. Bit Descriptions for COMMS

Bits	Bit Name	Settings	Description	Reset	Access
7	$\overline{\text{WEN}}$		This bit must be low to begin communications with the ADC.	0x0	W
6	R/$\overline{\text{W}}$		This bit determines if the command is a read or write operation.	0x0	W
		0	Write command		
		1	Read command		
[5:0]	RA		The register address bits determine which register is to be read from or written to as part of the current communication.	0x00	W
		000000	Status register		
		000001	ADC mode register		
		000010	Interface mode register		
		000011	Register checksum register		
		000100	Data register		
		000110	GPIO configuration register		
		000111	ID register		
		010000	Channel 0 register		
		010001	Channel 1 register		
		010010	Channel 2 register		
		010011	Channel 3 register		
		010100	Channel 4 register		
		010101	Channel 5 register		
		010110	Channel 6 register		
		010111	Channel 7 register		
		011000	Channel 8 register		
		011001	Channel 9 register		
		011010	Channel 10 register		
		011011	Channel 11 register		
		011100	Channel 12 register		
		011101	Channel 13 register		
		011110	Channel 14 register		
		011111	Channel 15 register		
		100000	Setup Configuration 0 register		
		100001	Setup Configuration 1 register		
		100010	Setup Configuration 2 register		
		100011	Setup Configuration 3 register		
		100100	Setup Configuration 4 register		
		100101	Setup Configuration 5 register		
		100110	Setup Configuration 6 register		
		100111	Setup Configuration 7 register		
		101000	Filter Configuration 0 register		
		101001	Filter Configuration 1 register		
		101010	Filter Configuration 2 register		
		101011	Filter Configuration 3 register		
		101100	Filter Configuration 4 register		
		101101	Filter Configuration 5 register		
		101110	Filter Configuration 6 register		
		101111	Filter Configuration 7 register		

Bits	Bit Name	Settings	Description	Reset	Access
		110000	Offset 0 register		
		110001	Offset 1 register		
		110010	Offset 2 register		
		110011	Offset 3 register		
		110100	Offset 4 register		
		110101	Offset 5 register		
		110110	Offset 6 register		
		110111	Offset 7 register		
		111000	Gain 0 register		
		111001	Gain 1 register		
		111010	Gain 2 register		
		111011	Gain 3 register		
		111100	Gain 4 register		
		111101	Gain 5 register		
		111110	Gain 6 register		
		111111	Gain 7 register		

STATUS REGISTER

Address: 0x00, Reset: 0x80, Name: STATUS

The status register is an 8-bit register that contains ADC and serial interface status information. It can optionally be appended to the data register by setting the DATA_STAT bit in the interface mode register.

Table 26. Bit Descriptions for STATUS

Bits	Bit Name	Settings	Description	Reset	Access
7	$\overline{RDY}$		The status of $\overline{RDY}$ is output to the DOUT/$\overline{RDY}$ pin whenever $\overline{CS}$ is low and a register is not being read. This bit goes low when the ADC has written a new result to the data register. In ADC calibration modes, this bit goes low when the ADC has written the calibration result. $\overline{RDY}$ is brought high automatically by a read of the data register.	0x1	R
		0	New data result available		
		1	Awaiting new data result		
6	ADC_ERROR		This bit by default indicates if an ADC overrange or underrange has occurred. The ADC result is clamped to 0xFFFFFF for overrange errors and 0x000000 for underrange errors. This bit is updated when the ADC result is written and is cleared at the next update after removing the overrange or underrange condition.	0x0	R
		0	No error		
		1	Error		
5	CRC_ERROR		This bit indicates if a CRC error has taken place during a register write. For register reads, the host microcontroller determines if a CRC error has occurred. This bit is cleared by a read of this register.	0x0	R
		0	No error		
		1	CRC error		
4	REG_ERROR		This bit indicates if the content of one of the internal registers has changed from the value calculated when the register integrity check was activated. The check is activated by setting the REG_CHECK bit in the interface mode register. This bit is cleared by clearing the REG_CHECK bit.	0x0	R
		0	No error		
		1	Error		
[3:0]	CHANNEL		These bits indicate which channel was active for the ADC conversion whose result is currently in the data register. This may be different from the channel currently being converted. The mapping is a direct map from the channel register; therefore, Channel 0 results in 0x0 and Channel 15 results in 0xF.	0x0	R
		0000	Channel 0		
		0001	Channel 1		
		0010	Channel 2		
		0011	Channel 3		
		0100	Channel 4		
		0101	Channel 5		
		0110	Channel 6		
		0111	Channel 7		
		1000	Channel 8		
		1001	Channel 9		
		1010	Channel 10		
		1011	Channel 11		
		1100	Channel 12		
		1101	Channel 13		
		1110	Channel 14		
		1111	Channel 15		

ADC MODE REGISTER

Address: 0x01, Reset: 0xA000, Name: ADCMODE

The ADC mode register controls the operating mode of the ADC and the master clock selection. A write to the ADC mode register resets the filter and the $\overline{RDY}$ bits and starts a new conversion or calibration.

Table 27. Bit Descriptions for ADCMODE

Bits	Bit Name	Settings	Description	Reset	Access
15	REF_EN		Enables internal reference and outputs a buffered 2.5 V to the REFOUT pin.	0x1	RW
		0	Disabled		
		1	Enabled		
14	HIDE_DELAY		If a programmable delay is set using the delay bits, this bit allows the delay to be hidden by absorbing the delay into the conversion time for selected data rates with the sinc5 + sinc1 filter. See the Delay section for more information.	0x0	RW
		0	Enabled		
		1	Disabled		
13	SING_CYC		This bit can be used when only a single channel is active to set the ADC to only output at the settled filter data rate.	0x1	RW
		0	Disabled		
		1	Enabled		
[12:11]	RESERVED		These bits are reserved; set these bits to 0.	0x0	R
[10:8]	DELAY		These bits allow a programmable delay to be added after a channel switch to allow the settling of external circuitry before the ADC starts processing its input.	0x0	RW
		000	0 µs		
		001	4 µs		
		010	16 µs		
		011	40 µs		
		100	100 µs		
		101	200 µs		
		110	500 µs		
		111	1 ms		
7	RESERVED		This bit is reserved; set this bit to 0.	0x0	R
[6:4]	MODE		These bits control the operating mode of the ADC. See the Operating Modes section for more information.	0x0	RW
		000	Continuous conversion mode		
		001	Single conversion mode		
		010	Standby mode		
		011	Power-down mode		
		100	Internal offset calibration		
		110	System offset calibration		
		111	System gain calibration		
[3:2]	CLOCKSEL		These bits are used to select the ADC clock source. Selecting the internal oscillator also enables the internal oscillator.	0x0	RW
		00	Internal oscillator		
		01	Internal oscillator output on the XTAL2/CLKIO pin		
		10	External clock input on the XTAL2/CLKIO pin		
		11	External crystal on the XTAL1 and XTAL2/CLKIO pins		
[1:0]	RESERVED		These bits are reserved; set these bits to 0.	0x0	R

INTERFACE MODE REGISTER

Address: 0x02, Reset: 0x0000, Name: IFMODE

The interface mode register configures various serial interface options.

Table 28. Bit Descriptions for IFMODE

Bits	Bit Name	Settings	Description	Reset	Access
[15:13]	RESERVED		These bits are reserved; set these bits to 0.	0x0	R
12	ALT_SYNC		This bit enables a different behavior of the SYNC pin to allow the use of SYNC as a control for conversions when cycling channels (see the description of the SYNC_EN bit in the GPIO Configuration Register section for details).	0x0	RW
		0	Disabled		
		1	Enabled		
11	IOSTRENGTH		This bit controls the drive strength of the DOUT/RDY pin. Set this bit when reading from the serial interface at high speed with a low IOVDD supply and moderate capacitance.	0x0	RW
		0	Disabled (default)		
		1	Enabled		
[10:9]	RESERVED		These bits are reserved; set these bits to 0.	0x0	R
8	DOUT_RESET		See the DOUT_RESET section for more information.	0x0	RW
		0	Disabled		
		1	Enabled		
7	CONTREAD		This bit enables the continuous read mode of the ADC data register. The ADC must be configured in continuous conversion mode to use continuous read mode. For more details, see the Operating Modes section.	0x0	RW
		0	Disabled		
		1	Enabled		
6	DATA_STAT		This bit enables the status register to be appended to the data register when read so that channel and status information are transmitted with the data. This is the only way to be sure that the channel bits read from the status register correspond to the data in the data register.	0x0	RW
		0	Disabled		
		1	Enabled		
5	REG_CHECK		This bit enables a register integrity checker, which can be used to monitor any change in the value of the user registers. To use this feature, configure all other registers as desired with this bit cleared. Then write to this register to set the REG_CHECK bit to 1. If the contents of any of the registers change, the REG_ERROR bit is set in the status register. To clear the error, set the REG_CHECK bit to 0. Neither the interface mode register nor the ADC data or status registers are included in the registers that are checked. If a register must have a new value written, this bit must first be cleared; otherwise, an error is flagged when the new register contents are written.	0x0	RW
		0	Disabled		
		1	Enabled		
4	RESERVED		This bit is reserved; set this bit to 0.	0x0	R
[3:2]	CRC_EN		These bits enable CRC protection of register reads/writes. CRC increases the number of bytes in a serial interface transfer by one. See the CRC Calculation section for more details.	0x00	RW
		00	Disabled		
		01	XOR checksum enabled for register read transactions; register writes still use CRC with these bits set		
		10	CRC checksum enabled for read and write transactions		
1	RESERVED		This bit is reserved; set this bit to 0.	0x0	R

Bits	Bit Name	Settings	Description	Reset	Access
0	WL16		This bit changes the ADC data register to 16 bits. The ADC is not reset by a write to the interface mode register; therefore, the ADC result is not rounded to the correct word length immediately after writing to these bits. The first new ADC result is correct.	0x0	RW
		0	24-bit data		
		1	16-bit data		

REGISTER CHECK

Address: 0x03, Reset: 0x000000, Name: REGCHECK

The register check register is a 24-bit checksum calculated by exclusively OR'ing the contents of the user registers. The REG_CHECK bit in the interface mode register must be set for this to operate; otherwise, the register reads 0.

Table 29. Bit Descriptions for REGCHECK

Bits	Bit Name	Settings	Description	Reset	Access
[23:0]	REGISTER_CHECK		This register contains the 24-bit checksum of user registers when the REG_CHECK bit is set in the interface mode register.	0x000000	R

DATA REGISTER

Address: 0x04, Reset: 0x000000, Name: DATA

The data register contains the ADC conversion result. The encoding is offset binary, or it can be changed to unipolar by the BI_UNIPOLARx bits in the setup configuration registers. Reading the data register brings the $\overline{\text{RDY}}$ bit and the $\overline{\text{RDY}}$ output high if it is low. The ADC result can be read multiple times; however, because the $\overline{\text{RDY}}$ output is brought high, it is not possible to know if another ADC result is imminent. After the command to read the ADC register is received, the ADC does not write a new result into the data register.

Table 30. Bit Descriptions for DATA

Bits	Bit Name	Settings	Description	Reset	Access
[23:0]	DATA		This register contains the ADC conversion result. If DATA_STAT is set in the interface mode register, the status register is appended to this register when read, making this a 32-bit register. If WL16 is set in the interface mode register, this register is reduced to 16 bits.	0x000000	R

GPIO CONFIGURATION REGISTER

Address: 0x06, Reset: 0x0800, Name: GPIOCON

The GPIO configuration register controls the general-purpose I/O pins of the ADC.

Table 31. Bit Descriptions for GPIOCON

Bits	Bit Name	Settings	Description	Reset	Access
15	RESERVED		These bits are reserved; set these bits to 0.	0x0	R
14	PDSW		This bit enables/disables the power-down switch function. Setting the bit allows the pin to sink current. This function can be used for bridge sensor applications where the switch controls the power-up/power-down of the bridge.	0x0	RW
13	OP_EN2_3		This bit enables the GPO2 and GPO3 pins. Outputs are referenced between AVDD1 and AVSS.	0x0	RW
12	MUX_IO		This bit allows the ADC to control an external multiplexer, using GPIO0/GPIO1/GPO2/GPO3 in sync with the internal channel sequencing. The analog input pins used for a channel can still be selected on a per channel basis. Therefore, it is possible to have a 16-channel multiplexer in front of each analog input pair (AIN0/AIN1 to AIN14/AIN15), giving a total of 128 differential channels. However, only 16 channels at a time can be automatically sequenced. Following the sequence of 16 channels, the user changes the analog input to the next pair of input channels, and it sequences through the next 16 channels. A delay can be inserted after switching an external multiplexer (see the delay bits in the ADC Mode Register section).	0x0	RW
11	SYNC_EN		This bit enables the $\overline{\text{SYNC}}$ pin as a synchronization input. When the pin is low, this holds the ADC and filter in reset until the $\overline{\text{SYNC}}$ pin goes high. An alternative operation of the $\overline{\text{SYNC}}$ pin is available when the ALT_SYNC bit in the interface mode register is set. This mode only works when multiple channels are enabled. In this case, a low on the $\overline{\text{SYNC}}$ pin does not immediately reset the filter/modulator. Instead, if the $\overline{\text{SYNC}}$ pin is low when the channel is due to be switched, the modulator and filter are prevented from starting a new conversion. Bringing $\overline{\text{SYNC}}$ high begins the next conversion. This alternative sync mode allows $\overline{\text{SYNC}}$ to be used while cycling through channels.	0x1	RW
		0	Disabled.		
		1	Enabled.		
[10:9]	ERR_EN		These bits enable the $\overline{\text{ERROR}}$ pin as an error input/output.	0x0	RW
		00	Disabled.		
		01	$\overline{\text{ERROR}}$ is an error input. The (inverted) readback state is OR'ed with other error sources and is available in the ADC_ERROR bit in the status register. The $\overline{\text{ERROR}}$ pin state can also be read from the ERR_DAT bit in this register.		
		10	$\overline{\text{ERROR}}$ is an open-drain error output. The status register error bits are OR'ed, inverted, and mapped to the $\overline{\text{ERROR}}$ pin. The $\overline{\text{ERROR}}$ pins of multiple devices can be wired together to a common pull-up resistor so that an error on any device can be observed.		
		11	$\overline{\text{ERROR}}$ is a general-purpose output. The status of the pin is controlled by the ERR_DAT bit in this register. This output is referenced between IOVDD and DGND, as opposed to the AVDD1 and AVSS levels used by the general-purpose I/O pins. The $\overline{\text{ERROR}}$ pin has an active pull-up in this case.		
8	ERR_DAT		This bit determines the logic level at the $\overline{\text{ERROR}}$ pin if the pin is enabled as a general-purpose output. This bit reflects the readback status of the pin if the pin is enabled as an input.	0x0	RW
7	GP_DATA3		This bit is the write data for GPO3.	0x0	W
6	GP_DATA2		This bit is the write data for GPO2.	0x0	W
5	IP_EN1		This bit turns GPIO1 into an input. Inputs are referenced to AVDD1 or AVSS.	0x0	RW
		0	Disabled.		
		1	Enabled.		
4	IP_EN0		This bit turns GPIO0 into an input. Inputs are referenced to AVDD1 or AVSS.	0x0	RW
		0	Disabled.		
		1	Enabled.		

Bits	Bit Name	Settings	Description	Reset	Access
3	OP_EN1		This bit turns GPIO1 into an output. Outputs are referenced between AVDD1 and AVSS.	0x0	RW
		0	Disabled.		
		1	Enabled.		
2	OP_EN0		This bit turns GPIO0 into an output. Outputs are referenced between AVDD1 and AVSS.	0x0	RW
		0	Disabled.		
		1	Enabled.		
1	GP_DATA1		This bit is the readback or write data for GPIO1.	0x0	RW
0	GP_DATA0		This bit is the readback or write data for GPIO0.	0x0	RW

ID REGISTER

Address: 0x07, Reset: 0x3CDx, Name: ID

The ID register returns a 16-bit ID. For the AD7175-8, this ID is 0x3CDx.

Table 32. Bit Descriptions for ID

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	ID		The ID register returns a 16-bit ID code that is specific to the ADC.	0x3CDx	R
		0x3CDx	AD7175-8		

CHANNEL REGISTER 0

Address: 0x10, Reset: 0x8001, Name: CH0

The channel registers are 16-bit registers used to select which channels are currently active, which inputs are selected for each channel, and which setup is used to configure the ADC for that channel.

Table 33. Bit Descriptions for CH0

Bits	Bit Name	Settings	Description	Reset	Access
15	CH_EN0		This bit enables Channel 0. If more than one channel is enabled, the ADC automatically sequences between them.	0x1	RW
		0	Disabled		
		1	Enabled (default)		
[14:12]	SETUP_SEL0		These bits identify which of the eight setups is used to configure the ADC for this channel. A setup comprises a set of four registers: setup configuration register, filter configuration register, offset register, and gain register. All channels can use the same setup, in which case the same 3-bit value must be written to these bits on all active channels, or up to eight channels can be configured differently.	0x0	RW
		000	Setup 0		
		001	Setup 1		
		010	Setup 2		
		011	Setup 3		
		100	Setup 4		
		101	Setup 5		
		110	Setup 6		
		111	Setup 7		
[11:10]	RESERVED		These bits are reserved; set these bits to 0.	0x0	R
[9:5]	AINPOS0		These bits select which input is connected to the positive input of the ADC for this channel.	0x0	RW
		00000	AIN0 (default)		
		00001	AIN1		
		00010	AIN2		
		00011	AIN3		
		00100	AIN4		
		00101	AIN5		
		00110	AIN6		
		00111	AIN7		

Bits	Bit Name	Settings	Description	Reset	Access
		01000	AIN8		
		01001	AIN9		
		01010	AIN10		
		01011	AIN11		
		01100	AIN12		
		01101	AIN13		
		01110	AIN14		
		01111	AIN15		
		10000	AIN16		
		10001	Temperature sensor+		
		10010	Temperature sensor−		
		10011	((AVDD1 − AVSS)/5)+ (analog input buffers must be enabled)		
		10100	((AVDD1 − AVSS)/5)− (analog input buffers must be enabled)		
		10101	REF+		
		10110	REF−		
[4:0]	AINNEG0		These bits select which input is connected to the negative input of the ADC for this channel.	0x1	RW
		00000	AIN0		
		00001	AIN1 (default)		
		00010	AIN2		
		00011	AIN3		
		00100	AIN4		
		00101	AIN5		
		00110	AIN6		
		00111	AIN7		
		01000	AIN8		
		01001	AIN9		
		01010	AIN10		
		01011	AIN11		
		01100	AIN12		
		01101	AIN13		
		01110	AIN14		
		01111	AIN15		
		10000	AIN16		
		10001	Temperature sensor+		
		10010	Temperature sensor−		
		10011	((AVDD1 − AVSS)/5)+		
		10100	((AVDD1 − AVSS)/5)−		
		10101	REF+		
		10110	REF−		

CHANNEL REGISTER 1 TO CHANNEL REGISTER 15

Address: 0x11 to 0x1F, Reset: 0x0001, Name: CH1 to CH7

The remaining 15 channel registers share the same layout as Channel Register 0.

Table 34. CH1 to CH15 Register Map

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x11	CH1	[15:8]	CH_EN1	SETUP_SEL1			RESERVED		AINPOS1[4:3]		0x0001	RW
		[7:0]	AINPOS1[2:0]			AINNEG1						
0x12	CH2	[15:8]	CH_EN2	SETUP_SEL2			RESERVED		AINPOS2[4:3]		0x0001	RW
		[7:0]	AINPOS2[2:0]			AINNEG2						
0x13	CH3	[15:8]	CH_EN3	SETUP_SEL3			RESERVED		AINPOS3[4:3]		0x0001	RW
		[7:0]	AINPOS3[2:0]			AINNEG3						
0x14	CH4	[15:8]	CH_EN4	SETUP_SEL4			RESERVED		AINPOS4[4:3]		0x0001	RW
		[7:0]	AINPOS4[2:0]			AINNEG4						
0x15	CH5	[15:8]	CH_EN5	SETUP_SEL5			RESERVED		AINPOS5[4:3]		0x0001	RW
		[7:0]	AINPOS5[2:0]			AINNEG5						
0x16	CH6	[15:8]	CH_EN6	SETUP_SEL6			RESERVED		AINPOS6[4:3]		0x0001	RW
		[7:0]	AINPOS6[2:0]			AINNEG6						
0x17	CH7	[15:8]	CH_EN7	SETUP_SEL7			RESERVED		AINPOS7[4:3]		0x0001	RW
		[7:0]	AINPOS7[2:0]			AINNEG7						
0x18	CH8	[15:8]	CH_EN8	SETUP_SEL8			RESERVED		AINPOS8[4:3]		0x0001	RW
		[7:0]	AINPOS8[2:0]			AINNEG8						
0x19	CH9	[15:8]	CH_EN9	SETUP_SEL9			RESERVED		AINPOS9[4:3]		0x0001	RW
		[7:0]	AINPOS9[2:0]			AINNEG9						
0x1A	CH10	[15:8]	CH_EN10	SETUP_SEL10			RESERVED		AINPOS10[4:3]		0x0001	RW
		[7:0]	AINPOS10[2:0]			AINNEG10						
0x1B	CH11	[15:8]	CH_EN11	SETUP_SEL11			RESERVED		AINPOS11[4:3]		0x0001	RW
		[7:0]	AINPOS11[2:0]			AINNEG11						
0x1C	CH12	[15:8]	CH_EN12	SETUP_SEL12			RESERVED		AINPOS12[4:3]		0x0001	RW
		[7:0]	AINPOS12[2:0]			AINNEG12						
0x1D	CH13	[15:8]	CH_EN13	SETUP_SEL13			RESERVED		AINPOS13[4:3]		0x0001	RW
		[7:0]	AINPOS13[2:0]			AINNEG13						
0x1E	CH14	[15:8]	CH_EN14	SETUP_SEL14			RESERVED		AINPOS14[4:3]		0x0001	RW
		[7:0]	AINPOS14[2:0]			AINNEG14						
0x1F	CH15	[15:8]	CH_EN15	SETUP_SEL15			RESERVED		AINPOS15[4:3]		0x0001	RW
		[7:0]	AINPOS15[2:0]			AINNEG15						

SETUP CONFIGURATION REGISTER 0

Address: 0x20, Reset: 0x1320, Name: SETUPCON0

The setup configuration registers are 16-bit registers that configure the reference selection, input buffers, and output coding of the ADC.

Table 35. Bit Descriptions for SETUPCON0

Bits	Bit Name	Settings	Description	Reset	Access
[15:13]	RESERVED		These bits are reserved; set these bits to 0.	0x0	R
12	BI_UNIPOLAR0		This bit sets the output coding of the ADC for Setup 0.	0x1	RW
		0	Unipolar coded output		
		1	Bipolar coded output (offset binary)		
11	REFBUF0+		This bit enables or disables the REF+ input buffer.	0x0	RW
		0	REF+ buffer disabled		
		1	REF+ buffer enabled		
10	REFBUF0−		This bit enables or disables the REF− input buffer.	0x0	RW
		0	REF− buffer disabled		
		1	REF− buffer enabled		
9	AINBUF0+		This bit enables or disables the AIN+ input buffer.	0x1	RW
		0	AIN+ buffer disabled		
		1	AIN+ buffer enabled		
8	AINBUF0−		This bit enables or disables the AIN− input buffer.	0x1	RW
		0	AIN− buffer disabled		
		1	AIN− buffer enabled		
7	BURNOUT_EN0		This bit enables a 10 μA current source on the positive analog input selected and a 10 μA current sink on the negative analog input selected. The burnout currents are useful in diagnosis of an open wire, whereby the ADC result goes to full scale. Enabling the burnout currents during measurement results in an offset voltage on the ADC. This means the strategy for diagnosing an open wire operates best by turning on the burnout currents at intervals, before or after precision measurements.	0x00	R
6	RESERVED		These bits are reserved; set these bits to 0.	0x00	R
[5:4]	REF_SEL0		These bits allow the user to select the reference source for ADC conversion on Setup 0.	0x2	RW
		00	External reference.		
		01	External Reference 2 supplied to AIN1/REF2+ and AIN0/REF2− pins.		
		10	Internal 2.5 V reference. This must also be enabled in the ADC mode register.		
		11	AVDD1 − AVSS. This can be used to as a diagnostic to validate other reference values.		
[3:0]	RESERVED		These bits are reserved; set these bits to 0.	0x0	R

SETUP CONFIGURATION REGISTER 1 TO SETUP CONFIGURATION REGISTER 7

Address: 0x21 to 0x27, Reset: 0x1320, Name: SETUPCON1 to SETUPCON7

The remaining seven setup configuration registers share the same layout as Setup Configuration Register 0.

Table 36. SETUPCON1 to SETUPCON7 Register Map

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x21	SETUPCON1	[15:8]	RESERVED			BI_UNIPOLAR1	REFBUF1+	REFBUF1–	AINBUF1+	AINBUF1–	0x1320	RW
		[7:0]	BURNOUT_EN1	RESERVED	REF_SEL1		RESERVED					
0x22	SETUPCON2	[15:8]	RESERVED			BI_UNIPOLAR2	REFBUF2+	REFBUF2–	AINBUF2+	AINBUF2–	0x1320	RW
		[7:0]	BURNOUT_EN2	RESERVED	REF_SEL2		RESERVED					
0x23	SETUPCON3	[15:8]	RESERVED			BI_UNIPOLAR3	REFBUF3+	REFBUF3–	AINBUF3+	AINBUF3–	0x1320	RW
		[7:0]	BURNOUT_EN3	RESERVED	REF_SEL3		RESERVED					
0x24	SETUPCON4	[15:8]	RESERVED			BI_UNIPOLAR4	REFBUF4+	REFBUF4–	AINBUF4+	AINBUF4–	0x1320	RW
		[7:0]	BURNOUT_EN4	RESERVED	REF_SEL4		RESERVED					
0x25	SETUPCON5	[15:8]	RESERVED			BI_UNIPOLAR5	REFBUF5+	REFBUF5–	AINBUF5+	AINBUF5–	0x1320	RW
		[7:0]	BURNOUT_EN5	RESERVED	REF_SEL5		RESERVED					
0x26	SETUPCON6	[15:8]	RESERVED			BI_UNIPOLAR6	REFBUF6+	REFBUF6–	AINBUF6+	AINBUF6–	0x1320	RW
		[7:0]	BURNOUT_EN6	RESERVED	REF_SEL6		RESERVED					
0x27	SETUPCON7	[15:8]	RESERVED			BI_UNIPOLAR7	REFBUF7+	REFBUF7–	AINBUF7+	AINBUF7–	0x1320	RW
		[7:0]	BURNOUT_EN7	RESERVED	REF_SEL7		RESERVED					

FILTER CONFIGURATION REGISTER 0

Address: 0x28, Reset: 0x0500, Name: FILTCON0

The filter configuration registers are 16-bit registers that configure the ADC data rate and filter options. Writing to any of these registers resets any active ADC conversion and restarts converting at the first channel in the sequence.

Table 37. Bit Descriptions for FILTCON0

Bits	Bit Name	Settings	Description	Reset	Access
15	SINC3_MAP0		If this bit is set, the mapping of the filter register changes to directly program the decimation rate of the sinc3 filter for Setup 0. All other options are eliminated. This allows fine tuning of the output data rate and filter notch for rejection of specific frequencies. The data rate when on a single channel equals $f_{MOD}/(32 \times FILTCON0[14:0])$.	0x0	RW
[14:12]	RESERVED		These bits are reserved; set these bits to 0.	0x0	R
11	ENHFILTEN0		This bit enables various postfilters for enhanced 50 Hz/60 Hz rejection for Setup 0. The ORDER0 bits must be set to 00 to select the sinc5 + sinc1 filter for this to work.	0x0	RW
		0	Disabled		
		1	Enabled		
[10:8]	ENHFILT0		These bits select between various postfilters for enhanced 50 Hz/60 Hz rejection for Setup 0.	0x5	RW
		010	27 SPS, 47 dB rejection, 36.7 ms settling		
		011	25 SPS, 62 dB rejection, 40 ms settling		
		101	20 SPS, 86 dB rejection, 50 ms settling		
		110	16.67 SPS, 92 dB rejection, 60 ms settling		
7	RESERVED		This bit is reserved; set this bit to 0.	0x0	R
[6:5]	ORDER0		These bits control the order of the digital filter that processes the modulator data for Setup 0.	0x0	RW
		00	Sinc5 + sinc1 (default)		
		11	Sinc3		
[4:0]	ODR0		These bits control the output data rate of the ADC and, therefore, the settling time and noise for Setup 0. Rates shown are for the sinc5 + sinc 1 filter. See Table 19 to Table 22.	0x0	RW
		00000	250,000		
		00001	125,000		
		00010	62,500		
		00011	50,000		
		00100	31,250		
		00101	25,000		
		00110	15,625		
		00111	10,000		
		01000	5000		
		01001	2500		
		01010	1000		
		01011	500		
		01100	397.5		
		01101	200		
		01110	100		
		01111	59.92		
		10000	49.96		
		10001	20		
		10010	16.66		
		10011	10		
		10100	5		

FILTER CONFIGURATION REGISTER 1 TO FILTER CONFIGURATION REGISTER 7

Address: 0x29 to 0x2F, Reset: 0x0500, Name: FILTCON1 to FILTCON7

The remaining seven filter configuration registers share the same layout as Filter Configuration Register 0.

Table 38. FILTCON1 to FILTCON7 Register Map

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x29	FILTCON1	[15:8]	SINC3_MAP1	RESERVED			ENHFILTEN1	ENHFILT1			0x0500	RW
		[7:0]	RESERVED	ORDER1		ODR1						
0x2A	FILTCON2	[15:8]	SINC3_MAP2	RESERVED			ENHFILTEN2	ENHFILT2			0x0500	RW
		[7:0]	RESERVED	ORDER2		ODR2						
0x2B	FILTCON3	[15:8]	SINC3_MAP3	RESERVED			ENHFILTEN3	ENHFILT3			0x0500	RW
		[7:0]	RESERVED	ORDER3		ODR3						
0x2C	FILTCON4	[15:8]	SINC3_MAP4	RESERVED			ENHFILTEN4	ENHFILT4			0x0500	RW
		[7:0]	RESERVED	ORDER4		ODR4						
0x2D	FILTCON5	[15:8]	SINC3_MAP5	RESERVED			ENHFILTEN5	ENHFILT5			0x0500	RW
		[7:0]	RESERVED	ORDER5		ODR5						
0x2E	FILTCON6	[15:8]	SINC3_MAP6	RESERVED			ENHFILTEN6	ENHFILT6			0x0500	RW
		[7:0]	RESERVED	ORDER6		ODR6						
0x2F	FILTCON7	[15:8]	SINC3_MAP7	RESERVED			ENHFILTEN7	ENHFILT7			0x0500	RW
		[7:0]	RESERVED	ORDER7		ODR7						

OFFSET REGISTER 0

Address: 0x30, Reset: 0x800000, Name: OFFSET0

The offset (zero-scale) registers are 24-bit registers that can be used to compensate for any offset error in the ADC or in the system.

Table 39. Bit Descriptions for OFFSET0

Bits	Bit Name	Settings	Description	Reset	Access
[23:0]	OFFSET0		Offset calibration coefficient for Setup 0.	0x800000	RW

OFFSET REGISTER 1 TO OFFSET REGISTER 7

Address: 0x31 to 0x37, Reset: 0x800000, Name: OFFSET1 to OFFSET7

The remaining seven offset registers share the same layout as Offset Register 0.

Table 40. OFFSET1 to OFFSET7 Register Map

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x30	OFFSET0	[23:0]	OFFSET0[23:0]								0x800000	RW
0x31	OFFSET1	[23:0]	OFFSET1[23:0]								0x800000	RW
0x32	OFFSET2	[23:0]	OFFSET2[23:0]								0x800000	RW
0x33	OFFSET3	[23:0]	OFFSET3[23:0]								0x800000	RW
0x34	OFFSET4	[23:0]	OFFSET4[23:0]								0x800000	RW
0x35	OFFSET5	[23:0]	OFFSET5[23:0]								0x800000	RW
0x36	OFFSET6	[23:0]	OFFSET6[23:0]								0x800000	RW
0x37	OFFSET7	[23:0]	OFFSET7[23:0]								0x800000	RW

GAIN REGISTER 0

Address: 0x38, Reset: 0x5XXXX0, Name: GAIN0

The gain (full-scale) registers are 24-bit registers that can be used to compensate for any gain error in the ADC or in the system.

Table 41. Bit Descriptions for GAIN0

Bits	Bit Name	Settings	Description	Reset	Access
[23:0]	GAIN0		Gain calibration coefficient for Setup 0.	0x5XXXX0	RW

GAIN REGISTER 1 TO GAIN REGISTER 7

Address: 0x39 to 0x3F, Reset: 0x5XXXX0, Name: GAIN1 to GAIN7

The remaining seven gain registers share the same layout as Gain Register 0.

Table 42. GAIN1 to GAIN7 Register Map

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x38	GAIN0	[23:0]	GAIN0[23:0]								0x5XXXX0	RW
0x39	GAIN1	[23:0]	GAIN1[23:0]								0x5XXXX0	RW
0x3A	GAIN2	[23:0]	GAIN2[23:0]								0x5XXXX0	RW
0x3B	GAIN3	[23:0]	GAIN3[23:0]								0x5XXXX0	RW
0x3C	GAIN4	[23:0]	GAIN4[23:0]								0x5XXXX0	RW
0x3D	GAIN5	[23:0]	GAIN5[23:0]								0x5XXXX0	RW
0x3E	GAIN6	[23:0]	GAIN6[23:0]								0x5XXXX0	RW
0x3F	GAIN7	[23:0]	GAIN7[23:0]								0x5XXXX0	RW

OUTLINE DIMENSIONS

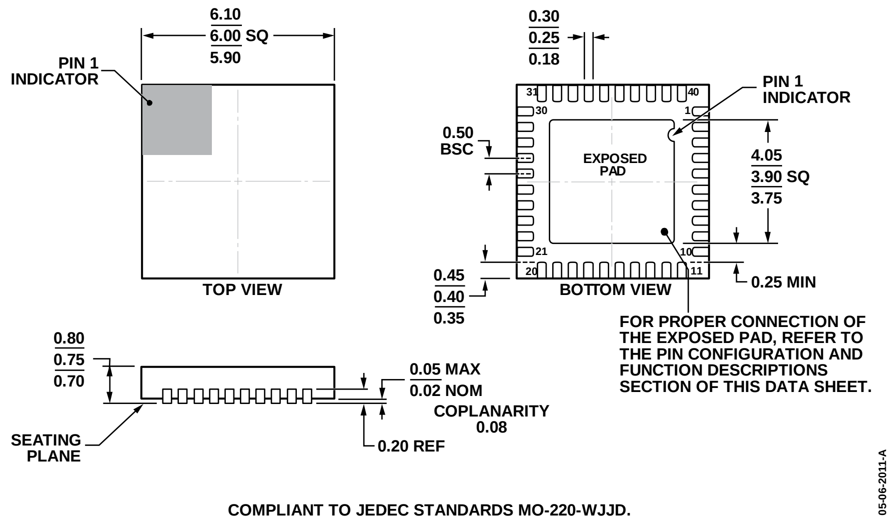


Figure 72. 40-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
6 mm × 6 mm Body, Very Very Thin Quad
(CP-40-14)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD7175-8BCPZ	−40°C to +105°C	40-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-40-14
AD7175-8BCPZ-RL	−40°C to +105°C	40-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-40-14
AD7175-8BCPZ-RL7	−40°C to +105°C	40-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-40-14

[1] Z = RoHS Compliant Part.