Synchronous, Step-Down DC-to-DC Controller with Voltage Tracking and Synchronization

Data Sheet

ADP1853

FEATURES

Input voltage range: 2.75 V to 20 V
Output voltage range: 0.6 V to 90% V_{IN}
Maximum output current of more than 25 A
Current mode architecture with current sense input
Configurable to voltage mode
±1% output voltage accuracy over temperature
Voltage tracking input
Programmable frequency: 200 kHz to 1.5 MHz
Synchronization input
Internal clock output
Power saving mode at light load
Precision enable input
Power good with internal pull-up resistor
Adjustable soft start
Programmable current sense gain
Integrated bootstrap diode
Starts into a precharged load
Externally adjustable slope compensation
Suitable for any output capacitor
Overvoltage and overcurrent-limit protection
Thermal overload protection
Input undervoltage lockout (UVLO)
Available in 20-lead, 4 mm × 4 mm LFCSP
Supported by ADIsimPower™ design tool

APPLICATIONS

Intermediate bus and POL systems requiring sequencing and tracking, including
Telecom base station and networking
Industrial and Instrumentation
Medical and healthcare

GENERAL DESCRIPTION

The ADP1853 is a wide range input, dc-to-dc, synchronous buck controller capable of running from commonly used 3.3 V to 12 V (up to 20 V) voltage inputs. The device nominally operates in current mode with valley current sensing providing the fastest step response for digital loads. It can also be configured as a voltage mode controller with low noise and crosstalk for sensitive loads.

The ADP1853 can be used as a master synchronization clock for the power system and for convenient synchronization between controllers. The CLKOUT signal can synchronize other devices in the ADP185x family such that slave devices are phase-shifted from the master to reduce the input ripple current, improve EMI, and reduce the size of the input bulk capacitance. The ADP1853 can also be configured as a slave device for current sharing. Additionally, the ADP1853 includes accurate tracking, precision enable, and power good functions for sequencing. The ADP1853 provides a high speed, high peak current gate driving capability to enable energy efficient power conversion. The device can be configured to operate in power saving mode by skipping pulses, reducing switching losses and improving efficiency at light load and standby conditions.

The accurate current limit allows design within a narrower range of tolerances and can reduce overall converter size and cost. The ADP1853 can regulate down to 0.6 V output using a high accuracy reference with ±1% tolerance over the temperature range from −40°C to 125°C.

With a wide range input voltage, the ADP1853 is designed to provide the designer with maximum flexibility for use in a variety of system configurations; loop compensation, soft start, frequency setting, power saving mode, current limit, and current sense gain can all be programmed using external components. In addition, the external RAMP resistor allows choosing optimal slope and V_{IN} feedforward in both current and voltage mode for excellent line rejection. The linear regulator and the boot strap diode for the high-side driver are internal.

Protection features include undervoltage lock out, overvoltage, overcurrent/short circuit, and overtemperature.

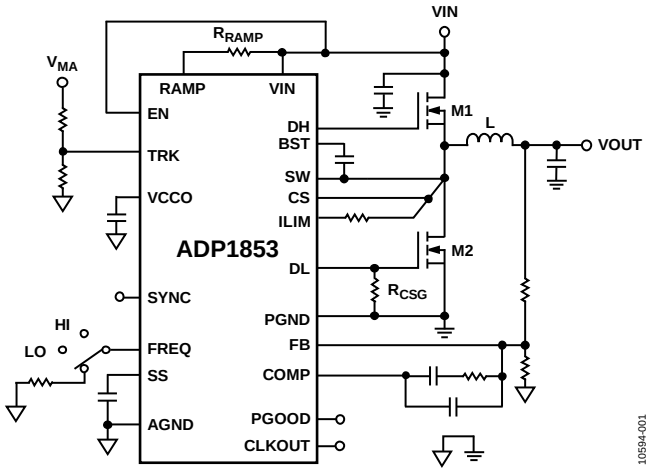


Figure 1. Typical Operation Circuit

Rev. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

ADP1853* Product Page Quick Links

Last Content Update: 11/01/2016

Comparable Parts

View a parametric search of comparable parts

Evaluation Kits

- ADP1853 Evalutaion Board

Documentation

Data Sheet

- ADP1853: Synchronous, Step-Down DC-to-DC Controller with Voltage Tracking and Synchronization Datasheet

User Guides

- UG-431: Evaluation Board for the ADP1853 Step-Down DC-to-DC Controller

Tools and Simulations

- ADIsimPower™ Voltage Regulator Design Tool
- ADP1851-53 Buck Designer Tool

Reference Materials

Press

- Analog Devices' DC-DC Switching Controller Features Current-mode and Voltage-mode Options for High-current Applications

Design Resources

- ADP1853 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

Discussions

View all ADP1853 EngineerZone Discussions

Sample and Buy

Visit the product page to see pricing options

Technical Support

Submit a technical question or find your regional support number

TABLE OF CONTENTS

REVISION HISTORY

5/12—Revision 0: Initial Version

SPECIFICATIONS

All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC). V_{IN} = 12 V. The specifications are valid for T_J = −40°C to +125°C, unless otherwise specified. Typical values are at T_A = 25°C.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY						
Input Voltage	V_{IN}		2.75		20	V
Undervoltage Lockout Threshold	$UVLO_{TRSH}$	V_{IN} rising	2.55	2.65	2.75	V
		V_{IN} falling	2.35	2.45	2.50	V
Undervoltage Lockout Hysteresis	$UVLO_{HYST}$			0.2		V
Quiescent Current	I_{IN}	EN = V_{IN} = 12 V, V_{FB} = V_{CCO} in forced pulse width modulation (PWM) mode (no switching)		4.2	5.7	mA
		EN = V_{IN} = 12 V, V_{FB} = V_{CCO} in PSM mode		2.5		mA
Shutdown Current	I_{IN_SD}	EN = GND, V_{IN} = 5.5 V or 20 V		100	200	µA
ERROR AMPLIFIER						
FB Input Bias Current	I_{FB}		−100	+1	+100	nA
Open-Loop Gain[1]				80		dB
Gain-Bandwidth Product[1]				20		MHz
TRK Input Bias Current	I_{TRK}	0 V ≤ V_{TRK} ≤ 5 V	−100	+1	+100	nA
CURRENT SENSE AMPLIFIER GAIN	A_{CS}	Gain resistor connected to DL, R_{CSG} = 47 kΩ ± 5%	2.6	3	3.4	V/V
		Gain resistor connected to DL, R_{CSG} = 22 kΩ ± 5%	5.2	6	6.8	V/V
		Default setting, R_{CSG} = open	10.5	12	13.5	V/V
		Voltage mode operation, resistor DL to PGND, R_{CSG} = 100 kΩ ± 5%		0		V/V
OUTPUT CHARACTERICTISTICS						
Feedback Accuracy Voltage	V_{FB}	T_J = −40°C to +85°C	597	600	603	mV
		T_J = −40°C to +125°C	594	600	606	mV
Line Regulation of PWM	$\Delta V_{FB}/\Delta V_{IN}$			±0.015		%/V
Load Regulation of PWM[1]	$\Delta V_{FB}/\Delta V_{COMP}$	V_{COMP} range = 0.9 V to 2.2 V		±0.3		%
OSCILLATOR						
Frequency	f_{OSC}	R_{FREQ} = 332 kΩ to AGND	170	200	230	kHz
		R_{FREQ} = 78.7 kΩ to AGND	720	800	880	kHz
		R_{FREQ} = 40.2 kΩ to AGND	1275	1500	1725	kHz
		FREQ to AGND	240	300	360	kHz
		FREQ to VCCO	480	600	720	kHz
SYNC Input Frequency Range[1]	f_{SYNC}	R_{FREQ} range from 332 kΩ to 40.2 kΩ	170		1725	kHz
SYNC Input Pulse Width[1]	$t_{SYNCMIN}$		100			ns
SYNC Pin Capacitance to GND	C_{SYNC}			5		pF
CLKOUT Frequency Range[1]	f_{CLKOUT}	f_{OSC} range from 170 kHz to 1725 kHz	170		1725	kHz
CLKOUT Pulse Duty Cycle	D_{CLKOUT}			50		%
CLKOUT Rise and Fall Time		C_{CLKOUT} = 47 pF		10		ns
LINEAR REGULATOR						
VCCO Output Voltage		I_{VCCO} = 100 mA	4.7	5.0	5.3	V
VCCO Load Regulation		I_{VCCO} = 0 mA to 100 mA		35		mV
VCCO Line Regulation		V_{IN} = 5.5 V to 20 V, I_{VCCO} = 20 mA		10		mV
VCCO Current Limit[1]		VCCO drops to 4 V from 5 V		350		mA
VCCO Short-Circuit Current[1]		VCCO < 0.5 V		370	400	mA
VIN to VCCO Dropout Voltage[2]	$V_{DROPOUT}$	I_{VCCO} = 100 mA, V_{IN} ≤ 5 V		0.33		V

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
LOGIC INPUTS						
EN		EN rising	0.57	0.63	0.68	V
EN Hysteresis				0.03		V
EN Input Leakage Current	I_{EN}	V_{IN} = 2.75 V to 20 V		1	200	nA
SYNC Logic Input Low					1.3	V
SYNC Logic Input High			1.9			V
SYNC Input Pull-Down Resistance	R_{SYNC}			1		MΩ
GATE DRIVERS						
DH Rise Time		C_{DH} = 3 nF, $V_{BST} - V_{SW}$ = 5 V		16		ns
DH Fall Time		C_{DH} = 3 nF, $V_{BST} - V_{SW}$ = 5 V		14		ns
DL Rise Time		C_{DL} = 3 nF		16		ns
DL Fall Time		C_{DL} = 3 nF		14		ns
DH to DL Dead Time		External 3 nF is connected to DH and DL		25		ns
DH or DL Driver R_{ON}, Sourcing Current[1]	R_{ON_SOURCE}	Sourcing 2 A with a 100 ns pulse		2		Ω
		Sourcing 1 A with a 100 ns pulse, V_{IN} = 3 V		2.3		Ω
DH or DL Driver R_{ON}, Tempco	TC_{RON}	V_{IN} = 3 V or 12 V		0.3		%/°C
DH or DL Driver R_{ON}, Sinking Current[1]	R_{ON_SINK}	Sinking 2 A with a 100 ns pulse		1.5		Ω
		Sinking 1 A with a 100 ns pulse, V_{IN} = 3 V		2		Ω
DH Maximum Duty Cycle[1]		f_{OSC} = 300 kHz	90			%
DH Maximum Duty Cycle[1]		f_{OSC} = 1500 kHz	50			%
Minimum DH On Time		f_{OSC} = 200 kHz to 1500 kHz			85	ns
Minimum DH Off Time		f_{OSC} = 200 kHz to 1500 kHz			345	ns
Minimum DL On Time		f_{OSC} = 200 kHz to 1500 kHz			295	ns
COMP VOLTAGE RANGE						
COMP Pulse Skip Threshold	$V_{COMP,THRES}$	In pulse skip mode (PSM)		0.9		V
COMP Clamp High Voltage	$V_{COMP,HIGH}$		2.2			V
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	T_{TMSD}			155		°C
Thermal Shutdown Hysteresis				20		°C
OVERVOLTAGE AND POWER GOOD THRESHOLDS						
FB Overvoltage Threshold	V_{OV}	V_{FB} rising	0.630	0.65	0.670	V
FB Overvoltage Hysteresis				18		mV
FB Undervoltage Threshold	V_{UV}	V_{FB} falling	0.525	0.55	0.575	V
FB Undervoltage Hysteresis				15		mV
TRK INPUT VOLTAGE RANGE[1]			0		5	V
FB TO TRK OFFSET VOLTAGE		TRK = 0.1 V to 0.57 V; offset = $V_{FB} - V_{TRK}$	−10	0	+10	mV
SOFT START						
SS Output Current	I_{SS}	During startup	4.6	6.5	8.4	µA
SS Pull-Down Resistor		During a fault condition		3		kΩ
FB to SS offset		V_{SS} = 0.1 V to 0.6 V; offset = $V_{FB} - V_{SS}$	−10		+10	mV

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
PGOOD						
PGOOD Pull-Up Resistor	R_{PGOOD}	Internal pull-up resistor to VCCO		12.5		kΩ
PGOOD Delay				12		µs
Overvoltage or Undervoltage Minimum Duration		This is the minimum duration required to trip the PGOOD signal		10		µs
ILIM Threshold Voltage[1]		Relative to PGND	−5	0	+5	mV
ILIM Output Current		ILIM = PGND	45	50	55	µA
Current Sense Blanking Period		After DL goes high, current limit is not sensed during this period		100		ns
INTEGRATED RECTIFIER (BOOST DIODE) RESISTANCE		At 20 mA forward current		16		Ω
ZERO CURRENT CROSS OFFSET (SW TO PGND)[1]		In pulse skip mode only; f_{OSC} = 300 kHz	0	2	4	mV

[1] Guaranteed by design.
[2] Connect V_{IN} to VCCO when V_{IN} < 5.5 V.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VIN, EN, RAMP	21 V
FB, COMP, SS, TRK, FREQ, SYNC, VCCO, PGOOD, CLKOUT	−0.3 V to +6 V
ILIM, SW, CS to PGND	−0.3 V to +21 V
BST, DH to PGND	−0.3 V to +28 V
DL to PGND	−0.3 V to VCCO + 0.3 V
BST to SW	−0.3 V to +6 V
BST to PGND to PGND 20 ns Transients	32 V
SW, CS to PGND 20 ns Transients	25 V
DL, SW, CS, ILIM to PGND 20 ns Negative Transients	−8 V
PGND to AGND	−0.3 V to +0.3 V
PGND to AGND 20 ns Transients	−8 V to +4 V
θ_{JA} (Natural Convection)[1, 2]	40°C/W
Operating Junction Temperature Range[3]	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Maximum Soldering Lead Temperature	260°C

[1] Measured with exposed pad attached to PCB.
[2] Junction-to-ambient thermal resistance (θ_{JA}) of the package was calculated or simulated on multilayer PCB.
[3] The junction temperature (T_J) of the device is dependent on the ambient temperature (T_A) the power dissipation of the device (P_D) and the junction to ambient thermal resistance of the package (θ_{JA}). Maximum junction temperature is calculated from the ambient temperature and power dissipation using the formula $T_J = T_A + P_D \times \theta_{JA}$.

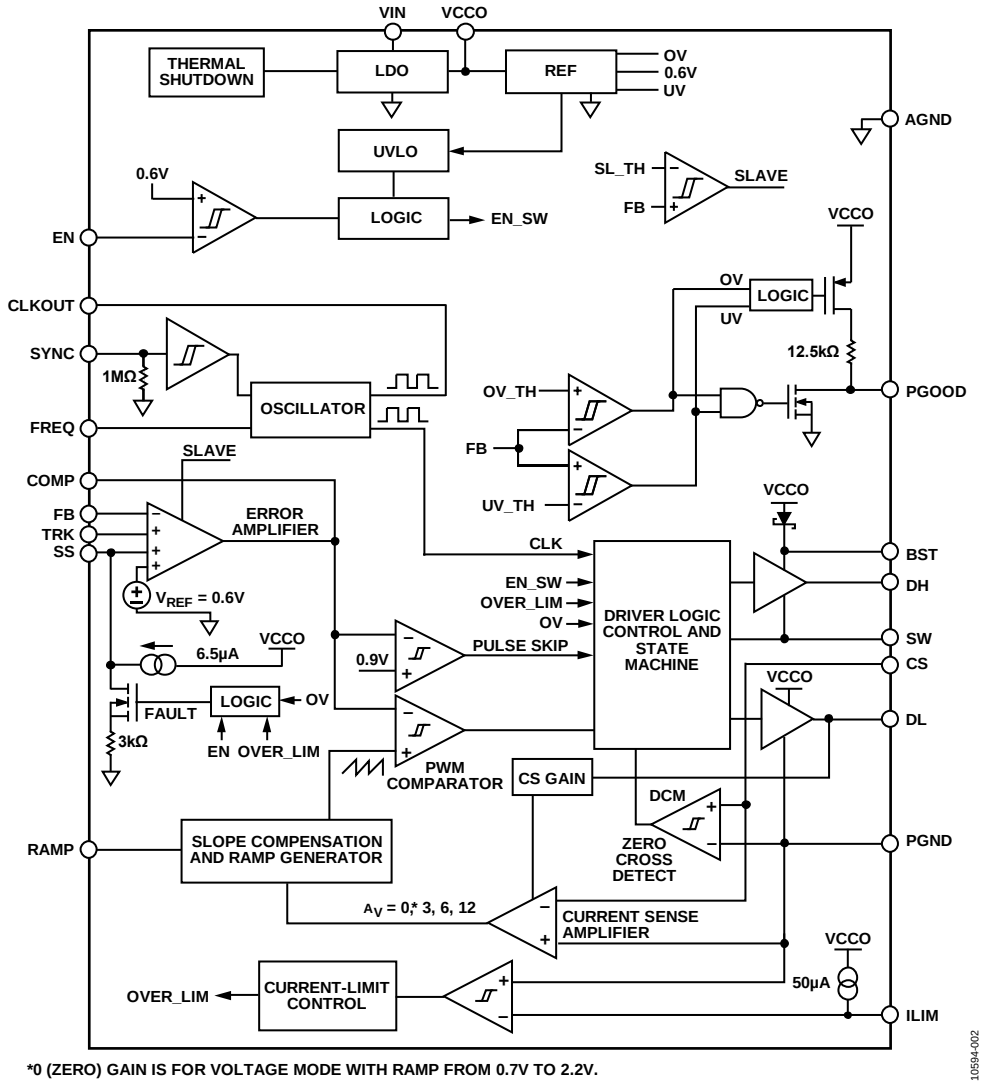
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings apply individually only, not in combination. Unless otherwise specified, all other voltages are referenced to GND.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

SIMPLIFIED BLOCK DIAGRAM



*0 (ZERO) GAIN IS FOR VOLTAGE MODE WITH RAMP FROM 0.7V TO 2.2V.

Figure 2.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

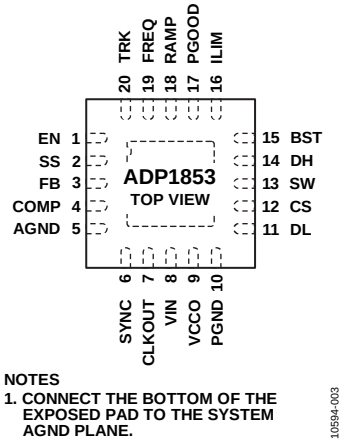


Figure 3. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	EN	Enable Input. Drive EN high to turn on the controller, and drive EN low to turn the controller off. Tie EN to V_{IN} for automatic startup. For a precision UVLO, put an appropriately sized resistor divider from V_{IN} to AGND, and tie the midpoint to this pin.
2	SS	Soft Start Input. Connect a capacitor from SS to AGND to set the soft start period. This node is internally pulled up to VCCO through a 6.5 µA current source.
3	FB	Output Voltage Feedback. Connect this pin to an output via a resistor divider. Tie FB to VCCO for slave mode operation in interleaved dual-phase configuration.
4	COMP	Compensation Node. Output of the error amplifier. Connect a resistor-capacitor network from COMP to FB to compensate the regulation control loop. In interleaved dual-phase configuration, tie this pin to the COMP pin of the second channel.
5	AGND	Analog Ground. Connect to the system AGND plane.
6	SYNC	Frequency Synchronization Input. This pin accepts an external clock signal with a frequency close to 1× the internal oscillator frequency, f_{OSC}, set by the FREQ pin. The controller operates in forced PWM when a periodic clock signal is detected at SYNC or when SYNC is high. The resulting switching frequency is 1× the SYNC frequency. When SYNC is low or left floating, the controller operates in pulse skip mode.
7	CLKOUT	Internal Clock Output. The CLKOUT is 1× the internal oscillator or input SYNC signal frequency, 180° phase-shifted. This pin can be used to synchronize another ADP1853 or other controllers.
8	VIN	Connect to Main Power Supply. Bypass with a 1 µF or larger ceramic capacitor connected as close to this pin as possible and AGND.
9	VCCO	Output of the Internal Low Dropout Regulator (LDO). The internal circuitry and gate drivers are powered from VCCO. Bypass VCCO to AGND with a 1 µF or larger ceramic capacitor. The VCCO output remains active even when EN is low. For operations at V_{IN} below 5 V, V_{IN} may be jumped to VCCO. Do not use the LDO to power other auxiliary system loads.
10	PGND	Power Ground. Ground for internal driver. Differential current.
11	DL	Low-Side Synchronous Rectifier Gate Driver Output. To program the gain of the current sense amplifier in a current mode or to set voltage mode control, connect a resistor between DL and PGND. This pin is capable of driving MOSFETs with a total input capacitance up to 20 nF.
12	CS	Current Sense Amplifier Input. Differential current is sensed between CS and PGND. Connect this pin to the current sense resistor or to the SW pin to sense the current. Tie this pin to PGND for voltage mode operation.
13	SW	Power Switch Node. Connect this pin to the source of the high-side N-channel MOSFET and the drain of the low-side N-channel MOSFET.
14	DH	High-Side Switch Gate Driver Output. This pin is capable of driving MOSFETs with a total input capacitance up to 20 nF.
15	BST	Boot Strapped Upper Rail of High-Side Internal Driver. Connect a 0.1 µF to a 0.22 µF multilayer ceramic capacitor (MLCC) between BST and SW. There is an internal boost diode rectifier connected between VCCO and BST.
16	ILIM	Current-Limit Sense Comparator Inverting Input. Connect a resistor between ILIM and SW to set the current-limit offset. For accurate current-limit sensing, connect ILIM to a current sense resistor at the source of the low-side MOSFET.

Pin No.	Mnemonic	Description
17	PGOOD	Power Good. The open-drain power good indicator logic output with an internal 12.5 kΩ resistor is connected between PGOOD and VCCO. PGOOD is pulled to ground when the output is outside the regulation window. An external pull-up resistor is not required. If the controller is configured as a slave in the interleaved dual-phase application by tying the FB pin high to VCCO, the pulse skip mode is enabled by driving the PGOOD pin low externally in cases when the master is in pulse skip mode at light loads. Otherwise, if the master is configured to forced PWM operation, PGOOD of the slave controller must be connected to the PGOOD of the master.
18	RAMP	Programmable Current Setting for Slope Compensation. Connect a resistor from RAMP to V_{IN}. The voltage at RAMP is 0.2 V during operation. This pin is high impedance when the channel is disabled.
19	FREQ	Internal Oscillator Frequency, f_{OSC}. Sets the desired operating frequency between 200 kHz and 1.5 MHz with one resistor between FREQ and AGND. Connect FREQ to AGND for a preprogrammed 300 kHz or tie FREQ to VCCO for 600 kHz operating frequency.
20	TRK	Tracking Input. Connect TRK to VCCO if tracking is not used.
	EPAD	Exposed Pad. Connect the bottom of the exposed pad to the system AGND plane.

TYPICAL PERFORMANCE CHARACTERISTICS

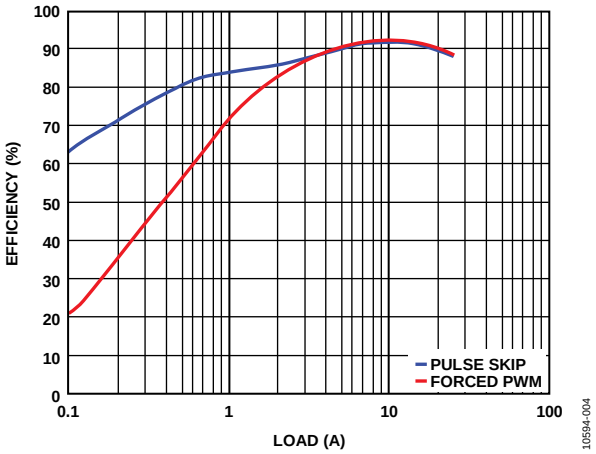


Figure 4. Efficiency Plot
12 V_{IN} to 3.3 V_{OUT}, 300 kHz, see Figure 36 for Circuit

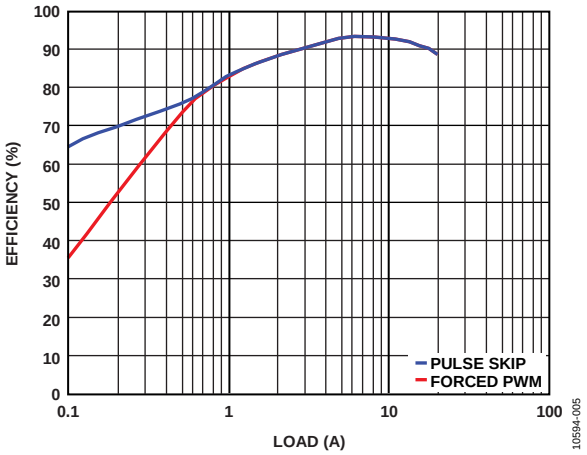


Figure 7. Efficiency Plot
15 V_{IN} to 5 V_{OUT}, 600 kHz, see Figure 35 for Circuit

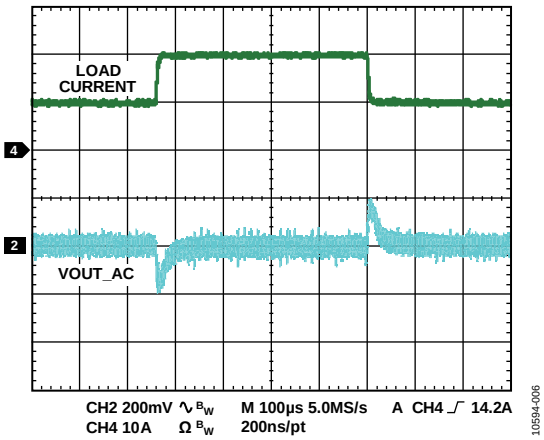


Figure 5. 10 A to 20 A Load Step,
12 V_{IN} to 3.3 V_{OUT}, 300 kHz, Current Mode

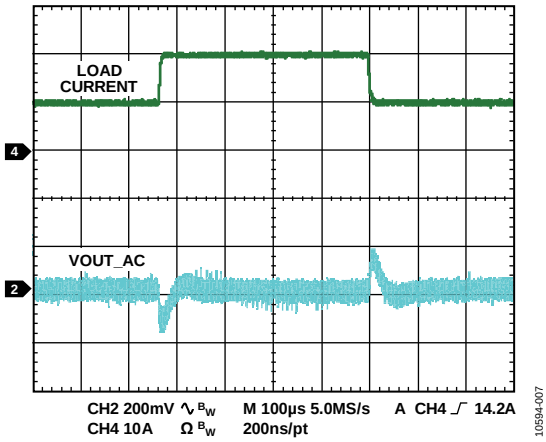


Figure 8. 10 A to 20 A Load Step,
12 V_{IN} to 3.3 V_{OUT}, 300 kHz, Voltage Mode

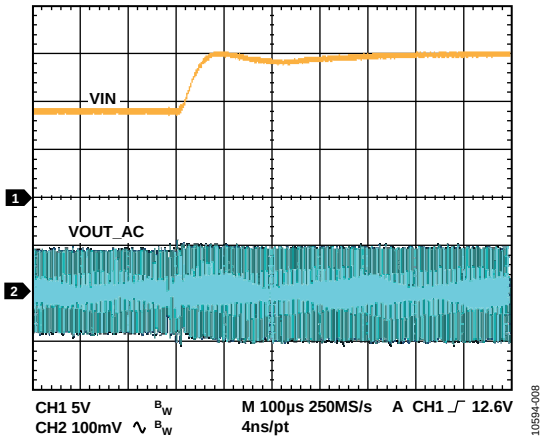


Figure 6. 9 V to 15 V Line Step,
3.3 V_{OUT}, 15 A Load, Current Mode

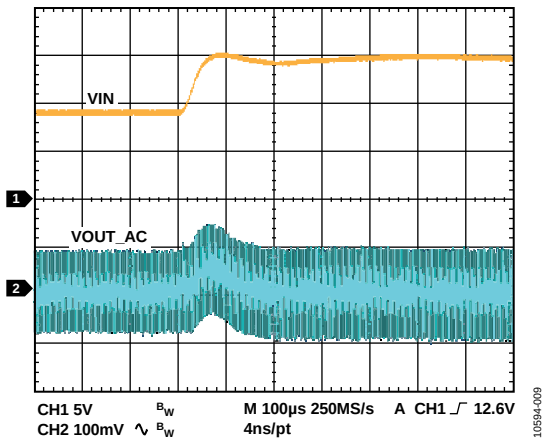


Figure 9. 9 V to 15 V Line Step,
3.3 V_{OUT}, 15 A Load, Voltage Mode

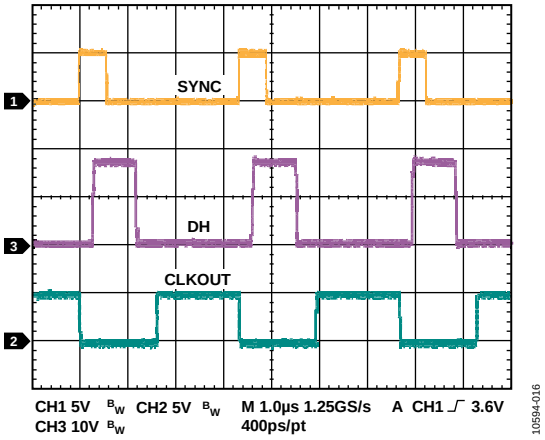


Figure 10. Synchronization and CLKOUT, f_{SYNC} = 300 kHz

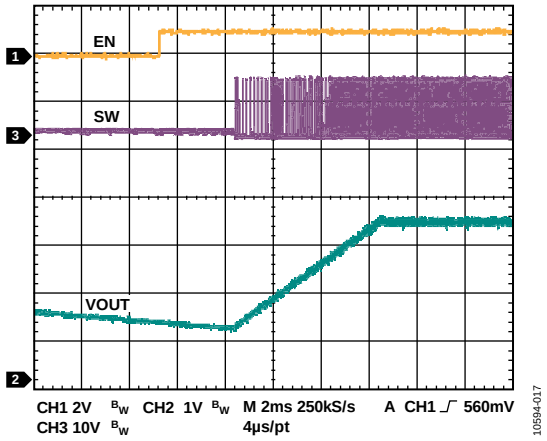


Figure 13. Soft Start with Precharged Output, 3.3 V_{OUT} Forced PWM

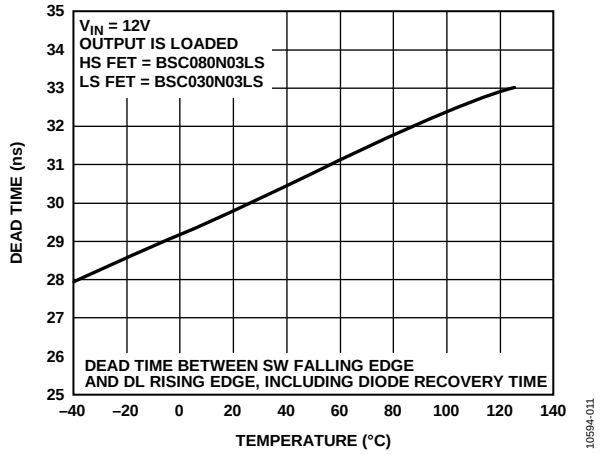


Figure 11. Dead Time vs. Temperature

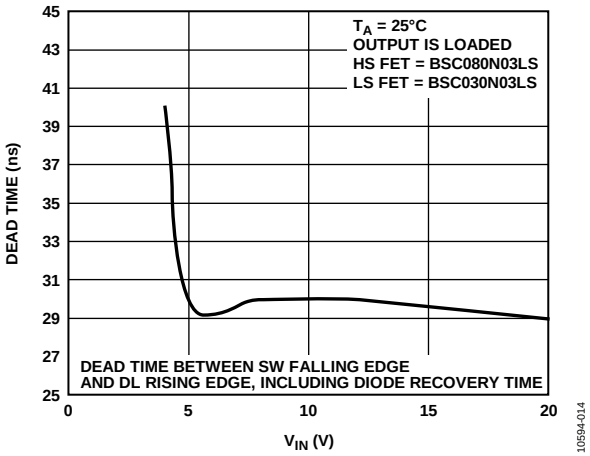


Figure 14. Dead Time vs. V_{IN}

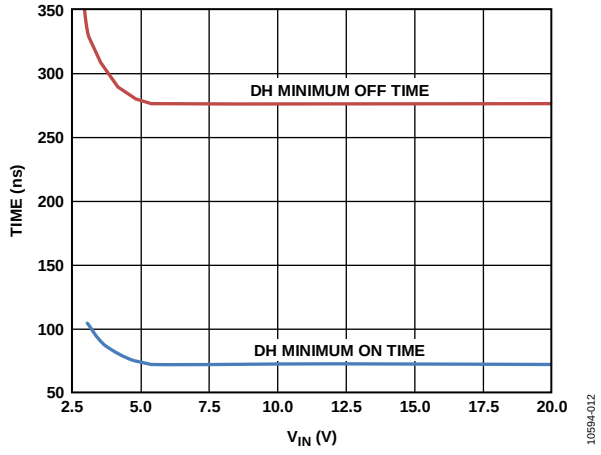


Figure 12. Typical DH Minimum On Time and Off Time

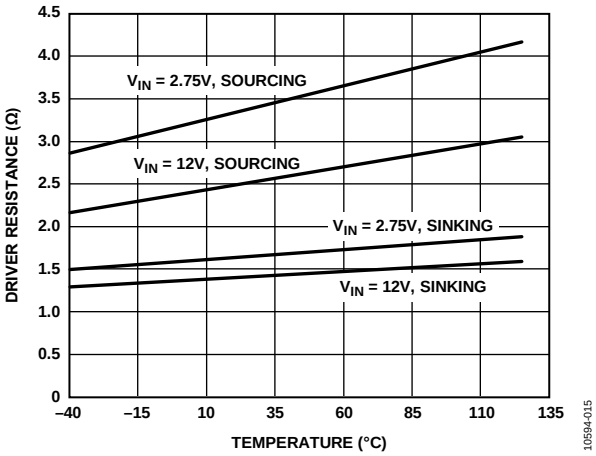


Figure 15. Driver Resistance vs. Temperature

THEORY OF OPERATION

The ADP1853 is a fixed frequency, step-down, synchronous switching controller with integrated drivers and bootstrapping for external N-channel power MOSFETs. The current mode control loop can also be configured into the voltage mode. The controller can be set to operate in pulse skip mode for power saving at a light load or in forced PWM. The ADP1853 includes programmable soft start, output overvoltage protection, programmable current limit, power good, and tracking functions. The controller can operate at a switching frequency between 200 kHz and 1.5 MHz that is programmed with a resistor or synchronized to an external clock. It also has the internal clock out signal that can be used to synchronize other devices.

CONTROL ARCHITECTURE

The ADP1853 is based on a fixed frequency, emulated peak current mode, PWM control architecture. The inductor current is sensed by the voltage drop measured across the external low-side MOSFET, R_{DSON}, or across the sense resistor placed in series between the low-side MOSFET source and the power ground. The current is sensed during the off period of the switching cycle and is conditioned with the internal current sense amplifier. The gain of the current sense amplifier is programmable to 3 V/V, 6 V/V, or 12 V/V during the controller power-up initialization before the device starts switching. A 47 kΩ resistor between DL and PGND programs the gain of 3 V/V; a 22 kΩ resistor sets a gain of 6 V/V. Without a resistor, the gain is programmed to 12 V/V. The output signal of the current sense amplifier is held, added to the emulated current ramp in the next switching cycle during the DH on time, and fed into the PWM comparator, as shown in Figure 16. This signal is compared with the COMP signal from the error amplifier and resets the flip-flop, which generates the PWM pulse. If voltage mode control is selected by placing a 100 kΩ resistor between DL and PGND, the emulated ramp is fed to the PWM comparator without adding the current sense signal.

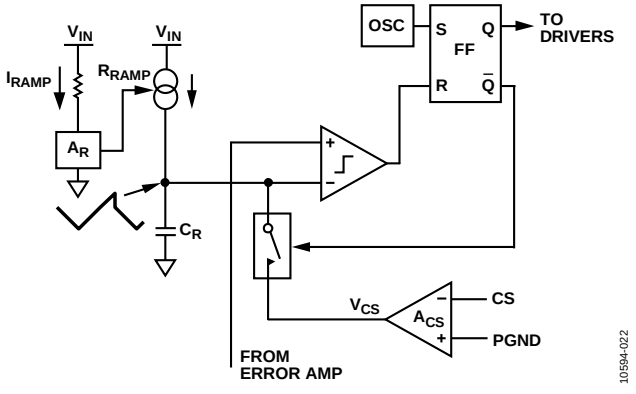


Figure 16. Simplified Control Architecture

As shown in Figure 16, the emulated current ramp is generated inside the IC, but offers programmability through the RAMP pin. Selecting an appropriate value resistor between V_{IN} to the RAMP pin programs a desired slope compensation value, and at the same time, provides a V_{IN} feed forward feature. Control logic enforces antishoot-through operation to limit cross conduction of the internal drivers and external MOSFETs.

OSCILLATOR FREQUENCY

The internal oscillator frequency, which ranges from 200 kHz to 1.5 MHz, is set by an external resistor, R_{FREQ}, at the FREQ pin. Some popular f_{OSC} values are shown in Table 4, and a graphical relationship is shown in Figure 17. For instance, a 78.7 kΩ resistor sets the oscillator frequency to 800 kHz. Furthermore, connecting FREQ to AGND or FREQ to VCCO sets the oscillator frequency to 300 kHz or 600 kHz, respectively. For other frequencies that are not listed in Table 4, the values of R_{FREQ} and f_{OSC} can be obtained from Figure 17, or use the following empirical formula to calculate these values:

$$R_{FREQ}(\text{k}\Omega) = 96{,}568 \times f_{OSC}(\text{kHz})^{-1.065}$$

Table 4. Setting the Oscillator Frequency

R_{FREQ}	f_{OSC} (Typical)
332 kΩ	200 kHz
78.7 kΩ	800 kHz
60.4 kΩ	1000 kHz
51 kΩ	1200 kHz
40.2 kΩ	1500 kHz
FREQ to AGND	300 kHz
FREQ to VCCO	600 kHz

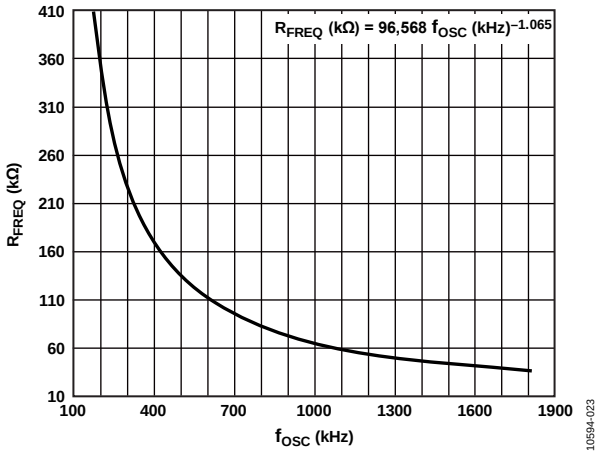


Figure 17. R_{FREQ} vs. f_{OSC}

SYNCHRONIZATION

The switching frequency of the ADP1853 can be synchronized to an external clock signal by connecting it to the SYNC pin. The internal oscillator frequency, programmed by the resistor at the FREQ pin must be set close to the external clock frequency; therefore, the external clock frequency may vary between 0.85× and 1.3× of the internal clock set. The resulting switching frequency is 1× of the external SYNC frequency. When synchronized, the ADP1853 operates in PWM.

When an external clock is detected at the first SYNC edge, the internal oscillator is reset, and the clock control shifts to SYNC. The SYNC edges then trigger subsequent clocking of the PWM outputs. The DH rising edge appears approximately 100 ns after the corresponding SYNC edge, and the frequency is locked to the external signal. If the external SYNC signal disappears during operation, the ADP1853 reverts to its internal oscillator. When the SYNC function is used, it is recommended to connect a pull-up resistor from SYNC to VCCO so that when the SYNC signal is lost, the ADP1853 continues to operate in PWM.

PWM OR PULSE SKIP MODE OF OPERATION

The SYNC pin is a multifunctional pin. PWM mode is enabled when SYNC is connected to VCCO or a high logic. With SYNC connected to ground or left floating, pulse skip mode is enabled. Switching SYNC from low to high or high to low on the fly causes the controller to transition from forced PWM to pulse skip mode or from pulse skip mode to forced PWM, respectively, in two clock cycles.

Table 5. Mode of Operation

SYNC Pin	Mode of Operation
Low	Pulse skip mode
High	Forced PWM
No Connect	Pulse skip mode
Clock Signal	Forced PWM

The ADP1853 has pulse skip sensing circuitry that allows the controller to skip PWM pulses, reducing the switching frequency at light loads and, therefore, maintaining better efficiency during a light load operation. The resulting output ripple is larger than that of the fixed frequency forced PWM. Figure 18 shows the ADP1853 operating in PSM under a light load. Pulse skip frequency under a light load is dependent on the inductor, output capacitance, output load, and input and output voltages.

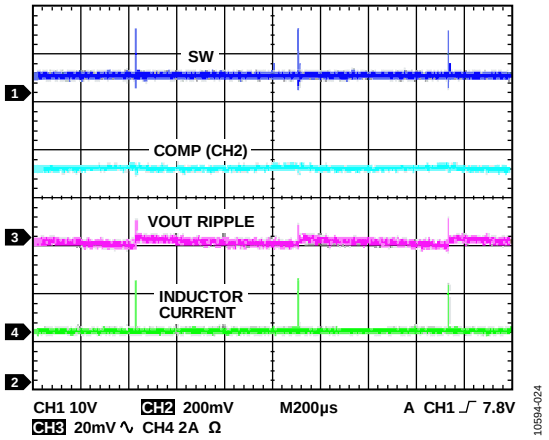


Figure 18. Example of Pulse Skip Mode Under a Light Load

When the output load is greater than the pulse skip threshold current, that is, when V_{COMP} reaches the threshold of 0.9 V, the ADP1853 exits the pulse skip mode of operation and enters the fixed frequency discontinuous conduction mode (DCM), as shown in Figure 19. When the load increases further, the ADP1853 enters continuous conduction mode (CCM).

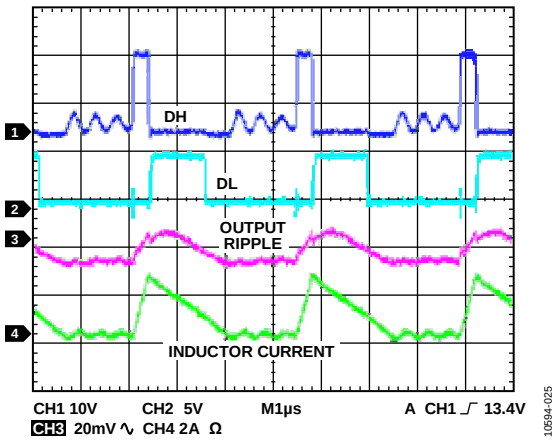


Figure 19. Example of Discontinuous Conduction Mode (DCM) Waveform

In forced PWM, the ADP1853 always operates in CCM at any load; therefore, the inductor current is always continuous.

CLKOUT SIGNAL

The ADP1853 has a clock output, CLKOUT, which can be used for synchronizing other ADP1853 controllers, thus eliminating the need for an external clock source. The CLKOUT frequency is 1× the internal oscillator frequency, f_{OSC}, and is 180° out of phase.

SYNCHRONOUS RECTIFIER AND DEAD TIME

In the ADP1853, the antishoot-through circuit monitors the DH to SW and DL to PGND voltages and adjusts the low-side and high-side drivers to ensure break-before-make switching that prevents cross-conduction or shoot-through between the high-side and low-side MOSFETs. This break-before-make switching is known as dead time, which is not fixed and depends on how fast the MOSFETs are turned on and off. In a typical application circuit that uses medium sized MOSFETs with an input capacitance of approximately 3 nF, the typical dead time is approximately 25 ns. When small and fast MOSFETs with fast diode recovery times are used, the dead time can be as low as 13 ns.

INPUT UNDERVOLTAGE LOCKOUT

When the bias input voltage at the VIN pin is less than the undervoltage lockout (UVLO) threshold of 2.6 V typical, the switch drivers stay inactive. If EN is high, the controller starts switching and the VIN pin voltage exceeds the UVLO threshold.

INTERNAL LINEAR REGULATOR

The internal linear regulator is a low dropout (LDO) VCCO. VCCO powers up the internal control circuitry and provides power for the gate drivers. It is guaranteed to have more than 200 mA of output current capability, which is sufficient to handle the gate driver requirements of typical logic threshold MOSFETs driven at up to 1.5 MHz. VCCO is always active and cannot be shut down by the EN signal; however, the over-temperature protection event disables the LDO together with the controller. Bypass VCCO to AGND with a 1 µF or greater capacitor.

Because the LDO supplies the gate driver current, the output of VCCO is subject to sharp transient currents as the drivers switch and the boost capacitors recharge during each switching cycle. The LDO has been optimized to handle these transients without overload faults. Due to the gate drive loading, using the VCCO output for other external auxiliary system loads is not recommended.

The LDO includes a current limit that is well above the expected maximum gate driver load. This current limit also includes a short-circuit foldback to further limit the VCCO current in the event of a short-circuit fault.

For an input voltage of less than 5.5 V, it is recommended to bypass the LDO by connecting VIN to VCCO, as shown in Figure 20, thus eliminating the dropout voltage. However, if the input range is 4 V to 7 V, the LDO cannot be bypassed by shorting VIN to VCCO because the 7 V input has exceeded the maximum voltage rating of the VCCO pin. In this case, use the LDO to drive the internal drivers, but keep in mind that there is a dropout when V_{IN} is less than 5 V.

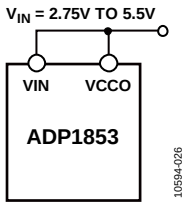


Figure 20. Configuration for V_{IN} < 5.5 V

OVERVOLAGE PROTECTION

The ADP1853 has a built-in circuit for detecting output over-voltage at the FB node. When the FB voltage, V_{FB}, rises above the overvoltage threshold, the high-side N-channel MOSFET (NMOSFET) is turned off, and the low-side NMOSFET is turned on until the V_{FB} drops below the undervoltage threshold. This action is known as the crowbar overvoltage protection. If the overvoltage condition is not removed, the controller maintains the feedback voltage between the overvoltage and undervoltage thresholds, and the output is regulated to within typically +8% and −8% of the regulation voltage. During an overvoltage event, the SS node discharges toward zero through an internal 3 kΩ pull-down resistor. When the voltage at FB drops below the undervoltage threshold, the soft start sequence restarts. Figure 21 shows the overvoltage protection scheme in action in PSM.

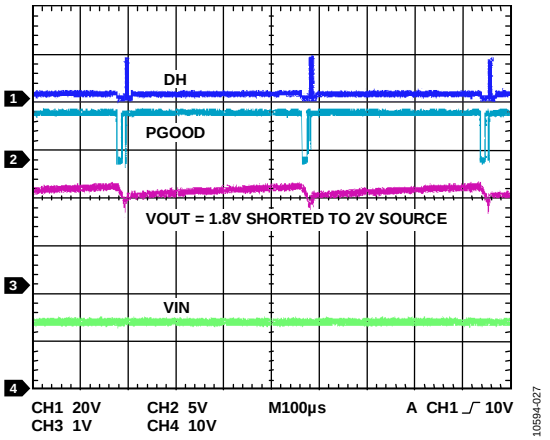


Figure 21. Overvoltage Protection in PSM

POWER GOOD

The PGOOD pin is an open-drain NMOSFET with an internal 12.5 kΩ pull-up resistor connected between PGOOD and VCCO. PGOOD is internally pulled up to VCCO during normal operation and is active low when tripped. When the feedback voltage, V_{FB}, rises above the overvoltage threshold or drops below the undervoltage threshold, the PGOOD output is pulled to ground after a delay of 12 µs. The overvoltage or undervoltage condition must exist for more than 10 µs for PGOOD to become active. The PGOOD output also becomes active if a thermal overload condition is detected.

SHORT-CIRCUIT AND CURRENT-LIMIT PROTECTION

When the output is shorted or the output current exceeds the current limit set by the current-limit setting resistor (between ILIM and CS) for eight consecutive cycles, the ADP1853 shuts off both the high-side and low-side drivers and restarts the soft start sequence every 10 ms, which is known as hiccup mode. The SS node discharges to zero through an internal 3 kΩ resistor during an overcurrent or short-circuit event. Figure 22 shows that the ADP1853 on a high current application circuit maintains current-limit hiccup mode when the output is shorted.

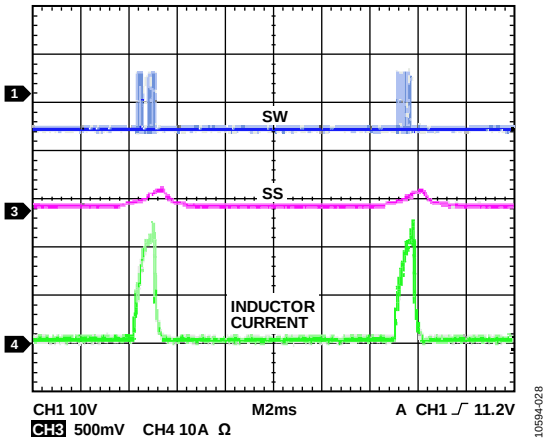


Figure 22. Current-Limit Hiccup Mode, 20 A Current Limit

ENABLE/DISABLE CONTROL

The EN pin is used to enable or disable the controller ADP1853; the precision enable typical threshold is 0.63 V. When the voltage at EN rises above the threshold voltage, the controller is enabled and starts normal operation after initialization of the internal oscillator, references, settings, and the soft start period. When the voltage at EN drops to typically 30 mV (hysteresis) below the threshold voltage, the driver and the internal controller circuits in the ADP1853 are turned off. The initial settings are still valid; therefore re-enabling the controller does not change the settings until the power at the VIN pin is cycled. In addition, the EN signal does not shut down the LDO at VCCO, which is always active when V_{IN} is above the UVLO threshold.

For the purpose of start-up power sequencing, the startup of the ADP1853 can be programmed by connecting an appropriate resistor divider from the master power supply to the EN pin, as shown in Figure 23. For instance, if the desired start-up voltage from the master power supply is 10 V, R1 and R2 can be set to 156 kΩ and 10 kΩ, respectively.

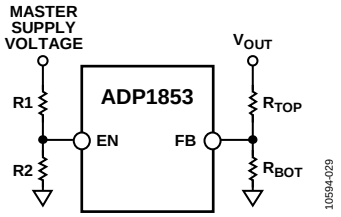


Figure 23. Optional Power-Up Sequencing Circuit

THERMAL OVERLOAD PROTECTION

The ADP1853 has an internal temperature sensor that senses the junction temperature of the chip. When the junction temperature of the ADP1853 reaches approximately 155°C, the ADP1853 goes into thermal shutdown, the converter is turned off, and SS discharges toward zero through an internal 3 kΩ resistor. At the same time, VCCO discharges to zero. When the junction temperature drops below 135°C, the ADP1853 resumes normal operation after the soft start sequence.

INTERLEAVED DUAL-PHASE OPERATION

Two ADP1853 controllers can be configured to design a dual-phase, interleaved, step-down, switching dc-to-dc regulators. In dual-phase operation, the two outputs of the switching regulators are tied together and can source more than 50 A of output current depending on the selection of the power components. See Figure 24 for a configuration of a typical dual-phase application circuit. Note that only one error amplifier, in the master ADP1853, works; the error amplifier in the slave ADP1853 output is turned to tristate by tying FB to VCCO. The CLKOUT signal from the master is connected to the SYNC input of the slave controller; the SS signals of the master and slave are tied together; COMP of the slave must be tied to COMP of the master; and PGOOD of the slave must be tied to PGOOD of the master.

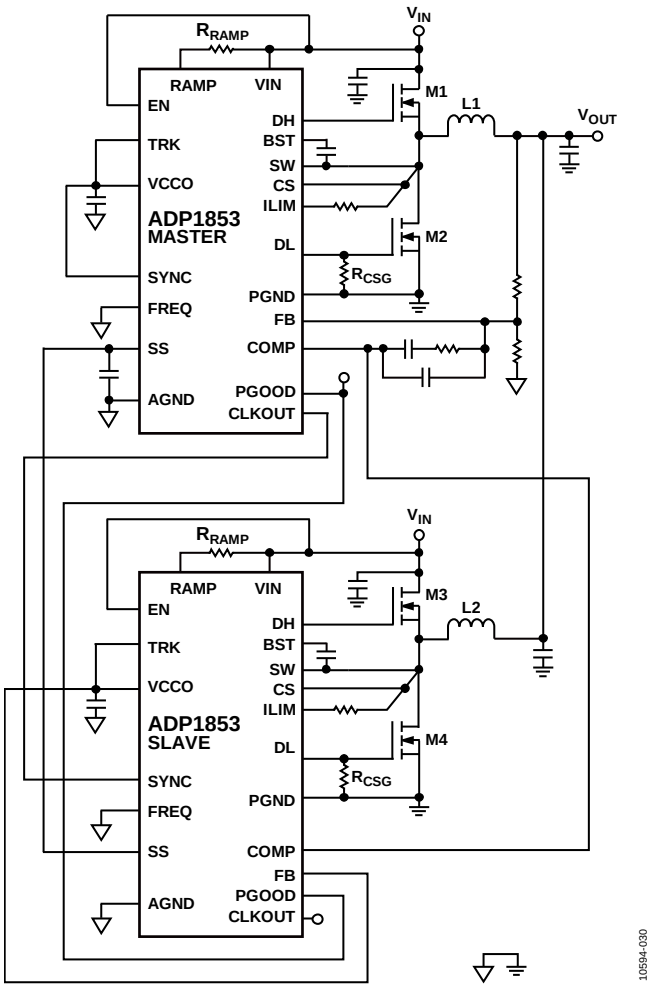


Figure 24. Dual-Phase Application

APPLICATIONS INFORMATION

ADIsimPower DESIGN TOOL

The ADP1853 is supported by the ADIsimPower design tool set. ADIsimPower is a collection of tools that produce complete power designs optimized to a specific design goal. The tools allow the user to generate a full schematic, bill of materials, and calculate performance in minutes. ADIsimPower can optimize designs for cost, area, efficiency, and parts count while taking into consideration the operating conditions and limitations of the IC and all real external components. The ADIsimPower tool can be found at www.analog.com/ADIsimPower and the user can request an unpopulated board through the tool.

SETTING THE OUTPUT VOLTAGE

The output voltage is set using a resistive voltage divider from the output to FB. For R_{BOT}, use a 1 kΩ to 20 kΩ resistor. Choose R_{TOP} to set the output voltage by using the following equation:

$$R_{TOP} = R_{BOT}\left(\frac{V_{OUT} - V_{FB}}{V_{FB}}\right)$$

where:
R_{TOP} is the high-side voltage divider resistance.
R_{BOT} is the low-side voltage divider resistance.
V_{OUT} is the regulated output voltage.
V_{FB} is the feedback regulation threshold, 0.6 V.

SOFT START

The soft start period is set by an external capacitor between SS and AGND. The soft start function limits the input inrush current and prevents output overshoot. When EN is enabled, a current source of 6.5 µA starts charging the capacitor, and the regulation voltage is reached when the voltage at SS reaches 0.6 V. The soft start time is approximated by

$$t_{SS} = \frac{0.6\ \text{V}}{6.5\ \mu\text{A}} C_{SS}$$

The SS pin reaches a final voltage equal to VCCO.

When a controller is disabled, for instance, if EN is pulled low or experiences an overcurrent limit condition, the soft start capacitor is discharged through an internal 3 kΩ pull-down resistor.

SETTING THE CURRENT LIMIT

The current-limit comparator measures the voltage across the low-side MOSFET to determine the load current.

The current limit is set by an external current-limit resistor, R_{ILIM}, between ILIM and CS. The current sense pin, ILIM, sources nominally 50 µA to this external resistor. This creates an offset voltage of R_{ILIM} multiplied by 50 µA. When the drop across the current sense element R_{CS} (a sense resistor or low-side MOSFET, R_{DSON}) is equal to or greater than this offset voltage, the ADP1853 flags a current-limit event.

$$R_{ILIM} = \frac{1.06 \times I_{LPK} \times R_{CS}}{50\ \mu\text{A}}$$

where:
I_{LPK} is the peak inductor current.

ACCURATE CURRENT-LIMIT SENSING

R_{DSON} of the MOSFET can vary by more than 50% over the temperature range. Accurate current-limit sensing is achieved by adding a current sense resistor from the source of the low-side MOSFET to PGND. Make sure that the power rating of the current sense resistor is adequate for the application. Figure 25 illustrates the implementation of accurate current-limit sensing.

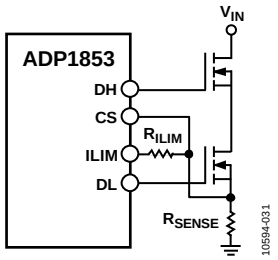


Figure 25. Accurate Current-Limit Sensing

INPUT CAPACITOR SELECTION

Use two parallel capacitors placed close to the drain of the high-side switch MOSFET (one bulk capacitor of sufficiently high current rating and a 10 µF ceramic decoupling capacitor).

Select an input bulk capacitor based on its ripple current rating. The minimum input capacitance required for a particular load is

$$C_{IN,MIN} = \frac{I_O \times D(1-D)}{(V_{PP} - I_O \times DR_{ESR}) f_{SW}}$$

where:
I_O is the output current.
D is the duty cycle.
V_{PP} is the desired input ripple voltage.
R_{ESR} is the equivalent series resistance of the capacitors.

VIN PIN FILTER

It is recommended to have a low-pass filter at the VIN pin. Connecting a resistor, between 2 Ω and 10 Ω, in series with VIN and a 1 µF ceramic capacitor between VIN and AGND creates a low-pass filter that effectively filters out any unwanted glitches caused by the switching regulator. Keep in mind that the input current could be larger than 100 mA when driving large MOSFETs. A 100 mA across a 10 Ω resistor creates a 1 V drop, which is the same voltage drop in VCCO. In this case, a lower resistor value is desirable.

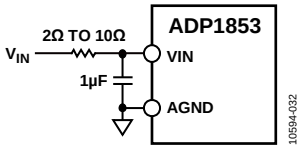


Figure 26. Input Filter Configuration

BOOST CAPACITOR SELECTION

Connect a boost capacitor between the SW and BST pins to provide the current for the high-side driver during switching. Choose a ceramic capacitor with a value between 0.1 µF and 0.22 µF.

INDUCTOR SELECTION

For most applications, choose an inductor value such that the inductor ripple current is between 20% and 40% of the maximum dc output load current.

Choose the inductor value by the following equation:

$$L = \frac{V_{IN} - V_{OUT}}{f_{SW} \times \Delta I_L} \times \frac{V_{OUT}}{V_{IN}}$$

where:
L is the inductor value.
f_{SW} is the switching frequency.
V_{OUT} is the output voltage.
V_{IN} is the input voltage.
ΔI_L is the peak-to-peak inductor ripple current.

Check the inductor data sheet to make sure that the saturation current of the inductor is well above the peak inductor current of a particular design.

OUTPUT CAPACITOR SELECTION

For maximum allowed switching ripple at the output, choose an output capacitor that is larger than

$$C_{OUT} \cong \frac{\Delta I_L}{8 f_{SW}} \times \frac{1}{\sqrt{\Delta V_{OUT}{}^2 - \Delta I_L{}^2 \times (R_{ESR}{}^2 - (4 f_{SW} \times L_{ESL})^2)}}$$

where:
ΔV_{OUT} is the target maximum output ripple voltage.
ΔI_L is the inductor ripple current.
R_{ESR} is the equivalent series resistance of the output capacitor (or the parallel combination of ESR of all output capacitors).
L_{ESL} is the equivalent series inductance of the output capacitor (or the parallel combination of ESL of all capacitors).

The impedance of the output capacitor at the switching frequency multiplied by the ripple current gives the output voltage ripple. The impedance is made up of the capacitive impedance plus the nonideal parasitic characteristics, the equivalent series resistance (ESR), and the equivalent series inductance (ESL).

Usually the capacitor impedance is dominated by ESR. The maximum ESR rating of the capacitor, such as in electrolytic or polymer capacitors, is provided in the manufacturer's data sheet; therefore, the output ripple reduces to

$$\Delta V_{OUT} \cong \Delta I_L \times R_{ESR}$$

Electrolytic capacitors also have significant ESL, on the order of 5 nH to 20 nH, depending on type, size, and geometry. PCB traces contribute some ESR and ESL, as well. However, using the maximum ESR rating from the capacitor data sheet usually provides some margin such that measuring the ESL may not be required.

In the case of output capacitors where the impedance of the ESR and ESL are small at the switching frequency, for instance, where the output capacitor is a bank of parallel MLCC capacitors, the capacitive impedance dominates, so the output capacitance must be larger than

$$C_{OUT} \cong \frac{\Delta I_L}{8 \, \Delta V_{OUT} \times f_{SW}}$$

Make sure that the ripple current rating of the output capacitors is greater than the maximum inductor ripple current.

To meet the requirement of the output voltage overshoot during load release, the output capacitance should be larger than

$$C_{OUT} \cong \frac{\Delta I_{STEP}{}^2 L}{(V_{OUT} + \Delta V_{OVERSHOOT})^2 - V_{OUT}{}^2}$$

where:
$\Delta V_{OVERSHOOT}$ is the maximum allowed overshoot.

Select the largest output capacitance given by either of the previous two equations.

MOSFET SELECTION

The choice of MOSFET directly affects the dc-to-dc converter performance. A MOSFET with low on resistance reduces I^2R losses, and low gate charge reduces transition losses. The MOSFET should have low thermal resistance to ensure that the power dissipated in the MOSFET does not result in excessive MOSFET die temperature.

The high-side MOSFET carries the load current during on time and usually carries most of the transition losses of the converter. Typically, the lower the on resistance of the MOSFET, the higher the gate charge and vice versa. Therefore, it is important to choose a high-side MOSFET that balances the two losses. The conduction loss of the high-side MOSFET is determined by the equation

$$P_C = (I_{LOAD(RMS)})^2 \times R_{DSON}$$

where:
R_{DSON} is the MOSFET on resistance.

The gate charging loss is approximated by the equation

$$P_G \cong V_{PV} \times Q_G \times f_{SW}$$

where:
V_{PV} is the gate driver supply voltage.
Q_G is the MOSFET total gate charge.

Note that the gate charging power loss is not dissipated in the MOSFET but rather in the ADP1853 internal drivers. This power loss should be taken into consideration when calculating the overall power efficiency.

The high-side MOSFET transition loss is approximated by the equation

$$P_T \cong \frac{V_{IN} \times I_{LOAD} \times (t_R + t_F) \times f_{SW}}{2}$$

where:
P_T is the high-side MOSFET switching loss power.
t_R is the rise time in charging the high-side MOSFET.
t_F is the fall time in discharging the high-side MOSFET.

t_R and t_F can be estimated by

$$t_R \cong \frac{Q_{GSW}}{I_{DRIVER\_RISE}}$$

$$t_F \cong \frac{Q_{GSW}}{I_{DRIVER\_FALL}}$$

where:
Q_{GSW} is the gate charge of the MOSFET during switching and is given in the MOSFET data sheet.
I_{DRIVER_RISE} and I_{DRIVER_FALL} are the driver current output from the ADP1853 internal gate drivers.

If Q_{GSW} is not given in the data sheet, it can be approximated by

$$Q_{GSW} \cong Q_{GD} + \frac{Q_{GS}}{2}$$

where:
Q_{GD} and Q_{GS} are the gate-to-drain and gate-to-source charges given in the MOSFET data sheet.

I_{DRIVER_RISE} and I_{DRIVER_FALL} can be estimated by

$$I_{DRIVER\_RISE} \cong \frac{V_{DD} - V_{SP}}{R_{ON\_SOURCE} + R_{GATE}}$$

$$I_{DRIVER\_FALL} \cong \frac{V_{SP}}{R_{ON\_SINK} + R_{GATE}}$$

where:
V_{DD} is the input supply voltage to the driver and is between 2.75 V and 5 V, depending on the input voltage.
V_{SP} is the switching point where the MOSFET fully conducts; this voltage can be estimated by inspecting the gate charge graph given in the MOSFET data sheet.
R_{ON_SOURCE} is the on resistance of the ADP1853 internal driver, given in Table 1, when charging the MOSFET.
R_{ON_SINK} is the on resistance of the ADP1853 internal driver, given in Table 1, when discharging the MOSFET.
R_{GATE} is the on gate resistance of MOSFET given in the MOSFET data sheet. If an external gate resistor is added, add this external resistance to R_{GATE}.

The total power dissipation of the high-side MOSFET is the sum of conduction and transition losses:

$$P_{HS} \cong P_C + P_T$$

The synchronous rectifier, or low-side MOSFET, carries the inductor current when the high-side MOSFET is off. The low-side MOSFET transition loss is small and can be neglected in the calculation. For high input voltage and low output voltage, the low-side MOSFET carries the current most of the time. Therefore, to achieve high efficiency, it is critical to optimize the low-side MOSFET for low on resistance. In cases where the power loss exceeds the MOSFET rating or lower resistance is required than is available in a single MOSFET, connect multiple low-side MOSFETs in parallel. The equation for low-side MOSFET conduction power loss is

$$P_{CLS} = (I_{LOAD(RMS)})^2 \times R_{DSON}$$

There is also additional power loss during the time, known as dead time, between the turn-off of the high-side switch and the turn-on of the low-side switch, when the body diode of the low-side MOSFET conducts the output current. The power loss in the body diode is given by

$$P_{BODYDIODE} = V_F \times t_D \times f_{SW} \times I_O$$

where:
V_F is the forward voltage drop of the body diode, typically 0.7 V.
t_D is the dead time in the ADP1853, typically 30 ns when driving a medium size MOSFETs with input capacitance, C_{iss}, of approximately 3 nF. The dead time is not fixed. Its effective value varies with gate drive resistance and C_{iss}; therefore, $P_{BODYDIODE}$ increases in high load current designs and low voltage designs.

Then the power loss in the low-side MOSFET is

$$P_{LS} = P_{CLS} + P_{BODYDIODE}$$

Note that MOSFET on resistance, R_{DSON}, increases with increasing temperature with a typical temperature coefficient of 0.4%/°C. The MOSFET junction temperature (T_J) rise over the ambient temperature is

$$T_J = T_A + \theta_{JA} \times P_D$$

where:
θ_{JA} is the thermal resistance of the MOSFET package.
T_A is the ambient temperature.
P_D is the total power dissipated in the MOSFET.

LOOP COMPENSATION—VOLTAGE MODE

Set the controller to voltage mode operation by placing a 100 kΩ resistor between DL and PGND. Chose the larger possible ramp amplitude for the voltage mode below 1.5 V. The ramp voltage is programmed by a resistor value between V_{IN} and the RAMP pin:

$$R_{RAMP} = \frac{V_{IN} - 0.2\text{ V}}{100\text{ pF} \times f_{SW} \times V_{RAMP}}$$

The voltage at the RAMP pin is fixed at 0.2 V, and the current going into RAMP should be between 10 µA and 160 µA. Make sure that the following condition is satisfied:

$$10\,\mu\text{A} \le \frac{V_{IN} - 0.2\text{ V}}{R_{RAMP}} \le 160\,\mu\text{A} \quad (1)$$

For instance, with an input voltage of 12 V, R_{RAMP} should not be less than 73.8 kΩ.

Assuming that the LC filter design is complete, the feedback control system can be compensated. In general, aluminum electrolytic capacitors have high ESR; however, if several aluminum electrolytic capacitors are connected in parallel and produce a low effective ESR, then Type III compensation is needed. In addition, ceramic capacitors have very low ESR (only a few milliohms) making Type III compensation a better choice.

Type III Compensation

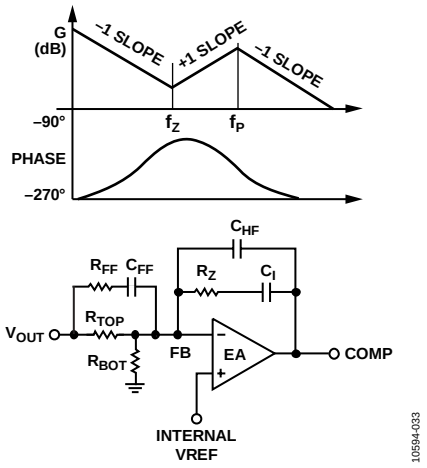


Figure 27. Type III Compensation

If the output capacitor ESR zero frequency is greater than ½ of the crossover frequency, use the Type III compensator as shown in Figure 27.

Calculate the output LC filter resonant frequency as follows:

$$f_{LC} = \frac{1}{2\pi\sqrt{LC}} \quad (2)$$

Chose a crossover frequency that is 1/10 of the switching frequency:

$$f_{CO} = \frac{f_{SW}}{10} \quad (3)$$

Set the poles and zeros as follows:

$$f_{P1} = f_{P2} = \frac{1}{2} f_{SW} \quad (4)$$

$$f_{Z1} = f_{Z2} = \frac{f_{CO}}{4} = \frac{f_{SW}}{40} = \frac{1}{2\pi R_Z C_I} \quad (5)$$

or

$$f_{Z1} = f_{Z2} = \frac{f_{LC}}{2} = \frac{1}{2\pi R_Z C_I} \quad (6)$$

Use the lower zero frequency from Equation 5 or Equation 6. Calculate the compensator resistor, R_Z, as follows:

$$R_Z = \frac{R_{TOP} V_{RAMP} f_{Z1} f_{CO}}{V_{IN} {f_{LC}}^2} \quad (7)$$

Next, calculate C_I:

$$C_I = \frac{1}{2\pi R_Z f_{Z1}} \quad (8)$$

Because of the finite output current drive of the error amplifier, C_I needs to be less than 10 nF. If it is larger than 10 nF, choose a larger R_{TOP} and recalculate R_Z and C_I until C_I is less than 10 nF.

Because C_{HF} << C_I, calculate C_{HF} as follows:

$$C_{HF} = \frac{1}{\pi f_{SW} R_Z} \quad (9)$$

Next, calculate the feedforward capacitor, C_{FF}, assuming R_{FF} << R_{TOP}:

$$R_{FF} = \frac{1}{\pi C_{FF} f_{SW}} \quad (10)$$

Check that the calculated component values are reasonable. For instance, capacitors smaller than about 10 pF should be avoided. In addition, R_Z values less than 3 kΩ and C_I values greater than 10 nF should be avoided. If necessary, recalculate the compensation network with a different starting value for R_{TOP}. If R_Z is too small or C_I is too big, start with a larger value for R_{TOP}. This compensation technique should yield a good working solution.

When precise compensation is needed, use the ADIsimPower design tool.

LOOP COMPENSATION—CURRENT MODE

Compensate the ADP1853 error voltage loop in current mode using Type II compensation.

Setting the Slope Compensation

In a current-mode control topology, slope compensation is needed to prevent subharmonic oscillations in the inductor current and to maintain a stable output. The external slope compensation is implemented by summing the amplified sense signal and a scaled voltage at the RAMP pin. To set the effective slope compensation, connect a resistor (R_{RAMP}) between the RAMP pin and the input voltage (V_{IN}). R_{RAMP} is calculated by

$$R_{RAMP} = \frac{7 \times 10^6 \times L}{A_{CS} \times R_{CS}}$$

where:
L is the inductor value measured in µH.
R_{CS} (mΩ) is resistance of the current sense element between CS and PGND (for instance, R_{DSON_MAX} is the low-side MOSFET maximum on resistance).
A_{CS} is the current sense amplifier gain and is 3 V/V, 6 V/V, or 12 V/V.

Thus, the voltage ramp amplitude, V_{RAMP}, is:

$$V_{RAMP} = \frac{V_{IN} - 0.2\ \text{V}}{100\ \text{pF} \times f_{SW} \times R_{RAMP}}$$

where 100 pF is the effective capacitance of the internal ramp capacitor, C_{RAMP}, with ±4% tolerance over the temperature and V_{IN} range.

The voltage at the RAMP pin is fixed at 0.2 V, and the current going into RAMP should be between 10 µA and 160 µA. Make sure that the following condition is satisfied:

$$10\ \mu\text{A} \le \frac{V_{IN} - 0.2\ \text{V}}{R_{RAMP}} \le 160\ \mu\text{A}$$

For instance, with an input voltage of 12 V, R_{RAMP} should not exceed 1.1 MΩ. If the calculated R_{RAMP} produces less than 10 µA, then select an R_{RAMP} value that produces between 10 µA and 15 µA.

Figure 28 illustrates the connection of the slope compensation resistor, R_{RAMP}, and the current sense gain resistor, R_{CSG}.

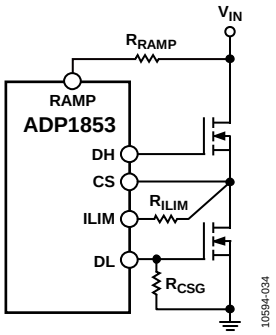


Figure 28. Slope Compensation and CS Gain Connection

Setting the Current Sense Gain

The voltage drop across the external low-side MOSFET is sensed by a current sense amplifier by multiplying the peak inductor current and the R_{DSON} of the MOSFET. The result is then amplified by a gain factor of 3 V/V, 6 V/V, or 12 V/V, which is programmable by an external resistor, R_{CSG}, connected to the DL pin. This gain is sensed only during power-up and not during normal operation. The amplified voltage is summed with the slope compensation ramp voltage and fed into the PWM controller for a stable regulation voltage.

The voltage range of the internal node, V_{CS}, is between 0.4 V and 2.2 V. Select the current sense gain such that the internal minimum amplified voltage (V_{CSMIN}) is above 0.4 V and the maximum amplified voltage (V_{CSMAX}) is 2.1 V. Note that V_{CSMIN} or V_{CSMAX} is not the same as V_{COMP}, which has a range of 0.85 V to 2.2 V. Make sure that the maximum V_{COMP} ($V_{COMPMAX}$) does not exceed 2.2 V to account for temperature and part-to-part variations. See the following equations for V_{CSMIN}, V_{CSMAX}, and $V_{COMPMAX}$:

$$V_{CSMIN} = 0.75\ \text{V} - \frac{1}{2} I_L \times R_{DSON\_MIN} \times A_{CS}$$

$$V_{CSMAX} = 0.75\ \text{V} + (I_{LOADMAX} - \frac{1}{2} I_L) \times R_{DSON\_MAX} \times A_{CS}$$

$$V_{COMPMAX} = \frac{(V_{IN} - 0.2\ \text{V}) \times t_{ON}}{100\ \text{pF} \times R_{RAMP}} + V_{CSMAX}$$

where:
V_{CSMIN} is the minimum amplified voltage of the internal current sense amplifier at zero output current.
I_L is the peak-to-peak ripple current in the inductor.
R_{DSON_MIN} is the low-side MOSFET minimum on resistance. The zero current level voltage of the current sense amplifier is 0.75 V.
V_{CSMAX} is the maximum amplified voltage of the internal current sense amplifier at the maximum output current.
$I_{LOADMAX}$ is the maximum output dc load current.
$V_{COMPMAX}$ is the maximum voltage at the COMP pin.
t_{ON} is the high-side driver (DH) on time.

Replace R_{DSON} with the resistance value of the current sense element, R_{CS}, if it is used.

Type II Compensation

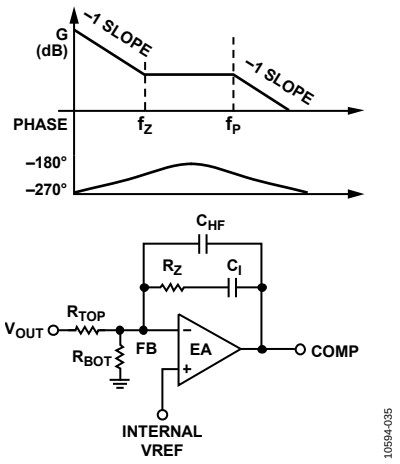


Figure 29. Type II Compensation

In this case, use the circuit shown in Figure 29. Calculate the compensation resistor, R_Z, with the following equation:

$$R_Z = R_{TOP} \times R_S \times 2\pi \times C_{OUT} f_{CO} \quad (11)$$

where:
f_{CO} is chosen to be 1/10 of f_{SW}.
$R_S = A_{CS} \times R_{DSON\_MIN}$.
A_{CS} is the current sense gain of either 3 V/V, 6 V/V, or 12 V/V, set by the gain resistor between DL and PGND.
R_{DSON_MIN} is the low-side MOSFET minimum on resistance.

If the current is sensed on a current sense resistor, R_{CS}, then R_{CS} becomes

$$R_S = A_{CS} \times R_{CS}$$

Next, choose the compensation capacitor to set the compensation zero, f_{Z1}, to the lesser of 1/5 of the crossover frequency or ½ of the LC resonant frequency

$$f_{Z1} = \frac{f_{CO}}{5} = \frac{f_{SW}}{50} = \frac{1}{2\pi R_Z C_I} \quad (12)$$

or

$$f_{Z1} = \frac{f_{LC}}{2} = \frac{1}{2\pi R_Z C_I} \quad (13)$$

Solving for C_I in Equation 12 yields

$$C_I = \frac{25}{\pi R_Z f_{SW}} \quad (14)$$

Solving for C_I in Equation 13 yields

$$C_I = \frac{1}{\pi R_Z f_{LC}} \quad (15)$$

Use the larger value of C_I from Equation 14 or Equation 15. Because of the finite output current drive of the error amplifier, C_I needs to be less than 10 nF. If it is larger than 10 nF, choose a larger R_{TOP} and recalculate R_Z and C_I until C_I is less than 10 nF.

Next, choose the high frequency pole, f_{P1}, to be ½ of f_{SW}.

$$f_{P1} = \frac{1}{2} f_{SW} \quad (16)$$

Because $C_{HF} << C_I$,

$$f_{P1} = \frac{1}{2\pi R_Z C_{HF}} \quad (17)$$

Combine Equation 16 and Equation 17, and solve for C_{HF},

$$C_{HF} = \frac{1}{\pi f_{SW} R_Z} \quad (18)$$

For maximally precise compensation solutions, use the ADIsimPower design tool.

SWITCHING NOISE AND OVERSHOOT REDUCTION

To reduce voltage ringing and noise, it is recommended to add an RC snubber between SW and PGND for high current applications, as illustrated in Figure 30.

In most applications, R_{SNUB} is typically 2 Ω to 4 Ω, and C_{SNUB} is typically 1.2 nF to 3 nF.

The size of the RC snubber components must be chosen correctly to handle the power dissipation. The power dissipated in R_{SNUB} is

$$P_{SNUB} = V_{IN}{}^2 \times C_{SNUB} \times f_{SW}$$

In most applications, a component size of 0805 for R_{SNUB} is sufficient. The RC snubber does not reduce the voltage overshoot. A resistor, shown as R_{RISE} in Figure 30, at the BST pin helps to reduce overshoot and is generally between 2 Ω and 4 Ω. Adding a resistor in series, typically between 2 Ω and 4 Ω, with the gate driver also helps to reduce overshoot. If a gate resistor is added, then R_{RISE} is not needed.

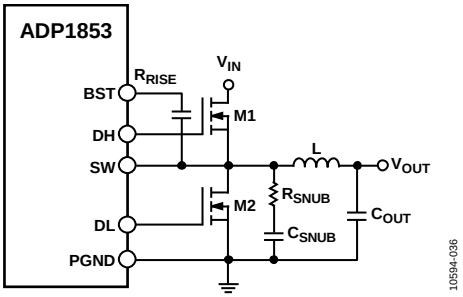


Figure 30. Application Circuit with a Snubber

VOLTAGE TRACKING

The ADP1853 includes a tracking feature that tracks a master voltage. In all tracking configurations, the output can be set as low as 0.6 V for a given operating condition. The soft start time setting of the master voltage should be longer than the soft start of the slave voltage. This forces the rise time of the master voltage to be imposed on the slave voltage. If the soft start setting of the slave voltage is longer, the slave comes up more slowly, and the tracking relationship is not seen at the output.

Two tracking configurations are possible with the ADP1853: coincident and ratiometric tracking.

Coincident Tracking

The most common application is coincident tracking, used in core vs. I/O voltage sequencing and similar applications. Coincident tracking forces the ramp rate of the output voltage to be the same for the master and slave until the slave output reaches its regulation. Connect the slave TRK input to a resistor divider from the master voltage that is the same as the divider used on the slave FB pin. This forces the slave voltage to be the same as the master voltage. For coincident tracking, use $R_{TRKT} = R_{TOP}$ and $R_{TRKB} = R_{BOT}$, as shown in Figure 32.

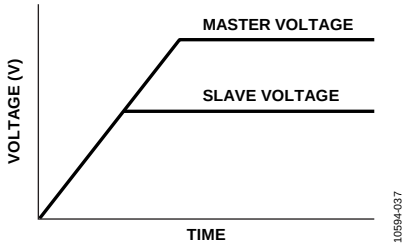


Figure 31. Coincident Tracking

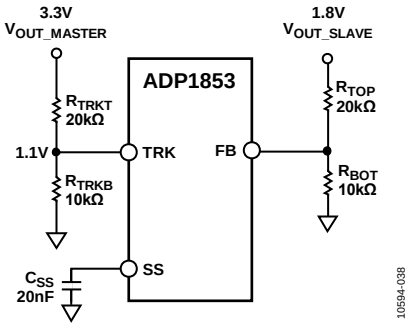


Figure 32. Example of a Coincident Tracking Circuit

The ratio of the slave output voltage to the master voltage is a function of the two dividers.

$$\frac{V_{OUT\_SLAVE}}{V_{OUT\_MASTER}} = \frac{\left(1 + \frac{R_{TOP}}{R_{BOT}}\right)}{\left(1 + \frac{R_{TRKT}}{R_{TRKB}}\right)}$$

As the master voltage rises, the slave voltage rises identically. Eventually, the slave voltage reaches its regulation voltage, where the internal reference takes over the regulation while the TRK input continues to increase, thus removing itself from influencing the output voltage.

To ensure that the output voltage accuracy is not compromised by the TRK pin being too close in voltage to the reference voltage (V_{FB}, typically 0.6 V), make sure that the final value of the TRK voltage of the slave channel is at least 30 mV above V_{FB}.

Ratiometric Tracking

Ratiometric tracking limits the output voltage to a fraction of the master voltage, as illustrated in Figure 33 and Figure 34. The final TRK voltage of the slave channel should be set to at least 30 mV below the FB voltage of the master channel. When the TRK voltage of the slave channel drops to a level that is below the minimum on time condition, the slave channel operates in pulse skip mode while keeping the output regulated and tracked to the master channel. In addition, when TRK or FB drops below the PGOOD undervoltage threshold, the PGOOD signal is tripped and becomes active low.

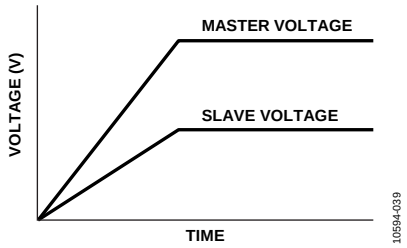


Figure 33. Ratiometric Tracking

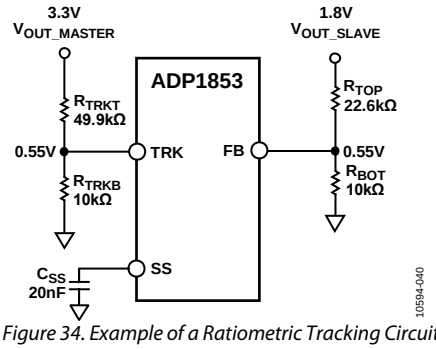
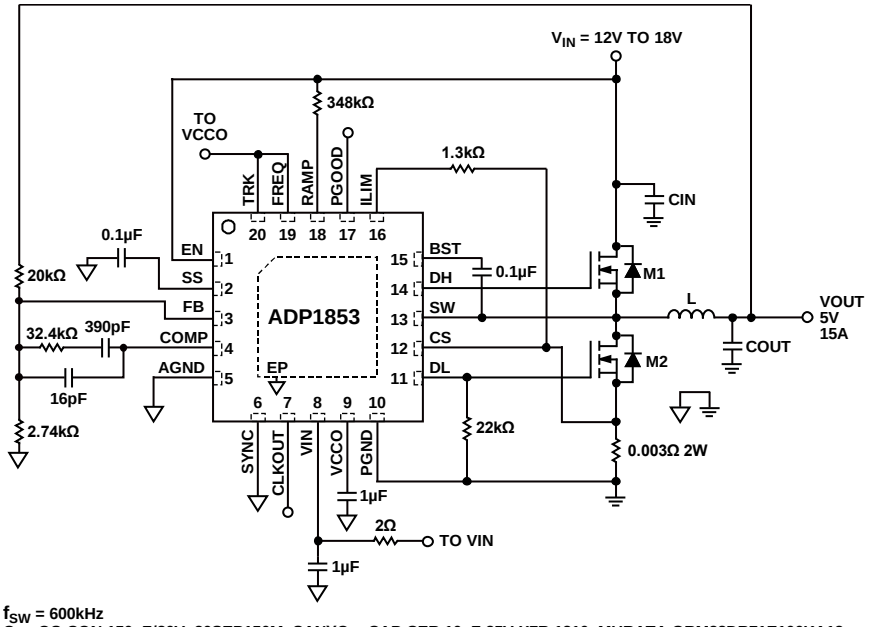


Figure 34. Example of a Ratiometric Tracking Circuit

PCB LAYOUT GUIDLINES

The recommended board layout practices for the synchronous buck controller are described in the AN-1119 Application Note.

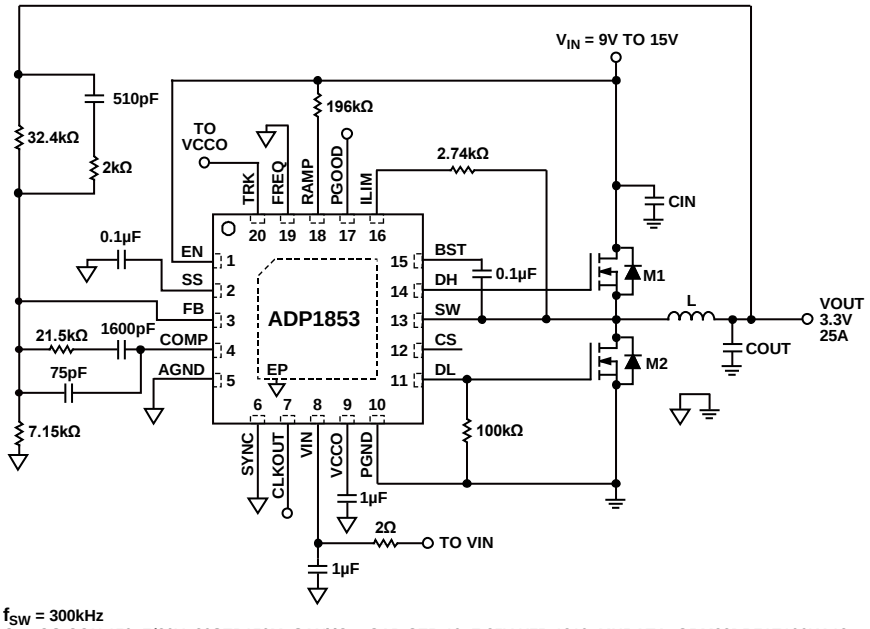
TYPICAL OPERATING CIRCUITS



f_{SW} = 600kHz
C_{IN}: OS-CON 150µF/20V, 20SEP150M, SANYO + CAP CER 10µF 25V X7R 1210, MURATA GRM32DR71E106KA12
L: 1.8µH WURTH ELECTRONIK WE-HCI 1050 744 325 180
M1: VISHAY SILICONIX SiR462DP
M2: VISHAY SILICONIX SiR866DP
C_{OUT}: POSCAP 100µF/6.3V SANYO 6TPE100MI + 2× CAP CER 22µF 10V X5R 1210 MURATA GRM32ER61A226KE20L

10594-041

Figure 35. 15 A Circuit Operating in Current Mode



f_{SW} = 300kHz
C_{IN}: OS-CON 150µF/20V, 20SEP150M, SANYO + CAP CER 10µF 25V X7R 1210, MURATA GRM32DR71E106KA12
L: 1µH COILCRAFT SER1412-102ME
M1: INFINEON BSC052N03LS
M2: INFINEON BSC0902NS
C_{OUT}: POSCAP 330µF/6.3V SANYO 6TPE330MFL + CAP CER 22µF 10V X5R 1210 MURATA GRM32ER61A226KE20L

Figure 36. 25 A Circuit Operating in Voltage Mode

OUTLINE DIMENSIONS

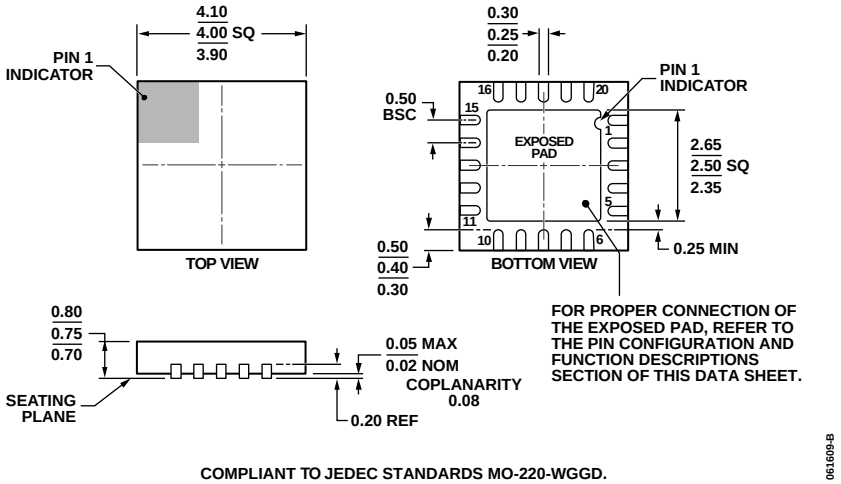


Figure 37. 20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-20-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADP1853ACPZ-R7	−40°C to +125°C	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-10

[1] Z = RoHS Compliant Part.

NOTES

D10594-0-5/12(0)