200 MHz, 16 × 16 Buffered Video Crosspoint Switch

AD8116

FEATURES

- **Large 16 × 16 High Speed Nonblocking Switch Array**
- **Switch Array Controllable via an 80-Bit Serial Word**
- **Serial Data Out Allows "Daisy Chaining" of Multiple AD8116s to Create Large Switch Arrays Over 256 × 256**
- **Complete Solution**
  - **Buffered Inputs**
  - **16 Individual Output Amplifiers**
  - **Drives 150 Ω Loads**
- **Excellent Video Performance**
  - **60 MHz 0.1 dB Gain Flatness**
  - **0.01% Differential Gain Error (R_L = 150 Ω)**
  - **0.01° Differential Phase Error (R_L = 150 Ω)**
- **Excellent AC Performance**
  - **200 MHz –3 dB Bandwidth**
  - **300 V/μs Slew Rate**
- **Low Power of 900 mW (3.5 mW per Point)**
- **Low All Hostile Crosstalk of –70 dB @ 5 MHz**
- **Output Disable Allows Direct Connection of Multiple Device Outputs**
- **Chip Enable Allows Selection of Individual AD8116s in Large Arrays (or Parallel Programming of AD8116s)**
- **Reset Pin Allows Disabling of All Outputs (Connected Through a Capacitor to Ground Provides "Power-On" Reset Capability)**
- **128-Lead LQFP Package (14 mm × 14 mm)**

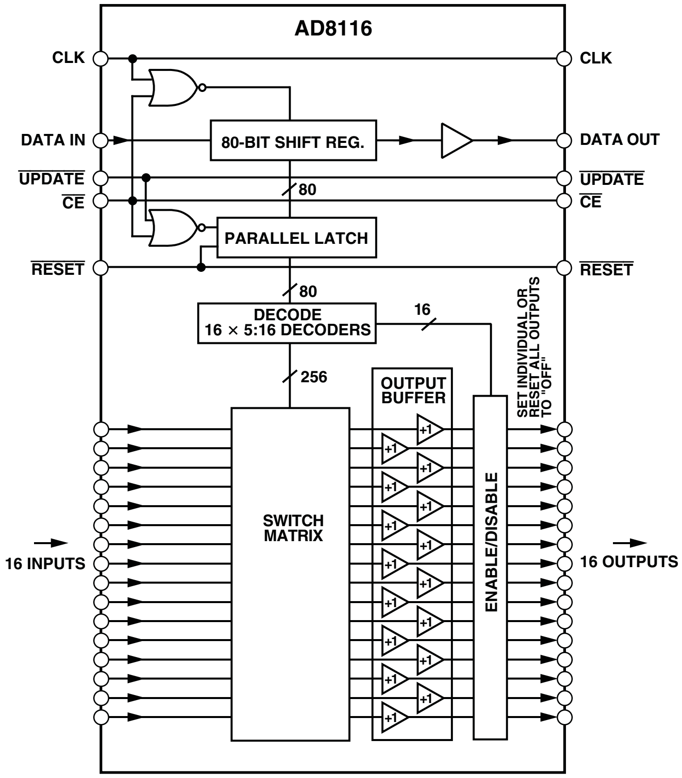
APPLICATIONS

- **Routing of High Speed Signals Including:**
  - **Composite Video (NTSC, PAL, S, SECAM, etc.)**
  - **Component Video (YUV, RGB, etc.)**
  - **3-Level Digital (HDB3)**
- **Video on Demand**
- **Ultrasound**
- **Communication Satellites**

PRODUCT DESCRIPTION

The AD8116 is a high speed 16 × 16 video crosspoint switch matrix. It offers a –3 dB signal bandwidth greater than 200 MHz and channel switch times of 60 ns with 0.1% settling. With –70 dB of crosstalk and –112 dB of isolation (@ 5 MHz), the AD8116 is useful in many high speed applications. The differential gain and differential phase errors of better than 0.01% and 0.01°, respectively, along with 0.1 dB flatness out to 60 MHz make the AD8116 ideal for video signal switching.

FUNCTIONAL BLOCK DIAGRAM



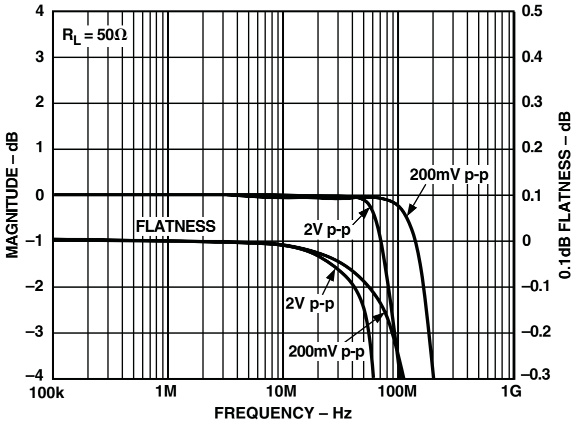


Figure 1. Frequency Response

The AD8116 includes output buffers that can be placed into a high impedance state for paralleling crosspoint outputs so that off channels do not load the output bus. It operates on voltage supplies of ±5 V while consuming only 90 mA of idle current. The channel switching is performed via a serial digital control that can accommodate "daisy chaining" of several devices.

The AD8116 is packaged in a 128-lead LQFP package occupying only 0.36 square inches, and is specified over the commercial temperature range of 0°C to 70°C.

Rev. C

Document Feedback

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Documentation

Application Notes

- AN-282: Fundamentals of Sampled Data Systems
- AN-348: Avoiding Passive-Component Pitfalls

Data Sheet

- AD8116: 200 MHz, 16 x 16 Buffered Video Crosspoint Switch Data Sheet

Tools and Simulations

- AD8116 SPICE Macro-Model

Reference Materials

Product Selection Guide

- High Speed Switches

Technical Articles

- CMOS Switches Offer High Performance in Low Power, Wideband Applications
- Data-acquisition system uses fault protection
- Enhanced Multiplexing for MEMS Optical Cross Connects

Design Resources

- AD8116 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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AD8116–SPECIFICATIONS (V_S = ±5 V, T_A = 25°C, R_L = 1 kΩ unless otherwise noted.)

Parameter	Conditions		Limit		Unit	Reference Figure
		Min	Typ	Max		
DYNAMIC PERFORMANCE						
–3 dB Bandwidth	200 mV p-p, R_L = 150 Ω		200		MHz	1
	1 V p-p, R_L = 150 Ω		120		MHz	
	2 V p-p, R_L = 150 Ω		80		MHz	1
Slew Rate	2 V Step, R_L = 150 Ω		300		V/µs	5
Settling Time	0.1%, 2 V Step, R_L = 150 Ω		60		ns	6
Gain Flatness	0.05 dB, 200 mV p-p, R_L = 150 Ω		25		MHz	1
	0.05 dB, 2 V p-p, R_L = 150 Ω		20		MHz	1
	0.1 dB, 200 mV p-p, R_L = 150 Ω		60		MHz	1
	0.1 dB, 2 V p-p, R_L = 150 Ω		45		MHz	1
NOISE/DISTORTION PERFORMANCE						
Differential Gain Error	NTSC or PAL, R_L = 1 kΩ		0.01		%	
	NTSC or PAL, R_L = 150 Ω		0.01		%	
Differential Phase Error	NTSC or PAL, R_L = 1 kΩ		0.01		Degrees	
	NTSC or PAL, R_L = 150 Ω		0.01		Degrees	
Crosstalk, All Hostile	f = 5 MHz		–70		dB	2
	f = 10 MHz		–60		dB	2
Off Isolation, Input-Output	f = 5 MHz, R_L = 150 Ω, One Channel		–112		dB	11
Input Voltage Noise	0.01 MHz to 50 MHz		15		nV/$\sqrt{\text{Hz}}$	8
DC PERFORMANCE						
Gain	No Load	0.995	0.999	1.000	V/V	
	R_L = 1 kΩ	0.992	0.999	1.000	V/V	
Gain Matching	No Load, Ch-Ch			0.15	%	
	R_L = 1 kΩ, Ch-Ch			0.5	%	
OUTPUT CHARACTERISTICS						
Output Offset Voltage	Worst-Case All Switch Configurations		15	45	mV	17
Output Impedance	DC, Enabled		0.2		Ω	12
	Disabled	1	10		MΩ	9
Output Disable Capacitance			3		pF	9
Output Leakage Current	Disabled		1		µA	
Output Voltage Range		±2.5	±3		V	
Output Current		20	40		mA	
Short Circuit Current			65		mA	
INPUT CHARACTERISTICS						
Input Voltage Range		±2.5	±3		V	
Input Capacitance	Any Switch Configuration		5		pF	13
Input Resistance		1	10		MΩ	13
Input Bias Current			2	5	µA	
SWITCHING CHARACTERISTICS						
Enable On Time			60		ns	
Switching Time	50% $\overline{\text{UPDATE}}$ to 1% Output Settling, 2 V Step		50		ns	16
Switching Transient (Glitch)			15		mV p-p	10
POWER SUPPLIES						
Supply Current	AVCC, Outputs Enabled, No Load		75	95	mA	
	Outputs Disabled		25		mA	
	AVEE, Outputs Enabled, No Load		70	95	mA	
	Outputs Disabled		22.5		mA	
	DVCC, Outputs Enabled, No Load		25	35	mA	
	DVEE, Outputs Enabled, No Load		10	15	mA	
Supply Voltage Range			±4.5 to ±5.5		V	
PSRR	f = 100 kHz		60		dB	7
	f = 1 MHz		40		dB	7
OPERATING TEMPERATURE RANGE						
Temperature Range	Operating (Still Air)		0 to 70		°C	
θ_{JA}	Operating (Still Air)		37		°C/W	

Specifications subject to change without notice.

TIMING CHARACTERISTICS

Parameter	Symbol	Limit			Unit
		Min	Typ	Max	
Data Setup Time	t_1	20			ns
CLK Pulsewidth	t_2	100			ns
Data Hold Time	t_3	20			ns
CLK Pulse Separation	t_4	100			ns
CLK to $\overline{\text{UPDATE}}$ Delay	t_5	0			ns
$\overline{\text{UPDATE}}$ Pulsewidth	t_6	50			ns
CLK to DATA OUT Valid	t_7			200	ns
Propagation Delay, $\overline{\text{UPDATE}}$ to Switch On or Off	–			50	ns
Data Load Time, CLK = 5 MHz	–		16		µs
CLK, $\overline{\text{UPDATE}}$ Rise and Fall Times	–			100	ns
$\overline{\text{RESET}}$ Time	–			200	ns

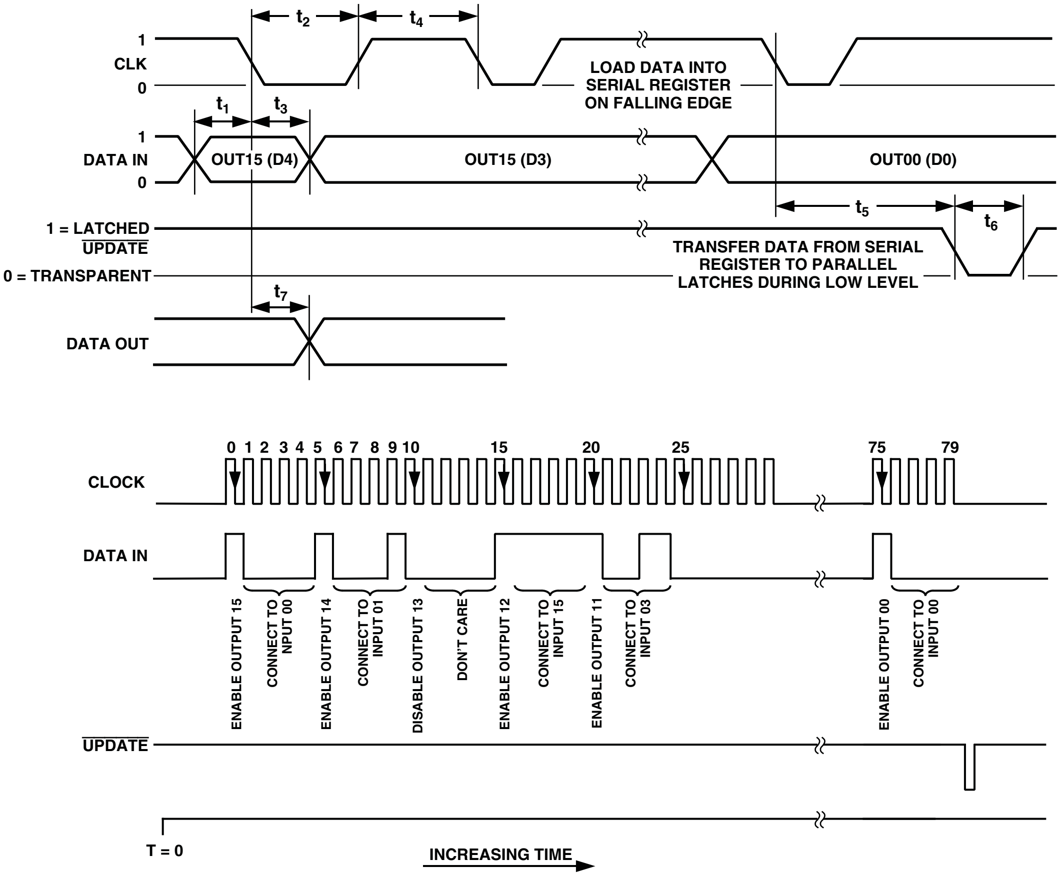


Figure 2. Timing Diagram and Programming Example

Table I. Logic Levels

V_{IH}	V_{IL}	V_{OH}	V_{OL}	I_{IH}	I_{IL}	I_{OH}	I_{OL}
CLK, DATA IN, $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	CLK, DATA IN, $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	DATA OUT	DATA OUT	CLK, DATA IN, $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	CLK, DATA IN, $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	DATA OUT	DATA OUT
2.0 V min	0.8 V max	2.7 V min	0.5 V max	20 µA max	–400 µA min	–400 µA max	3.0 mA min

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . 12.0 V
Internal Power Dissipation[2]
  AD8116 128-Lead Plastic LQFP (ST) . . . . 3.5 W
Input Voltage . . . . ±V_S
Output Short Circuit Duration
  . . . . Observe Power Derating Curves
Storage Temperature Range . . . . –65°C to +125°C
Lead Temperature Range (Soldering 10 sec) . . . . 300°C

NOTES

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2] Specification is for device in free air (T_A = 25°C):
128-lead plastic LQFP (ST): θ_{JA} = 37°C/W.

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8116 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure.

While the AD8116 is internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (150°C) is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the maximum power derating curves shown in Figure 3.

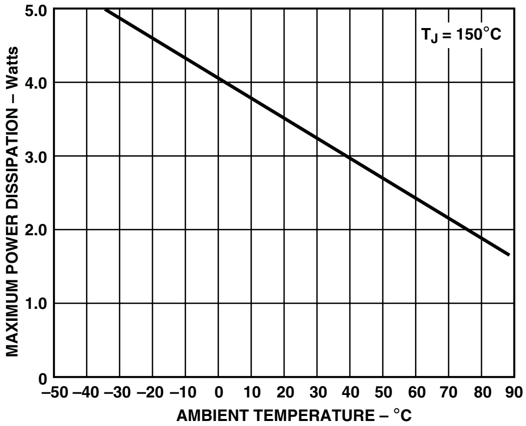


Figure 3. Maximum Power Dissipation vs. Temperature

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8116 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Table II. Operation Truth Table

Control Lines

$\overline{\text{CE}}$	$\overline{\text{UPDATE}}$	CLK	DATA IN	DATA OUT	$\overline{\text{RESET}}$	Operation/Comment
1	X	X	X	X	1	No change in logic.
0	1	↓	Data $_i$	Data $_{i-80}$	1	The data on the DATA IN line is loaded into the serial register. The first bit clocked into the serial register appears at DATA OUT 80 clocks later.
0	0	X	X	X	1	Data in the serial shift register transfers into the parallel latches that control the switch array. Latches are transparent.
X	X	X	X	X	0	Asynchronous operation. All outputs are disabled. Remainder of logic is unchanged.

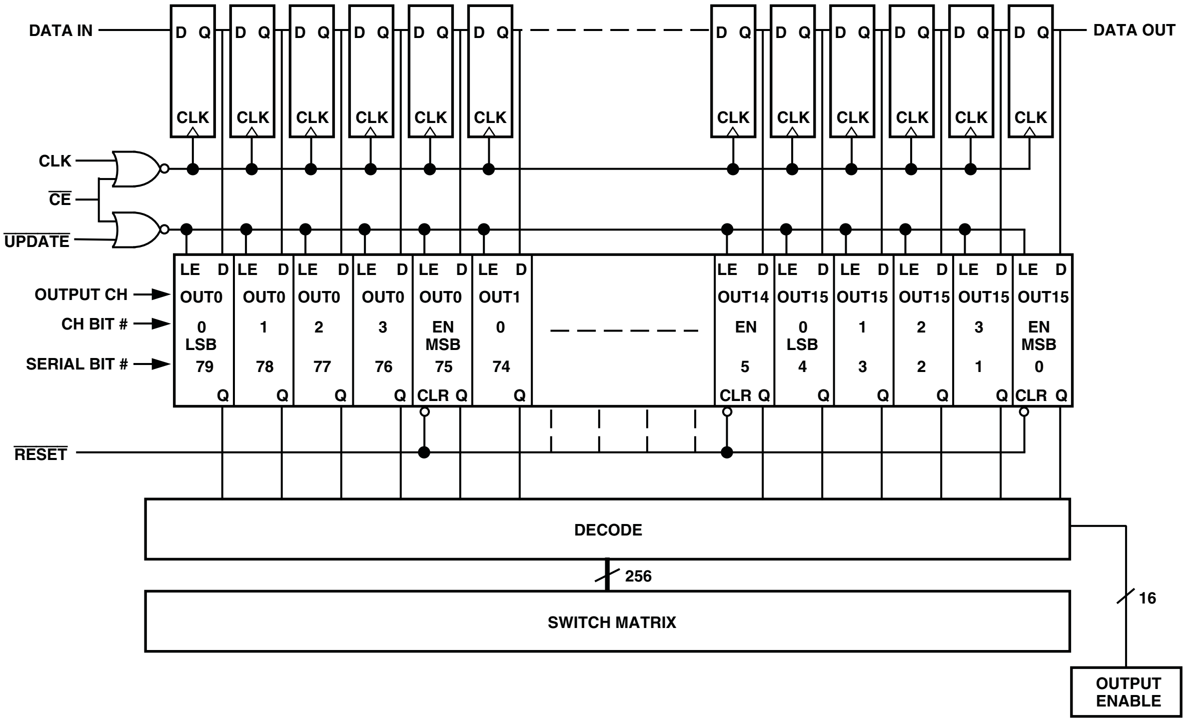
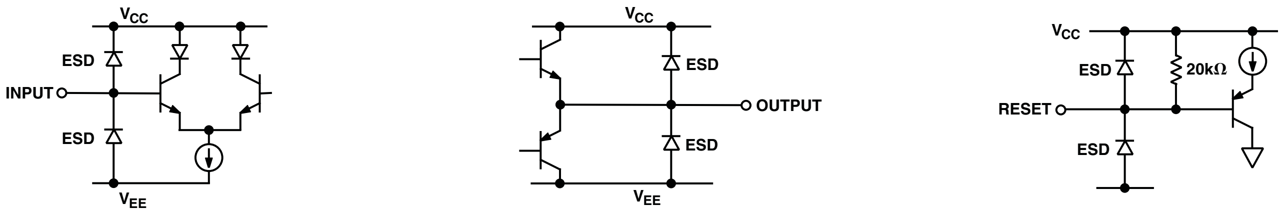


Figure 4. Logic Diagram

PIN FUNCTION DESCRIPTIONS

Pin Name	Pin Numbers	Pin Description
INxx	2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30, 32	Analog Inputs; xx = Channel No. 00 thru 15.
DATA IN	37, 126	Serial Data Input, TTL Compatible.
CLK	36, 125	Serial Clock, TTL Compatible. Falling edge triggered.
DATA OUT	35, 124	Serial Data Out, TTL Compatible.
$\overline{\text{UPDATE}}$	38, 123	Enable (Transparent) "Low." Allows serial register to connect directly to switch matrix. Data latched when "high."
$\overline{\text{RESET}}$	39, 122	Disable Outputs, Enable "Low."
$\overline{\text{CE}}$	40, 121	Chip Enable, Enable "Low." *Must be "low" to clock in & latch data.*
OUTyy	65, 67, 69, 71, 73, 75, 77, 79, 81, 83, 85, 87, 89, 91, 93, 95	Analog Outputs yy = Channel Nos. 00 thru 15.
AGND	1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31, 33, 128	Analog Ground for inputs and switch matrix.
DVCC	34, 127	+5 V for Digital Circuitry.
DGND	41, 120	Ground for Digital Circuitry.
DVEE	42, 119	–5 V for Digital Circuitry.
AVEE	43, 44, 45, 116, 117, 118	–5 V for Inputs and Switch Matrix.
AVCC	46, 47, 48, 113, 114, 115	+5 V for Inputs and Switch Matrix.
AGNDxx	56–63, 97–104	Ground for Output Amp, xx = Output Channel Nos. 00 thru 15. *Must be connected.*
AVCC00	96	+5 V for Output Channel 00. *Must be connected.*
AVCC15	64	+5 V for Output Channel 15. *Must be connected.*
AVCCxx/yy	68, 72, 76, 80, 84, 88, 92	+5 V for Output Amplifier that is shared by Channel Nos. xx and yy. *Must be connected.*
AVEExx/yy	66, 70, 74, 78, 82, 86, 90, 94	–5 V for Output Amplifier that is shared by Channel Nos. xx and yy. *Must be connected.*

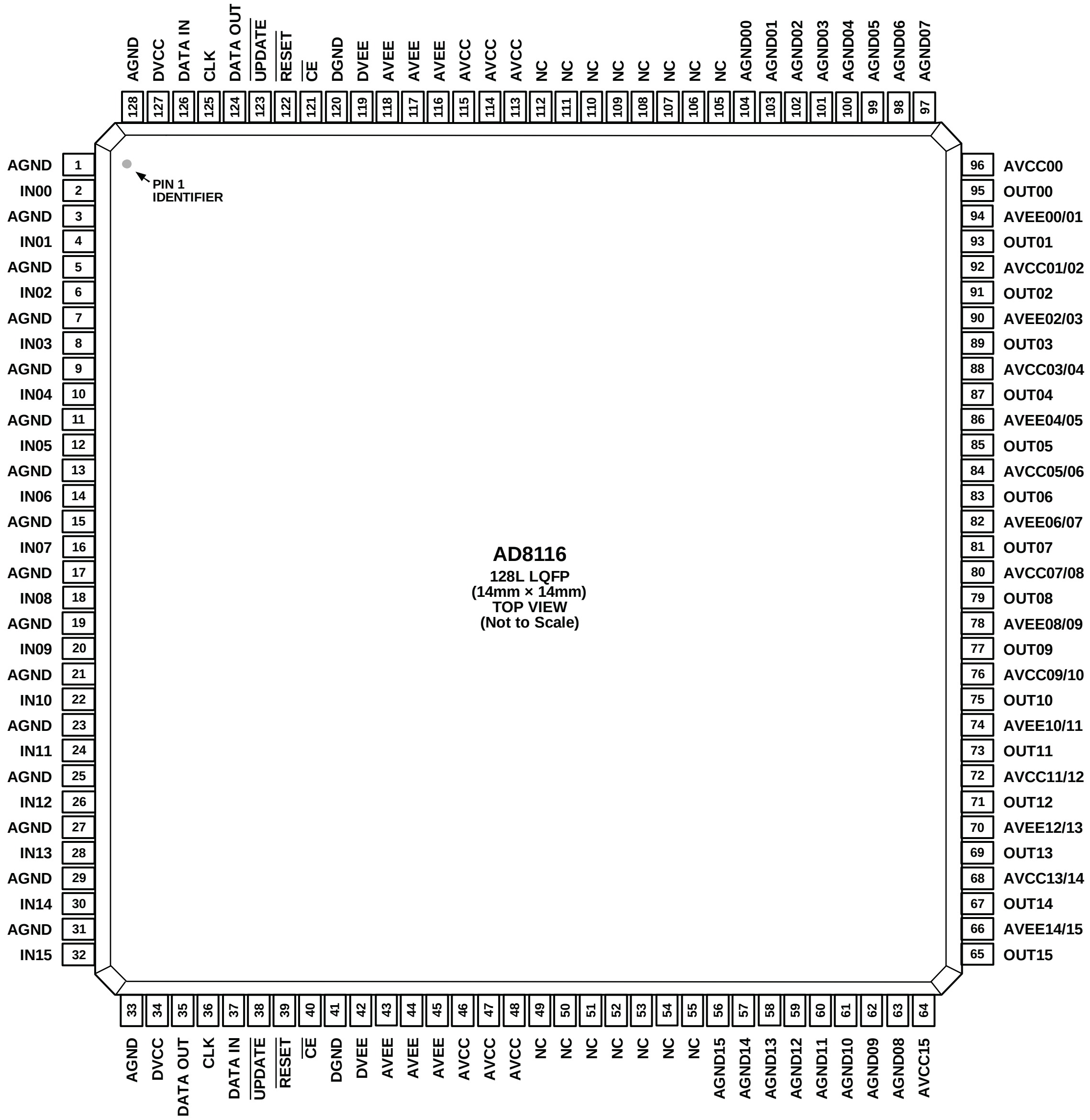


a. *Analog Input*   b. *Analog Output*   c. *Reset Input*

d. *Logic Input*   e. *Logic Output*

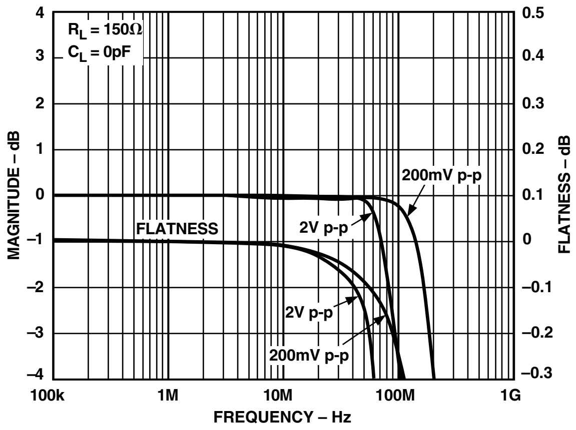
Figure 5. I/O Pin Schematics

PIN CONFIGURATION

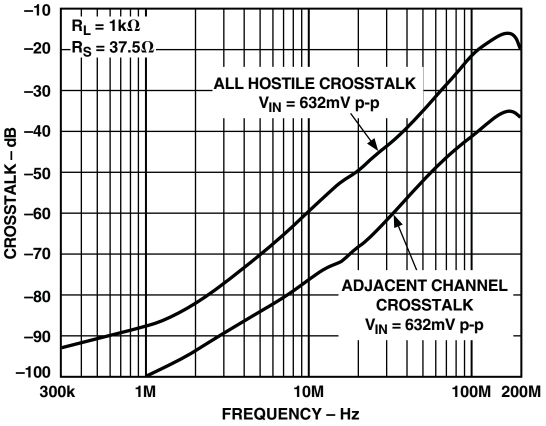


NC = NO CONNECT

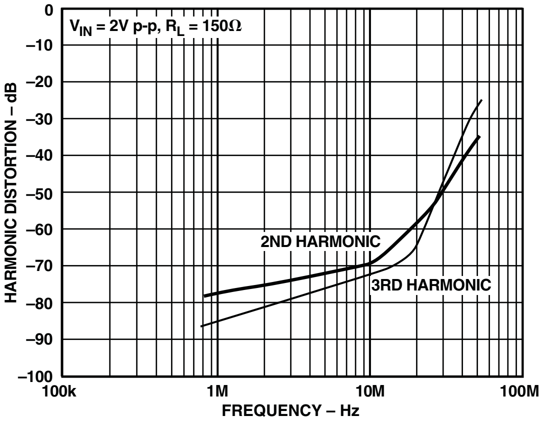
AD8116–Typical Performance Characteristics



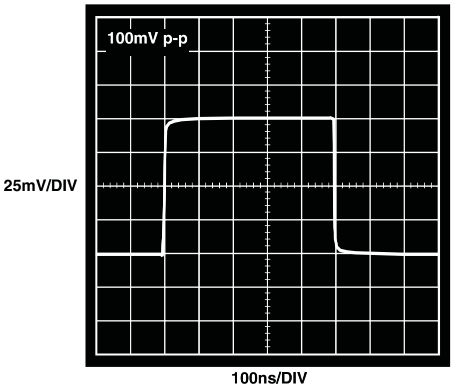
TPC 1. Frequency Response



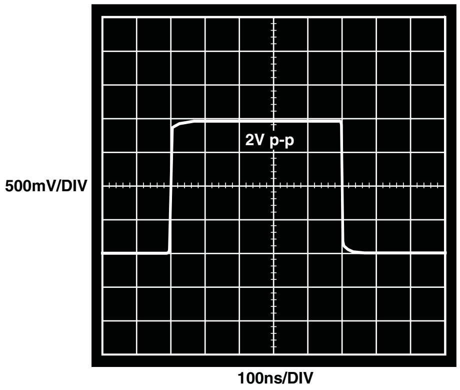
TPC 2. Crosstalk vs. Frequency



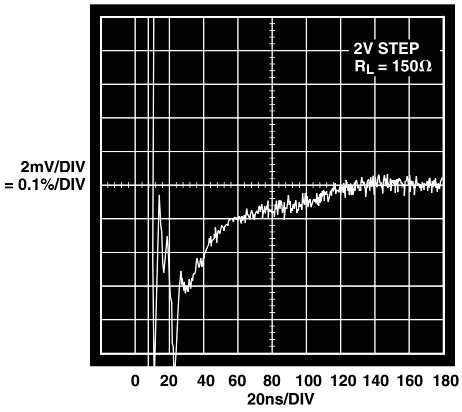
TPC 3. Total Harmonic Distortion



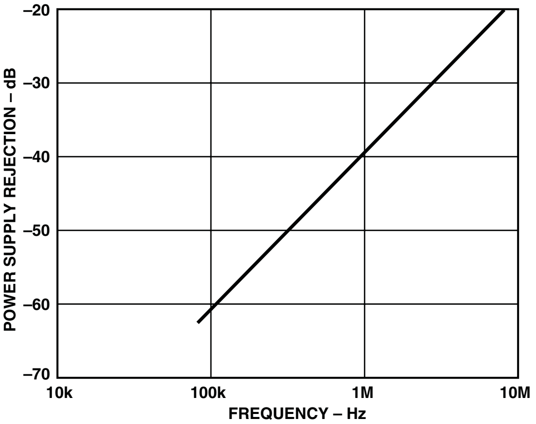
TPC 4. Step Response, 100 mV Step



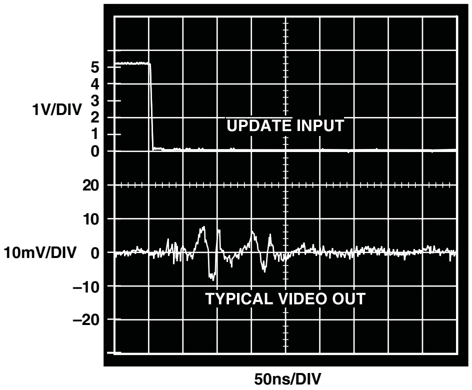
TPC 5. Step Response, 2 V Step



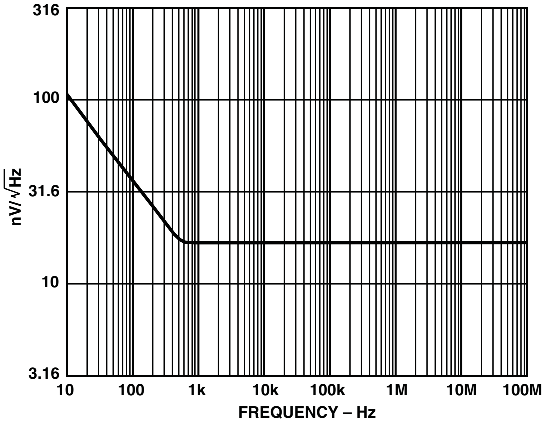
TPC 6. Settling Time



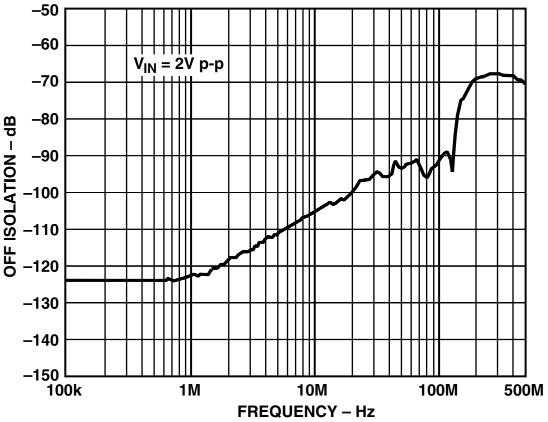
TPC 7. PSRR vs. Frequency



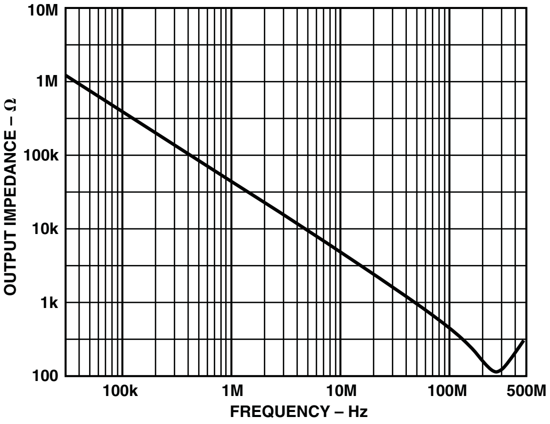
TPC 10. Switching Transient (Glitch)



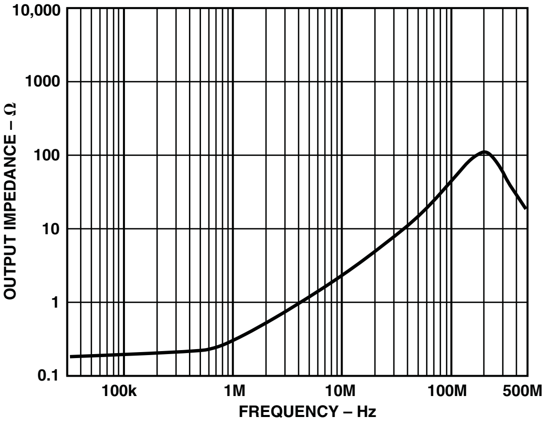
TPC 8. Voltage Noise vs. Frequency



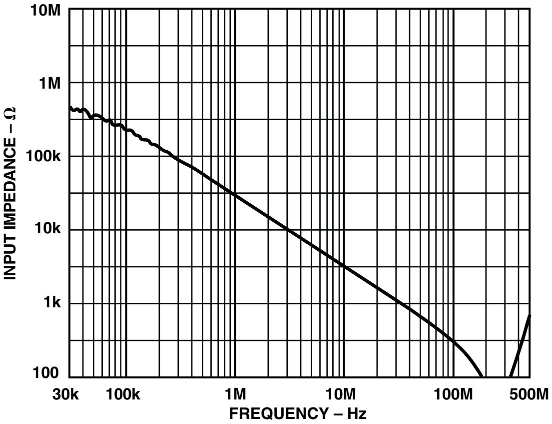
TPC 11. Off Isolation, Input-Output



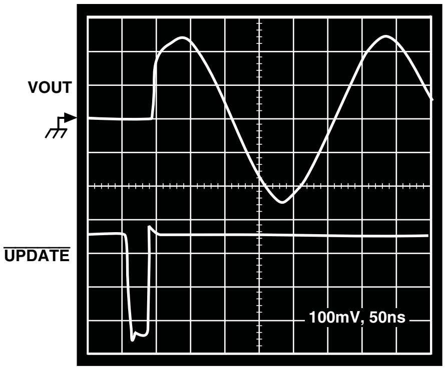
TPC 9. Output Impedance, Disabled



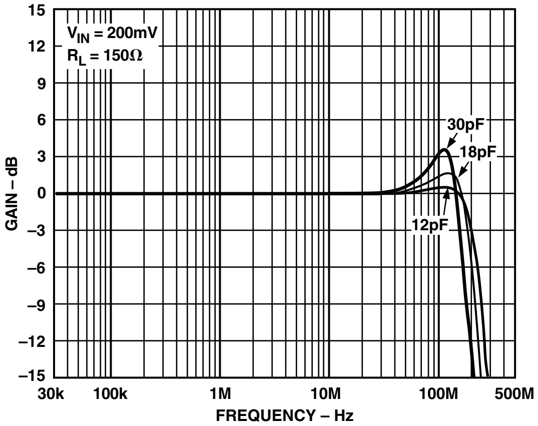
TPC 12. Output Impedance, Enabled



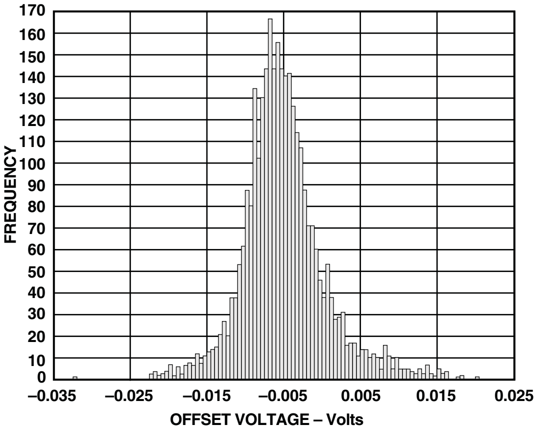
TPC 13. Input Impedance vs. Frequency



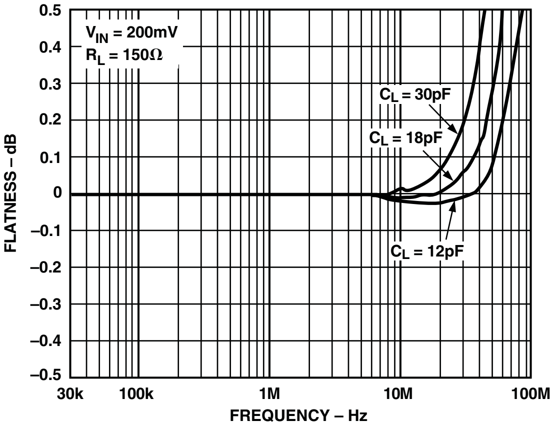
TPC 16. Switching Time



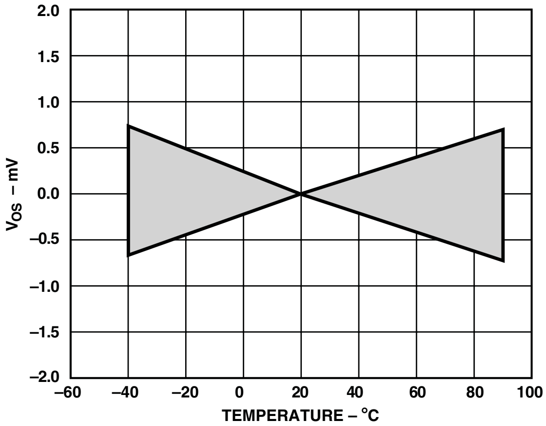
TPC 14. Frequency Response vs. Capacitive Load



TPC 17. Offset Voltage Distribution



TPC 15. Flatness vs. Capacitive Load



TPC 18. Offset Voltage Drift vs. Temperature

THEORY OF OPERATION

Loading Data

Data to control the switches is clocked serially into an 80-bit shift register and then transferred in parallel to an 80-bit latch. The falling edge of CLK (the serial clock input) loads data into the shift register. The first five bits of the 80 bits are loaded via DATA IN (the serial data input) program OUT15. The first of the five bits (D4) enables or disables the output. The next four bits (D3–D0, D3 = MSB, D0 = LSB) determine which one of the 16 inputs will be connected to OUT15 (only one of the 16 inputs can be connected to a given output). The remaining bits program OUT14 through OUT00.

After the shift register is filled with the new 80 bits of control data, $\overline{\text{UPDATE}}$ is activated (low) to transfer the data to the parallel latches. The switch control latches are static and will hold their data as long as power is applied.

To extend the number of switches in an array, the DATA OUT and DATA IN pins of multiple AD8116s can be daisy-chained together. The DATA OUT pin is the end of the shift register and may be directly connected to the DATA IN pin of the follow-on AD8116. $\overline{\text{CE}}$ can be used to control the clocking of data into selected devices.

Serial Logic

The AD8116 employs a serial interface for programming the state of the crosspoint array. The 80-bit shift register (Figure 4) consists of static D flip-flops while the parallel latch uses transparent latches that are latched by a logic high state of $\overline{\text{UPDATE}}$, and transparent on logic low of the same signal. The 4-to-16 decoder is a small current-mode multilevel gate array that steers a small select current to the selected point in the crosspoint array.

The $\overline{\text{RESET}}$ signal is connected to only the enable/disable bit on each output buffer. This means that the AD8116 will have a random configuration on power-up. In normal operation though, $\overline{\text{RESET}}$ and $\overline{\text{UPDATE}}$ can be used together to alternately enable and disable an entire array at once, if desired.

Separate chip enable ($\overline{\text{CE}}$), update ($\overline{\text{UPDATE}}$) and serial data out (DATA OUT) signals allow several options for programming larger arrays of AD8116s. The function of each bit in the 80-bit word that programs the state of the AD8116 is shown in Figure 4. In normal operation, the DATA OUT pin of one AD8116 is connected to the DATA IN of the next. In this way, for example, an array of eight AD8116s would be programmed with one 640-bit sequence. In this mode $\overline{\text{CE}}$ is logic low and the CLK and $\overline{\text{UPDATE}}$ pins are connected in parallel.

In one alternate mode of programming, the $\overline{\text{CE}}$ pin can be used to select one AD8116 at a time. This might be desirable when the ability to program just one device at a time is required. In this mode CLK, $\overline{\text{UPDATE}}$ and DATA IN are all connected in parallel. The user then selects each AD8116 in turn (with the $\overline{\text{CE}}$ signal) and programs it with the desired data. Larger arrays can also be programmed by connecting each DATA IN signal to a larger parallel bus. In this way only 80 clock cycles would be needed to program the entire array. The logic signals are configured so that all programming can be accomplished with synchronous logic and a continuous clock, so that no missing cycles or delays need be generated.

APPLICATIONS

Multichannel Video

The excellent video specifications of the AD8116 make it an ideal candidate for creating composite video crosspoint switches. These can be made quite dense by taking advantage of the AD8116's high level of integration and the fact that composite video requires only one crosspoint channel per system video channel. There are, however, other video formats that can be routed with the AD8116 requiring more than one crosspoint channel per video channel.

Some systems use twisted pair wiring to carry video signals. These systems utilize differential signals and can lower costs because they use lower cost cables, connectors and termination methods. They also have the ability to lower crosstalk and reject common-mode signals, which can be important for equipment that operates in noisy environments or where common-mode voltages are present between transmitting and receiving equipment.

In such systems, the video signals are differential; there is a positive and negative (or inverted) version of the signals. These complementary signals are transmitted onto each of the two wires of the twisted pair, yielding a first order zero common-mode voltage. At the receive end, the signals are differentially received and converted back into a single-ended signal.

When switching these differential signals, two channels are required in the switching element to handle the two differential signals that make up the video channel. Thus, one differential video channel is assigned to a pair of crosspoint channels, both input and output. For a single AD8116, eight differential video channels can be assigned to the 16 inputs and 16 outputs. This will effectively form an 8 × 8 differential crosspoint switch.

Programming such a device will require that inputs and outputs be programmed in pairs. This information can be deduced by inspection of the programming format of the AD8116 and the requirements of the system.

There are other analog video formats requiring more than one analog circuit per video channel. One two-circuit format that is more commonly being used in systems such as satellite TV, digital cable boxes and higher quality VCRs, is called S-video or Y/C video. This format carries the brightness (luminance or Y) portion of the video signal on one channel and the color (chrominance or C) on a second channel.

Since S-video also uses two separate circuits for one video channel, creating a crosspoint system requires assigning one video channel to two crosspoint channels as in the case of a differential video system. Aside from the nature of the video format, other aspects of these two systems will be the same.

There are yet other video formats using three channels to carry the video information. Video cameras produce RGB (red, green, blue) directly from the image sensors. RGB is also the usual format used by computers internally for graphics. RGB can also be converted to Y, R-Y, B-Y format, sometimes called YUV format. These three-circuit video standards are referred to as component analog video.

The three-circuit video standards require three crosspoint channels per video channel to handle the switching function. In a fashion similar to the two-circuit video formats, the inputs and outputs are assigned in groups of three and the appropriate logic programming is performed to route the video signals.

Creating Larger Crosspoint Arrays

The AD8116 is a high density building block for crosspoint arrays over 256 × 256. Various features such as output disable, chip enable, serial data out and multiple pinouts for logic signals are very useful for the creation of these larger arrays.

The first consideration in constructing a larger crosspoint is to determine the minimum number of devices that are required. The 16 × 16 architecture of the AD8116 contains 256 "points," which is a factor of four greater than an 8 × 8 crosspoint and a factor of 64 greater than a 4 × 1 crosspoint. The PC board area and power consumption savings are readily apparent when compared to using these smaller devices.

For a nonblocking crosspoint, the number of points required is the product of the number of inputs multiplied by the number of outputs. Nonblocking requires that the programming of a given input to one or more outputs does not restrict the availability of that input to be a source for any other outputs.

Thus a 32 × 32 crosspoint will require 1024 points. This number is then divided by 256, or the number of points in one AD8116 device, to yield four in this case. This says that the minimum number of 16 × 16 devices required for a fully programmable 32 × 32 crosspoint is four.

Some nonblocking crosspoint architectures will require more than this minimum as calculated above. Also, there are blocking architectures that can be constructed with fewer devices than this minimum. These systems have connectivity available on a statistical basis that is determined when designing the overall system.

The basic concept in constructing larger crosspoint arrays is to connect inputs in parallel in a horizontal direction and to "wire-OR" the outputs together in the vertical direction. The meaning of horizontal and vertical can best be understood by looking at a diagram. Figure 6 illustrates this concept for a 32 × 32 crosspoint array. A 48 × 48 crosspoint is illustrated in Figure 7.

The 32 × 32 crosspoint requires each input driver drive two inputs in parallel and each output be wire-ORed with one other output. The 48 × 48 crosspoint requires driving three inputs in parallel and having the outputs wire-ORed in groups of three. It is required of the system programming that only one output of a wired-OR node be active at a time.

It is not essential that crosspoint architectures be square. For example, a 64 × 16 crosspoint array can be constructed with four AD8116s by driving each input with a separate signal and wire-ORing together the corresponding outputs of each device. It can be seen, however, that by going to larger arrays the number of disabled outputs an active output has to drive starts to increase.

At some point, the number of outputs that are wire-ORed becomes too great to maintain system performance. This will vary according to which system specifications are most important. For example, a 128 × 16 crosspoint can be created with eight AD8116s. This design will have 128 separate inputs and have the corresponding outputs of each device wire-ORed together in groups of eight.

Using additional crosspoint devices in the design can lower the number of outputs that have to be wire-ORed together. Figure 8 shows a block diagram of a system using ten AD8116s to create a nonblocking 128 × 16 crosspoint that restricts the wire-ORing at the output to only four outputs. This will prevent an enabled output from having to drive a large number of disabled devices. Additionally, by using the lower eight outputs from each of the two Rank 2 AD8116s, a blocking 128 × 32 crosspoint array can be realized.

There are, however, some drawbacks to this technique. The offset voltages of the various cascaded devices will accumulate and the bandwidth limitations of the devices will compound. In addition, the extra devices will consume more current and take up more board space. Once again, the overall system design specifications will determine how to make the various trade-offs.

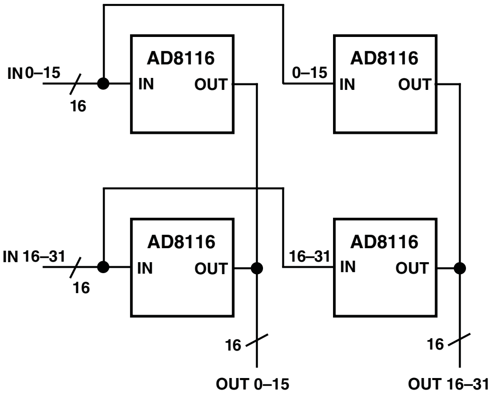


Figure 6. 32 × 32 Crosspoint Array Using Four AD8116s

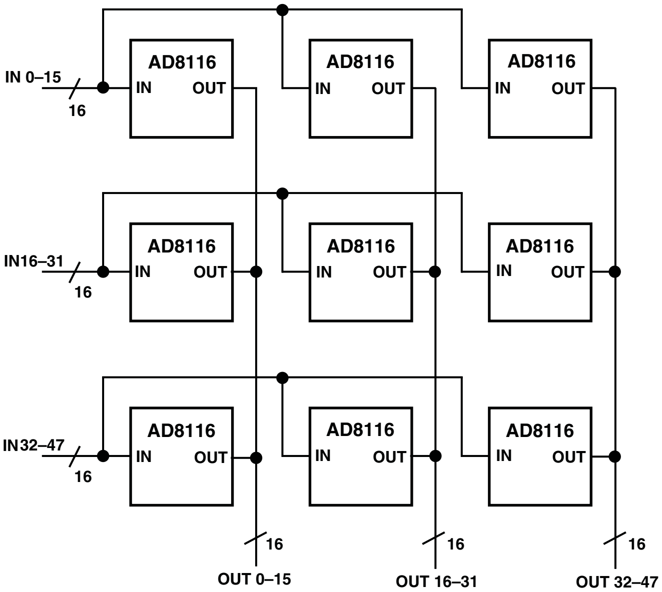


Figure 7. 48 × 48 Crosspoint Array Using Nine AD8116s

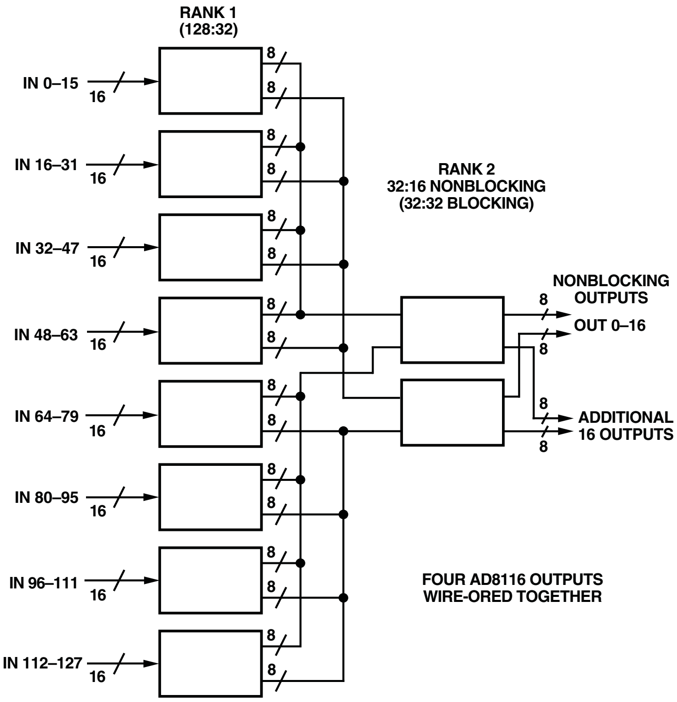


Figure 8. Nonblocking 128 × 16 Array (128 × 32 Blocking)

Logic Operation

There are two basic options for controlling the logic in multicrosspoint arrays. One is to serially connect the data paths (DATA OUT to DATA IN) of all the devices and tie all the CLK and $\overline{\text{UPDATE}}$ signals in parallel. $\overline{\text{CE}}$ can be tied low for all the devices. A long serial sequence with the desired programming data consisting of 80 bits times the number of AD8116 devices can then be shifted through all the parallel devices by using the DATA IN of the first device and the CLK. When finished clocking in the data, $\overline{\text{UPDATE}}$ can be pulled low to program all the device crosspoint matrices.

This technique has an advantage in that a separate $\overline{\text{CE}}$ signal is not required for each chip, but has a disadvantage in that several chips' data cannot be shifted in parallel. In addition, if another device is added into the system between already existing devices, the programming sequence will have to be lengthened at some midpoint to allow for programming of the added device.

The second programming method is to connect all the CLK and the DATA IN pins in parallel and use the $\overline{\text{CE}}$ pins in sequence to program each device. If a byte or 16-bit word of data is available for providing the programming data, then multiple AD8116s can be programmed in parallel with just 80 clock cycles. This method can be used to speed up the programming of large arrays. Of course, in a practical system, various combinations of these basic methods can be used.

Power-On Reset

Most systems will want all the AD8116s to be in the reset state (all outputs disabled) when power is applied to the system. This ensures that two outputs that are wire-ORed together will not fight each other at power up.

The power-on reset function can be implemented by adding a 0.1 μF capacitor from the $\overline{\text{RESET}}$ pin to ground. This will hold this signal low after the power is applied to reset the device. An on-chip 20 kΩ resistor from $\overline{\text{RESET}}$ to DVCC will charge the capacitor to the logical high state. If several AD8116s are used, the pull-up resistors will be in parallel, so a larger value capacitance should be used.

If the system requires the ability to be reset while power is still applied, the $\overline{\text{RESET}}$ driver will have to be able to charge and discharge this capacitance in the required time. With too many devices in parallel, this might become more difficult; if this occurs, the reset circuits should be broken up into smaller subsets with each controlled by a separate driver.

CROSSTALK

Many systems, such as broadcast video, that handle numerous analog signal channels have strict requirements for keeping the various signals from influencing any of the others in the system. Crosstalk is the term used to describe the coupling of the signals of other nearby channels to a given channel.

When there are many signals in close proximity in a system, as will undoubtedly be the case in a system that uses the AD8116, the crosstalk issues can be quite complex. A good understanding of the nature of crosstalk and some definition of terms is required in order to specify a system that uses one or more AD8116s.

Types of Crosstalk

Crosstalk can be propagated by means of any of three methods. These fall into the categories of electric field, magnetic field and sharing of common impedances. This section will explain these effects.

Every conductor can be both a radiator of electric fields and a receiver of electric fields. The electric field crosstalk mechanism occurs when the electric field created by the transmitter propagates across a stray capacitance and couples with the receiver and induces a voltage. This voltage is an unwanted crosstalk signal in any channel that receives it.

Currents flowing in conductors create magnetic fields that circulate around the currents. These magnetic fields will then generate voltages in any other conductors whose paths they link. The undesired induced voltages in these other channels are crosstalk signals. The channels that crosstalk can be said to have a mutual inductance that couples signals from one channel to another.

The power supplies, grounds and other signal return paths of a multichannel system are generally shared by the various channels. When a current from one channel flows in one of these paths, a voltage that is developed across the impedance becomes an input crosstalk signal for other channels that share the common impedance.

All these sources of crosstalk are vector quantities, so the magnitudes cannot be simply added together to obtain the total crosstalk. In fact, there are conditions where driving additional circuits in parallel in a given configuration can actually reduce the crosstalk.

Areas of Crosstalk

For a practical AD8116 circuit, it is required that it be mounted to some sort of circuit board in order to connect it to power supplies and measurement equipment. Great care has been taken to create a characterization board that adds minimum crosstalk to the intrinsic device. This, however, raises the issue that a system's crosstalk is a combination of the intrinsic crosstalk of the devices and the circuit board to which they are mounted. It is important to try to separate these two areas of crosstalk when attempting to minimize its effect.

In addition, crosstalk can occur among the input circuits to a crosspoint and among the output circuits. Techniques will be discussed for diagnosing which part of a system is contributing to crosstalk.

Measuring Crosstalk

Crosstalk is measured by applying a signal to one or more channels and measuring the relative strength of that signal on a desired selected channel. The measurement is usually expressed as dB down from the magnitude of the test signal. The crosstalk is expressed by:

$$|XT| = 20\log_{10}(Asel(s)/Atest(s))$$

where $s = j\omega$ is the Laplace transform variable, $Asel(s)$ is the amplitude of the crosstalk-induced signal in the selected channel and $Atest(s)$ is the amplitude of the test signal. It can be seen that crosstalk is a function of frequency, but not a function of the magnitude of the test signal. In addition, the crosstalk signal will have a phase relative to the test signal associated with it.

A network analyzer is most commonly used to measure crosstalk over a frequency range of interest. It can provide both magnitude and phase information about the crosstalk signal.

As a crosspoint system or device grows larger, the number of theoretical crosstalk combinations and permutations can become extremely large. For example, in the case of the 16 × 16 matrix of the AD8116, we can examine the number of crosstalk terms that can be considered for a single channel, say IN00 input. IN00 is programmed to connect to one of the AD8116 outputs where the measurement can be made.

First, we can measure the crosstalk terms associated with driving a test signal into each of the other 15 inputs one at a time. We can then measure the crosstalk terms associated with driving a parallel test signal into all 15 other inputs taken two at a time in all possible combinations; and then three at a time, etc., until, finally, there is only one way to drive a test signal into all 15 other inputs.

Each of these cases is legitimately different from the others and might yield a unique value depending on the resolution of the measurement system, but it is hardly practical to measure all these terms and then to specify them. In addition, this describes the crosstalk matrix for just one input channel. A similar crosstalk matrix can be proposed for every other input. In addition, if the possible combinations and permutations for connecting inputs to the other (not used for measurement) outputs are taken into consideration, the numbers rather quickly grow to astronomical proportions. If a larger crosspoint array of multiple AD8116s is constructed, the numbers grow larger still.

Obviously, some subset of all these cases must be selected to be used as a guide for a practical measure of crosstalk. One common term is “all hostile” crosstalk. This term means that all other system channels are driven in parallel, and the crosstalk to the selected channel is measured. In general, this will yield the worst crosstalk number, but this is not always the case.

Other useful crosstalk measurements are those created by one nearest neighbor or by the two nearest neighbors on either side. These crosstalk measurements will generally be higher than those of more distant channels, so they can serve as a worst case measure for any other one-channel or two-channel crosstalk measurements.

Input and Output Crosstalk

The flexible programming capability of the AD8116 can be used to diagnose whether crosstalk is occurring more on the input side or the output side. Some examples are illustrative. A given input channel (IN07 in the middle for this example) can be programmed to drive OUT07. The input to IN07 is just terminated to ground and no signal is applied.

All the other inputs are driven in parallel with the same test signal (practically provided by a distribution amplifier), but all other outputs except OUT07 are disabled. Since grounded IN07 is programmed to drive OUT07, there should be no signal present. Any signal that is present can be attributed to the other 15 hostile input signals, because no other outputs are driven. Thus, this method measures the all-hostile input contribution to crosstalk into IN07. Of course, the method can be used for other input channels and combinations of hostile inputs.

For output crosstalk measurement, a single input channel is driven (IN00 for example) and all outputs other than a given output (IN07 in the middle) are programmed to connect to IN00. OUT07 is programmed to connect to IN15 which is terminated to ground. Thus OUT07 should not have a signal present since it is listening to a quiet input. Any signal measured at the OUT07 can be attributed to the output crosstalk of the other 15 hostile outputs. Again, this method can be modified to measure other channels and other crosspoint matrix combinations.

Effect of Impedances on Crosstalk

The input side crosstalk can be influenced by the output impedance of the sources that drive the inputs. The lower the impedance of the drive source, the lower the magnitude of the crosstalk. The dominant crosstalk mechanism on the input side is capacitive coupling. The high impedance inputs do not have significant current flow to create magnetically induced crosstalk.

From a circuit standpoint, the input crosstalk mechanism looks like a capacitor coupling to a resistive load. For low frequencies the magnitude of the crosstalk will be given by:

$$|XT| = 20\log_{10}[(R_S C_M) \times s]$$

where R_S is the source resistance, C_M is the mutual capacitance between the test signal circuit and the selected circuit, and s is the Laplace transform variable.

From the equation it can be observed that this crosstalk mechanism has a high pass nature; it can be also minimized by reducing the coupling capacitance of the input circuits and lowering the output impedance of the drivers. If the input is driven from a 75 Ω terminated cable, the input crosstalk can be reduced by buffering this signal with a low output impedance buffer.

On the output side, the crosstalk can be reduced by driving a lighter load. Although the AD8116 is specified with excellent differential gain and phase when driving a standard 150 Ω video load, the crosstalk will be higher than the minimum due to the high output currents. These currents will induce crosstalk via the mutual inductance of the output pins and bond wires of the AD8116.

From a circuit standpoint, this output crosstalk mechanism looks like a transformer with a mutual inductance between the windings that drives a load resistor. For low frequencies, the magnitude of the crosstalk is given by:

$$|XT| = 20 \log_{10} (Mxy \times s/R_L)$$

where Mxy is the mutual inductance of output x to output y and R_L is the load resistance on the measured output. This crosstalk mechanism can be minimized by keeping the mutual inductance low and increasing R_L. The mutual inductance can be kept low by increasing the spacing of the conductors and minimizing their parallel length.

One way to increase the load resistance is to buffer the outputs with a high input impedance buffer as shown in Figure 9. The AD8079AR is a dual buffer that can be strapped for a gain of +2 (B grade = +2.2). This offsets the halving of the signal when driving a standard back-terminated video cable.

The input of the buffer requires a path for bias current. This can be provided by a 500 Ω to 5 kΩ resistor to ground. This resistor also serves the purpose of biasing the outputs of the crosspoints at zero volts when all the outputs are disabled.

In addition, the load resistor actually lowers the crosstalk compared to the conditions of the AD8116 outputs driving a high impedance (greater than 10 kΩ) or driving a video load (150 Ω). This is because the electric field crosstalk that dominates in the high impedance case has a phase of –90 degrees, while the magnetic field crosstalk that dominates in the video load case has a phase of +90 degrees. With a 500 Ω to 5 kΩ load, the contributions from each of these is roughly equal, and there is some cancellation of crosstalk due to the phase differences.

PCB Layout

Extreme care must be exercised to minimize additional crosstalk generated by the system circuit board(s). The areas that must be carefully detailed are grounding, shielding, signal routing and supply bypassing.

The packaging of the AD8116 is designed to help keep the crosstalk to a minimum. Each input is separated from each other's input by an analog ground pin. All of these AGNDs should be directly connected to the ground plane of the circuit board. These ground pins provide shielding, low impedance return paths and physical separation for the inputs. All of these help to reduce crosstalk.

Each output is separated from its two neighboring outputs by analog supply pins of either polarity. Each of these analog supply pins provides power to the output stages of only the two adjacent outputs. These supply pins provide shielding, physical separation and low impedance supply for the channel outputs. Individual bypassing of each of these supply pins with a 0.01 µF chip capacitor directly to the ground plane minimizes high frequency output crosstalk via the mechanism of sharing common impedances.

Each output also has an on-chip compensation capacitor that is individually tied to a package pin via the signals called AGND00 through AGND15. This technique reduces crosstalk by preventing the currents that flow in these paths from sharing a common impedance on the IC and in the package pins. These AGNDxx signals should all be connected directly to the ground plane.

The input and output signals minimize crosstalk if they are located between ground planes on layers above and below, and separated by ground in between. Vias should be located as close to the IC as possible to carry the inputs and outputs to the inner layer. The only place the input and output signals surface is at the input termination resistors and the output series back termination resistors. These signals should also be separated, to the extent possible, as soon as they emerge from the IC package.

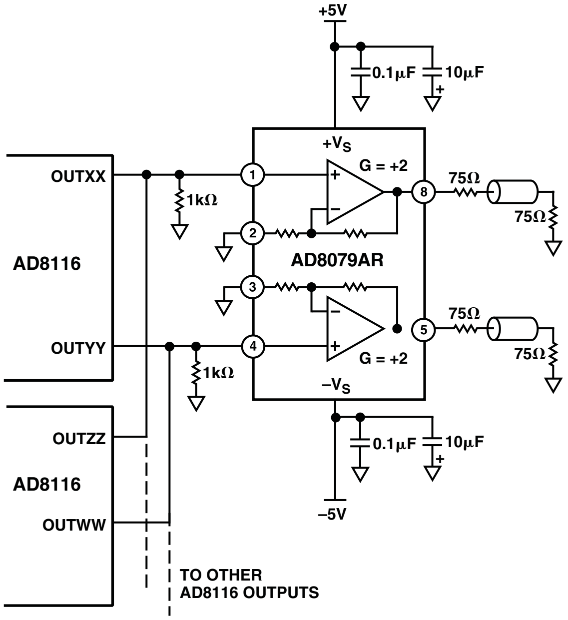


Figure 9. Buffering Wired OR Outputs with the AD8079

OUTLINE DIMENSIONS

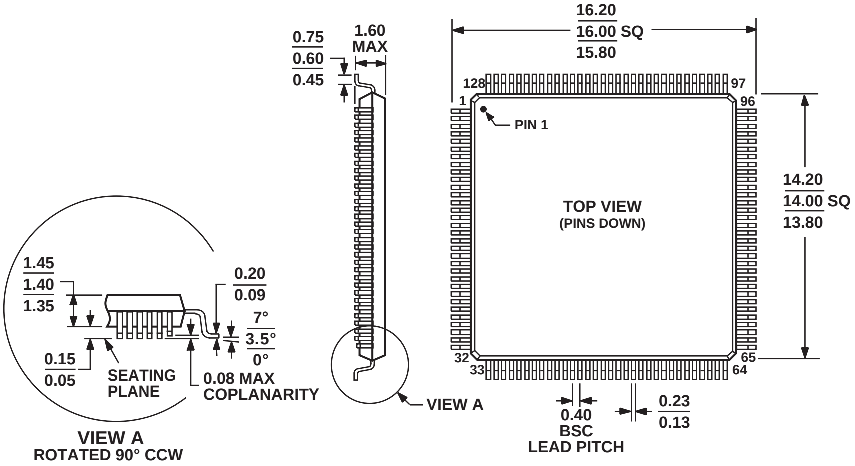


Figure 10. 128-Lead Low Profile Quad Flat Package [LQFP]
(ST-128-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD8116JSTZ	0°C to 70°C	128-Lead Low Profile Quad Flat Package [LQFP]	ST-128-1

[1] Z = RoHS-Compliant Part.

REVISION HISTORY

5/16—Rev. B to Rev. C

Changes to General Description 1
Changes to Off Isolation, Input-Output Parameter...................... 2
Changes to Areas of Crosstalk Section.. 13
Deleted Evaluation Board Section 15
Deleted Figure 10; Renumbered Sequentially 16
Moved Outline Dimensions, Ordering Guide, and Revision History 16
Updated Outline Dimensions... 16
Changes to Ordering Guide.. 16
Deleted Figure 11 17
Deleted Figure 12 18
Deleted Figure 13 19
Deleted Figure 14 20
Deleted Figure 15 21
Deleted Figure 16 22
Deleted Figure 17 23
Deleted Controlling the Evaluation Board from a PC Section, Figure 18, and Overshoot on PC Printer Ports' Data Lines Section 24
Deleted Figure 19 25

6/01—Rev. A to Rev. B

Correction to Pin Number in Pin Function Description 6

C01071a-0-5/16(C)