High Accuracy Instrumentation Amplifier

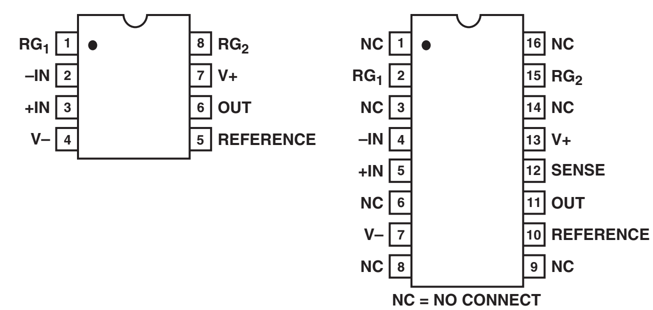
AMP02

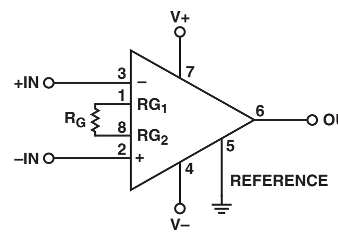
FEATURES
Low Offset Voltage: 100 μV max
Low Drift: 2 μV/°C max
Wide Gain Range: 1 to 10,000
High Common-Mode Rejection: 115 dB min
High Bandwidth (G = 1000): 200 kHz typ
Gain Equation Accuracy: 0.5% max
Single Resistor Gain Set
Input Overvoltage Protection
Low Cost
Available in Die Form

APPLICATIONS
Differential Amplifier
Strain Gage Amplifier
Thermocouple Amplifier
RTD Amplifier
Programmable Gain Instrumentation Amplifier
Medical Instrumentation
Data Acquisition Systems

FUNCTIONAL BLOCK DIAGRAM

8-Lead PDIP and CERDIP **16-Lead SOIC**





$$G = \frac{V_{OUT}}{(+IN) - (-IN)} = \left(\frac{50k\Omega}{R_G}\right) + 1$$

FOR SOL CONNECT SENSE TO OUTPUT

Figure 1. Basic Circuit Connections

GENERAL DESCRIPTION

The AMP02 is the first precision instrumentation amplifier available in an 8-lead package. Gain of the AMP02 is set by a single external resistor and can range from 1 to 10,000. No gain set resistor is required for unity gain. The AMP02 includes an input protection network that allows the inputs to be taken 60 V beyond either supply rail without damaging the device.

Laser trimming reduces the input offset voltage to under 100 μV. Output offset voltage is below 4 mV, and gain accuracy is better than 0.5% for a gain of 1000. ADI's proprietary thin-film resistor process keeps the gain temperature coefficient under 50 ppm/°C.

Due to the AMP02's design, its bandwidth remains very high over a wide range of gain. Slew rate is over 4 V/μs, making the AMP02 ideal for fast data acquisition systems.

A reference pin is provided to allow the output to be referenced to an external dc level. This pin may be used for offset correction or level shifting as required. In the 8-lead package, sense is internally connected to the output.

For an instrumentation amplifier with the highest precision, consult the AMP01 data sheet.

REV. E

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AMP02* Product Page Quick Links

Last Content Update: 11/01/2016

Comparable Parts

View a parametric search of comparable parts

Documentation

Application Notes

- AN-244: A User's Guide to I.C. Instrumentation Amplifiers
- AN-245: Instrumentation Amplifiers Solve Unusual Design Problems
- AN-282: Fundamentals of Sampled Data Systems
- AN-589: Ways to Optimize the Performance of a Difference Amplifier
- AN-671: Reducing RFI Rectification Errors in In-Amp Circuits

Data Sheet

- AMP02: High Accuracy 8-Pin Instrumentation Amplifier Data Sheet

Technical Books

- A Designer's Guide to Instrumentation Amplifiers, 3rd Edition, 2006

Tools and Simulations

- In-Amp Error Calculator
- AMP02 SPICE Macro-Model

Reference Materials

Technical Articles

- Auto-Zero Amplifiers
- High-performance Adder Uses Instrumentation Amplifiers
- Input Filter Prevents Instrumentation-amp RF-Rectification Errors
- The AD8221 - Setting a New Industry Standard for Instrumentation Amplifiers

Design Resources

- AMP02 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

Discussions

View all AMP02 EngineerZone Discussions

Sample and Buy

Visit the product page to see pricing options

Technical Support

Submit a technical question or find your regional support number

AMP02–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	AMP02E Min	AMP02E Typ	AMP02E Max	AMP02F Min	AMP02F Typ	AMP02F Max	Unit
OFFSET VOLTAGE									
Input Offset Voltage	V_{IOS}	T_A = 25°C		20	100		40	200	µV
		–40°C ≤ T_A ≤ +85°C		50	200		100	350	µV
Input Offset Voltage Drift	TCV_{IOS}	–40°C ≤ T_A ≤ +85°C		0.5	2		1	4	µV/°C
Output Offset Voltage	V_{OOS}	T_A = 25°C		1	4		2	8	mV
		–40°C ≤ T_A ≤ +85°C		4	10		9	20	mV
Output Offset Voltage Drift	TCV_{OOS}	–40°C ≤ T_A ≤ +85°C		50	100		100	200	µV/°C
Power Supply Rejection	PSR	V_S = ±4.8 V to ±18 V							
		G = 100, 1000	115	125		110	115		dB
		G = 10	100	110		95	100		dB
		G = 1	80	90		75	80		dB
		V_S = ±4.8 V to ±18 V							
		–40°C ≤ T_A ≤ +85°C							
		G = 1000, 100	110	120		105	110		dB
		G = 10	95	110		90	95		dB
		G = 1	75	90		70	75		dB
INPUT CURRENT									
Input Bias Current	I_B	T_A = 25°C		2	10		4	20	nA
Input Bias Current Drift	TCI_B	–40°C ≤ T_A ≤ +85°C		150			250		pA/°C
Input Offset Current	I_{OS}	T_A = 25°C		1.2	5		2	10	nA
Input Offset Current Drift	TCI_{OS}	–40°C ≤ T_A ≤ +85°C		9			15		pA/°C
INPUT									
Input Resistance	R_{IN}	Differential, G ≤ 1000		10			10		GΩ
		Common Mode, G = 1000		16.5			16.5		GΩ
Input Voltage Range	IVR	T_A = 25°C[1]	±11			±11			V
Common-Mode Rejection	CMR	V_{CM} = ±11 V							
		G = 1000, 100	115	120		110	115		dB
		G = 10	100	115		95	110		dB
		G = 1	80	95		75	90		dB
		V_{CM} = ±11 V							
		–40°C ≤ T_A ≤ +85°C							
		G = 100, 1000	110	120		105	115		dB
		G = 10	95	110		90	105		dB
		G = 1	75	90		70	85		dB
GAIN									
Gain Equation Accuracy	$G = \frac{50\ k\Omega}{R_G} + 1$	G = 1000			0.50			0.70	%
		G = 100			0.30			0.50	%
		G = 10			0.25			0.40	%
		G = 1			0.02			0.05	%
Gain Range	G		1		10k	1		10k	V/V
Nonlinearity		G = 1 to 1000		0.006			0.006		%
Temperature Coefficient	G_{TC}	1 ≤ G ≤ 1000[2, 3]		20	50		20	50	ppm/°C
OUTPUT RATING									
Output Voltage Swing	V_{OUT}	T_A = 25°C, R_L = 1 kΩ	±12	±13		±12	±13		V
		R_L = 1 kΩ, –40°C ≤ T_A ≤ +85°C	±11	±12		±11	±12		V
Positive Current Limit		Output-to-Ground Short		22			22		mA
Negative Current Limit		Output-to-Ground Short		32			32		mA
NOISE									
Voltage Density, RTI	e_n	f_O = 1 kHz							
		G = 1000		9			9		nV/√Hz
		G = 100		10			10		nV/√Hz
		G = 10		18			18		nV/√Hz
		G = 1		120			120		nV/√Hz
Noise Current Density, RTI	i_n	f_O = 1 kHz, G = 1000		0.4			0.4		pA/√Hz
Input Noise Voltage	e_n p-p	0.1 Hz to 10 Hz							
		G = 1000		0.4			0.4		µV p-p
		G = 100		0.5			0.5		µV p-p
		G = 10		1.2			1.2		µV p-p
DYNAMIC RESPONSE									
Small-Signal Bandwidth	BW	G = 1		1200			1200		kHz
(–3 dB)		G = 10		300			300		kHz
G = 100, 1000				200			200		kHz
Slew Rate	SR	G = 10, R_L = 1 kΩ	4	6		4	6		V/µs
Settling Time	t_S	To 0.01% ±10 V Step							
		G = 1 to 1000		10			10		µs
SENSE INPUT									
Input Resistance	R_{IN}			25			25		kΩ
Voltage Range				±11			±11		V
REFERENCE INPUT									
Input Resistance	R_{IN}			50			50		kΩ
Voltage Range				±11			±11		V
Gain to Output				1			1		V/V

Parameter	Symbol	Conditions	AMP02E Min	AMP02E Typ	AMP02E Max	AMP02F Min	AMP02F Typ	AMP02F Max	Unit
POWER SUPPLY									
Supply Voltage Range	V_S		±4.5		±18	±4.5		±18	V
Supply Current	I_{SY}	$T_A = 25°C$		5	6		5	6	mA
		$-40°C \le T_A \le +85°C$		5	6		5	6	mA

NOTES
[1]Input voltage range guaranteed by common-mode rejection test.
[2]Guaranteed by design.
[3]Gain tempco does not include the effects of external component drift.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1, 2]

Supply Voltage	±18 V
Common-Mode Input Voltage	[(V–) – 60 V] to [(V+) + 60 V]
Differential Input Voltage	[(V–) – 60 V] to [(V+) + 60 V]
Output Short-Circuit Duration	Continuous
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Function Temperature Range	–65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

Package Type	θ_{JA}[3]	θ_{JC}	Unit
8-Lead Plastic DIP (P)	96	37	°C/W
16-Lead SOIC (S)	92	27	°C/W

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[3]θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for P-DIP package; θ_{JA} is specified for device soldered to printed circuit board for SOIC package.

ORDERING GUIDE

Model	V_{IOS} max @ $T_A = 25°C$	V_{OOS} max @ $T_A = 25°C$	Temperature Range	Package Description
AMP02EP	100 µV	4 mV	–40°C to +85°C	8-Lead Plastic DIP
AMP02FP	200 µV	8 mV	–40°C to +85°C	8-Lead Plastic DIP
AMP02AZ/883C	200 µV	10 mV	–55°C to +125°C	8-Lead CERDIP
AMP02FS	200 µV	8 mV	–40°C to +85°C	16-Lead SOIC
AMP02GBC				Die
AMP02FS-REEL	200 µV	8 mV	–40°C to +85°C	16-Lead SOIC

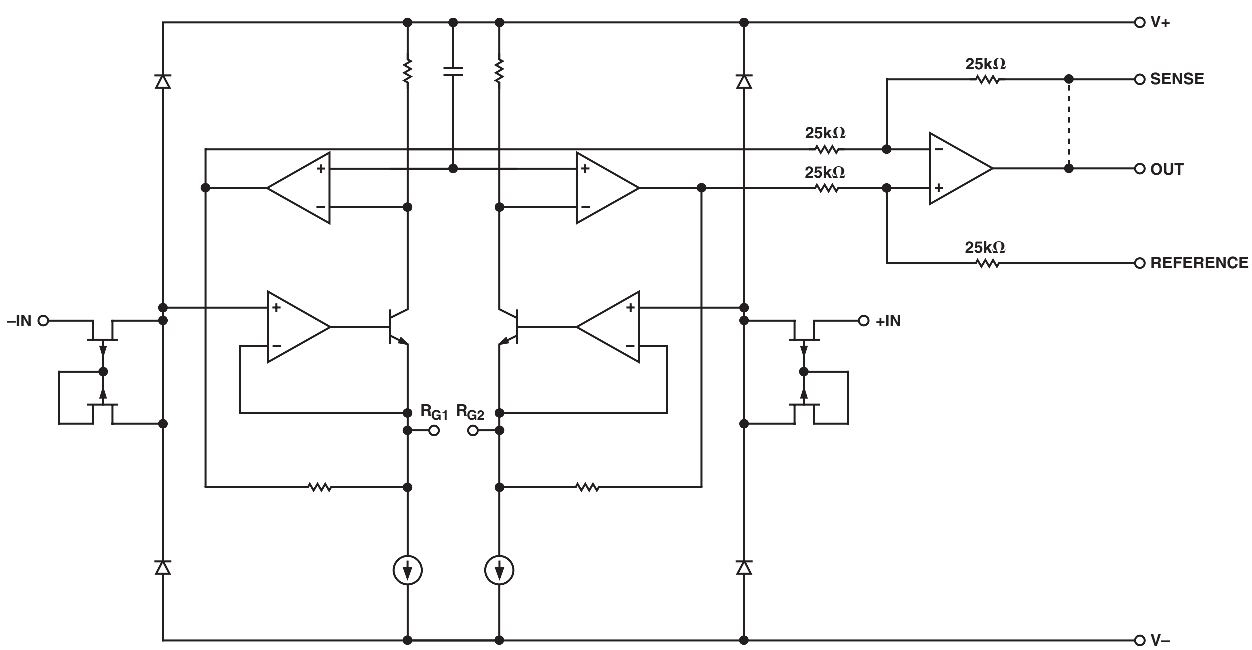
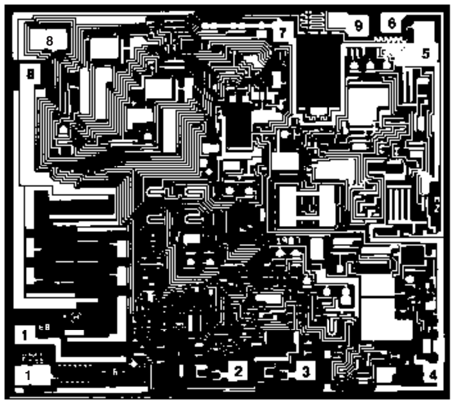


Figure 2. Simplified Schematic



1. RG_1
2. –IN
3. +IN
4. V–
5. REFERENCE
6. OUT
7. V+
8. RG_2
9. SENSE

CONNECT SUBSTRATE TO V–

DIE SIZE 0.103 inch × 0.116 inch, 11,948 sq. mils
(2.62 mm × 2.95 mm, 7.73 sq. mm)
NOTE: PINS 1 and 8 are KELVIN CONNECTED

Die Characteristics

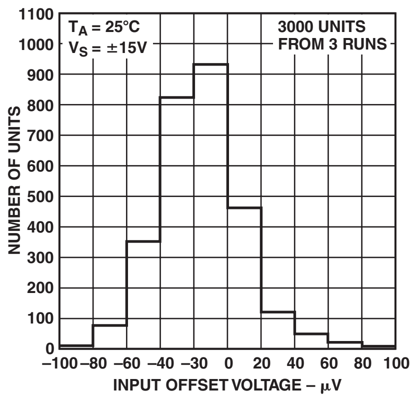
WAFER TEST LIMITS* (@ V_S = ±15 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	AMP02 GBC Limits	Unit
Input Offset Voltage	V_{IOS}		200	μV max
Output Offset Voltage	V_{OOS}		8	mV max
Power Supply Rejection	PSR	V_S = ±4.8 V to ±18 V G = 1000 G = 100 G = 10 G = 1	 110 110 95 75	dB
Input Bias Current	I_B		20	nA max
Input Offset Current	I_{OS}		10	nA max
Input Voltage Range	IVR	Guaranteed by CMR Tests	±11	V min
Common-Mode Rejection	CMR	V_{CM} = ±11 V G = 1000 G = 100 G = 10 G = 1	 110 110 95 75	dB
Gain Equation Accuracy		$G = \frac{50\ k\Omega}{R_G} + 1, G = 1000$	0.7	% max
Output Voltage Swing	V_{OUT}	R_L = 1 kΩ	±12	V min
Supply Current	I_{SY}		6	mA max

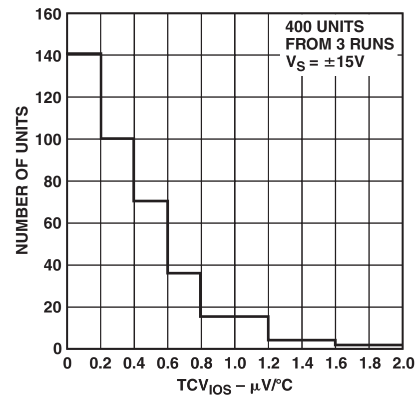
*Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

CAUTION

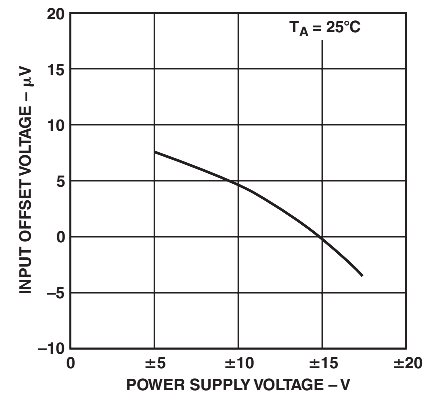
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AMP02 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



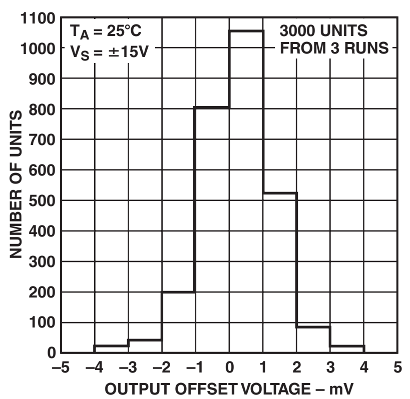
TPC 1. Typical Distribution of Input Offset Voltage



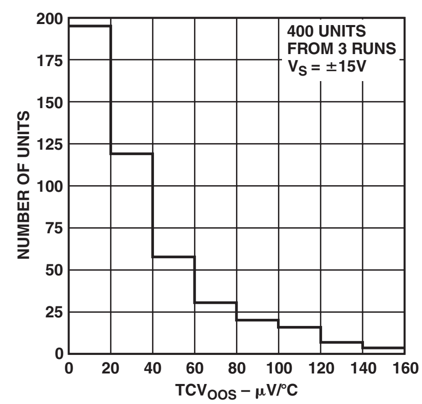
TPC 2. Typical Distribution of TCV_{IOS}



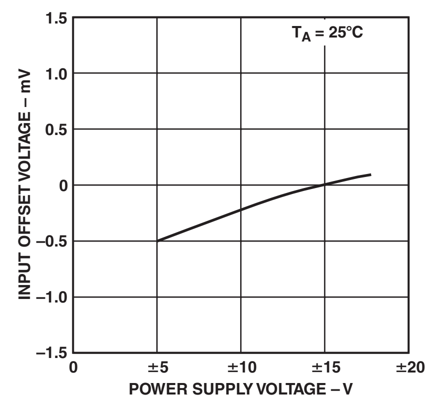
TPC 3. Input Offset Voltage Change vs. Supply Voltage



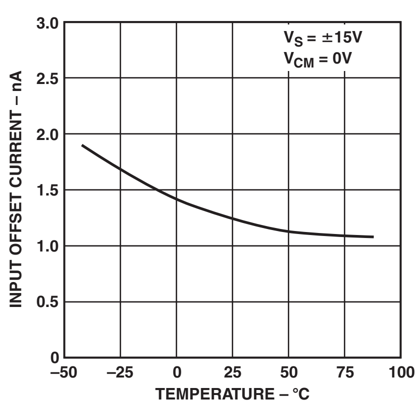
TPC 4. Typical Distribution of Output Offset Voltage



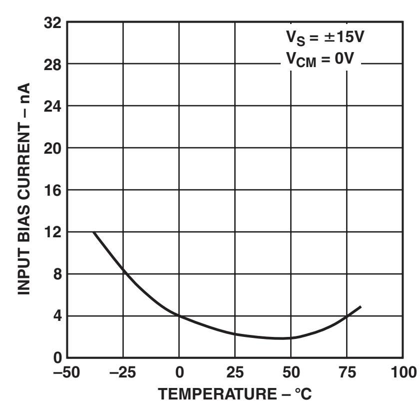
TPC 5. Typical Distribution of TCV_{OOS}



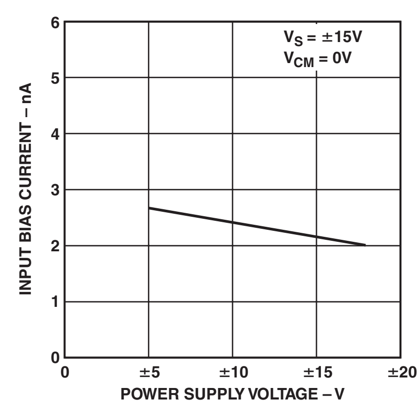
TPC 6. Output Offset Voltage Change vs. Supply Voltage



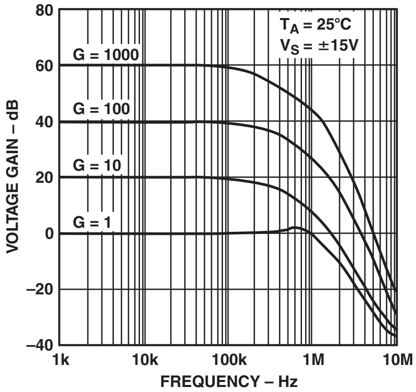
TPC 7. Input Offset Current vs. Temperature



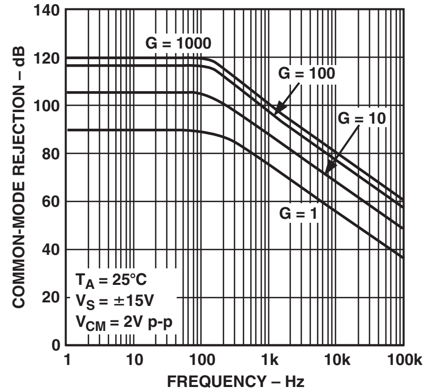
TPC 8. Input Bias Current vs. Temperature



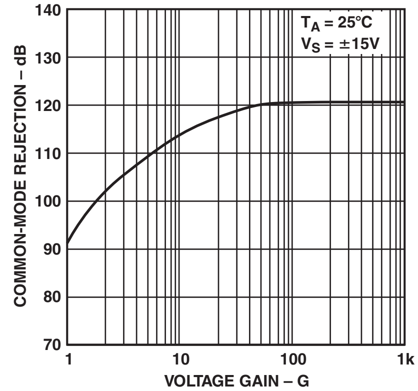
TPC 9. Input Bias Current vs. Supply Voltage



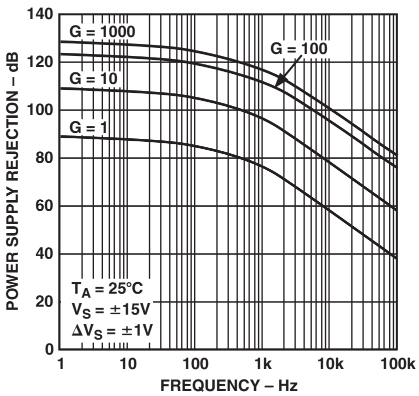
TPC 10. Closed-Loop Voltage Gain vs. Frequency



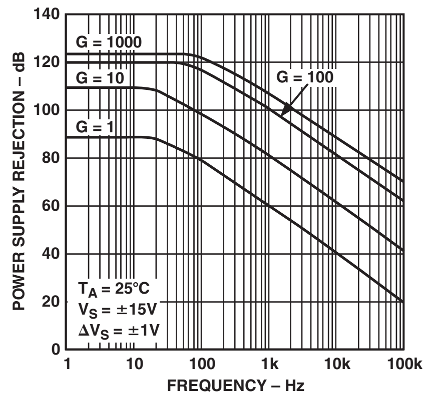
TPC 11. Common-Mode Rejection vs. Frequency



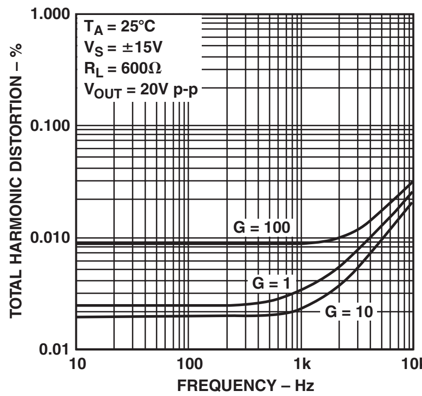
TPC 12. Common-Mode Rejection vs. Voltage Gain



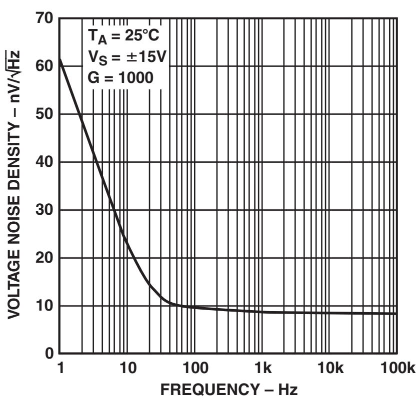
TPC 13. Positive PSR vs. Frequency



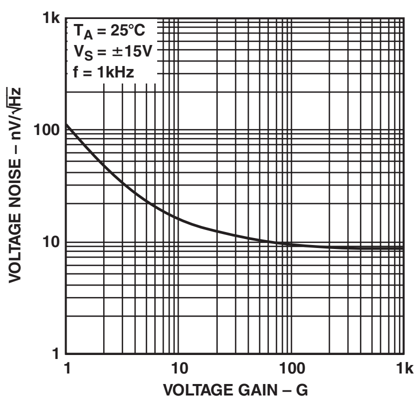
TPC 14. Negative PSR vs. Frequency



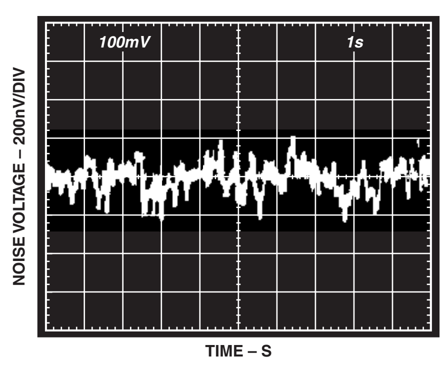
TPC 15. Total Harmonic Distortion vs. Frequency



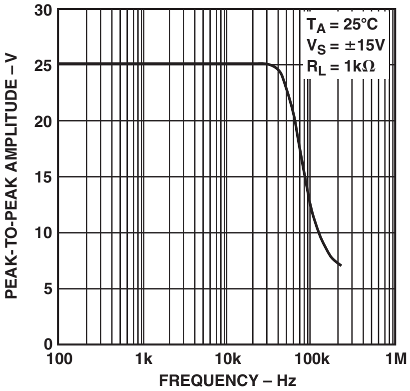
TPC 16. Voltage Noise Density vs. Frequency



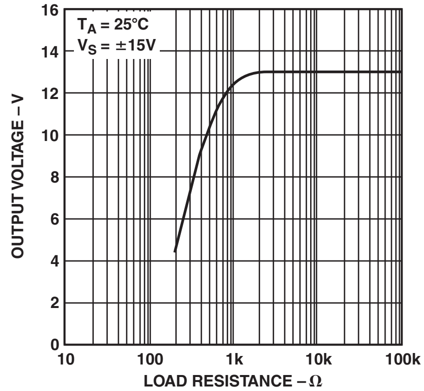
TPC 17. RTI Voltage Noise Density vs. Gain



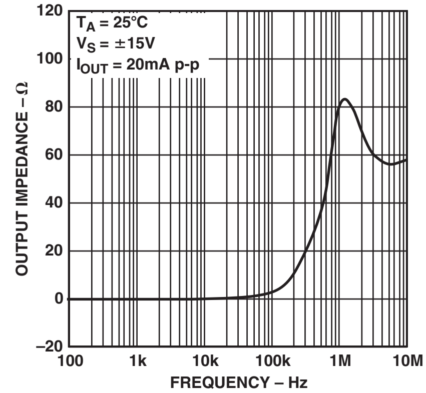
TPC 18. 0.1 Hz to 10 Hz Noise A_V = 1000



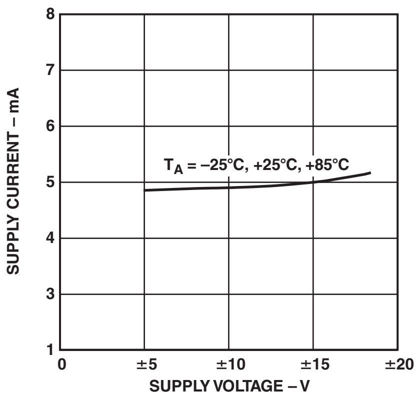
TPC 19. Maximum Output Swing vs. Frequency



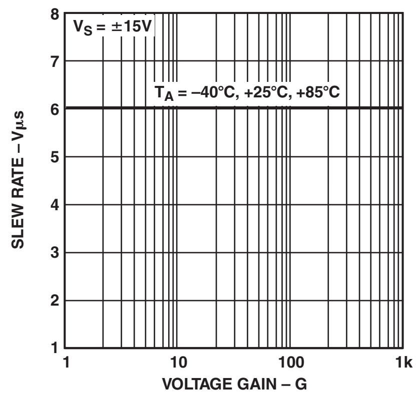
TPC 20. Maximum Output Voltage vs. Load Resistance



TPC 21. Closed Loop Output Impedance vs. Frequency



TPC 22. Supply Current vs. Supply Voltage



TPC 23. Slew Rate vs. Voltage Gain

APPLICATIONS INFORMATION

Input and Output Offset Voltages

Instrumentation amplifiers have independent offset voltages associated with the input and output stages. The input offset component is directly multiplied by the amplifier gain, whereas output offset is independent of gain. Therefore at low gain, output-offset errors dominate while at high gain, input-offset errors dominate. Overall offset voltage, V_{OS}, referred to the output (*RTO*) is calculated as follows:

$$V_{OS}\left(RTO\right)=\left(V_{IOS}\times G\right)+V_{OOS}$$

where V_{IOS} and V_{OOS} are the input and output offset voltage specifications and G is the amplifier gain.

The overall offset voltage drift TCV_{OS}, referred to the output, is a combination of input and output drift specifications. Input offset voltage drift is multiplied by the amplifier gain, G, and summed with the output offset drift:

$$TCV_{OS}\left(RTO\right)=\left(TCV_{IOS}\times G\right)+TCV_{OOS}$$

where TCV_{IOS} is the input offset voltage drift, and TCV_{OOS} is the output offset voltage drift. Frequently, the amplifier drift is referred back to the input (*RTI*), which is then equivalent to an input signal change:

$$TCV_{OS}\left(RTI\right)=TCV_{IOS}+\frac{TCV_{OOS}}{G}$$

For example, the maximum input-referred drift of an AMP02EP set to G = 1000 becomes:

$$TCV_{OS}\left(RTI\right)=2\,\mu V/^{\circ}C+\frac{100\,\mu V/^{\circ}C}{1000}=2.1\,\mu V/^{\circ}C$$

Input Bias and Offset Currents

Input transistor bias currents are additional error sources that can degrade the input signal. Bias currents flowing through the signal source resistance appear as an additional offset voltage. Equal source resistance on both inputs of an IA will minimize offset changes due to bias current variations with signal voltage and temperature; however, the difference between the two bias currents (the input offset current) produces an error. The magnitude of the error is the offset current times the source resistance.

A current path must always be provided between the differential inputs and analog ground to ensure correct amplifier operation. Floating inputs such as thermocouples should be grounded close to the signal source for best common-mode rejection.

Gain

The AMP02 only requires a single external resistor to set the voltage gain. The voltage gain, G, is:

$$G=\frac{50\,k\Omega}{R_G}+1$$

and

$$R_G=\frac{50\,k\Omega}{G-1}$$

The voltage gain can range from 1 to 10,000. A gain set resistor is not required for unity-gain applications. Metal-film or wirewound resistors are recommended for best results.

The total gain accuracy of the AMP02 is determined by the tolerance of the external gain set resistor, R_G, combined with the gain equation accuracy of the AMP02. Total gain drift combines the mismatch of the external gain set resistor drift with that of the internal resistors (20 ppm/°C typ). Maximum gain drift of the AMP02 independent of the external gain set resistor is 50 ppm/°C.

All instrumentation amplifiers require attention to layout so thermocouple effects are minimized. Thermocouples formed between copper and dissimilar metals can easily destroy the TCV_{OS} performance of the AMP02, which is typically 0.5 µV/°C. Resistors themselves can generate thermoelectric EMFs when mounted parallel to a thermal gradient.

The AMP02 uses the triple op amp instrumentation amplifier configuration with the input stage consisting of two transimpedance amplifiers followed by a unity-gain differential amplifier. The input stage and output buffer are laser-trimmed to increase gain accuracy. The AMP02 maintains wide bandwidth at all gains as shown in Figure 3. For voltage gains greater than 10, the bandwidth is over 200 kHz. At unity gain, the bandwidth of the AMP02 exceeds 1 MHz.

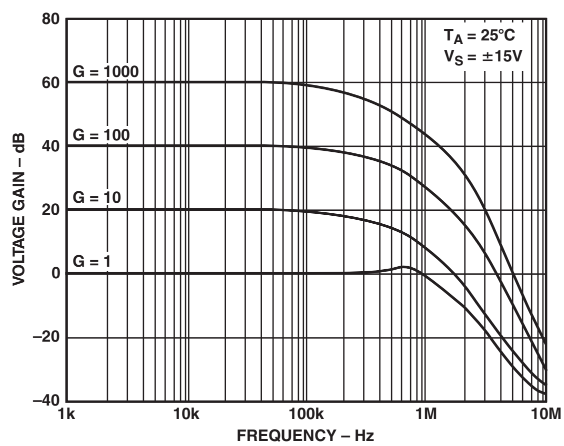


Figure 3. The AMP02 Keeps Its Bandwidth at High Gains

Common-Mode Rejection

Ideally, an instrumentation amplifier responds only to the difference between the two input signals and rejects common-mode voltages and noise. In practice, there is a small change in output voltage when both inputs experience the same common-mode voltage change; the ratio of these voltages is called the common-mode gain. Common-mode rejection (CMR) is the logarithm of the ratio of differential-mode gain to common-mode gain, expressed in dB. Laser trimming is used to achieve the high CMR of the AMP02.

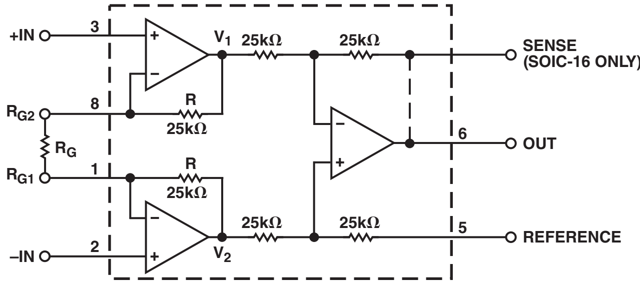


Figure 4. Triple Op Amp Topology

Figure 4 shows the triple op amp configuration of the AMP02. With all instrumentation amplifiers of this type, it is critical not to exceed the dynamic range of the input amplifiers. The amplified differential input signal and the input common-mode voltage must not force the amplifier's output voltage beyond ±12 V (V_S = ±15 V) or nonlinear operation will result.

The input stage amplifier's output voltages at V_1 and V_2 equal:

$$V_1 = -\left(1 + \frac{2R}{R_G}\right)\frac{V_D}{2} + V_{CM}$$

$$= -G\frac{V_D}{2} + V_{CM}$$

$$V_2 = \left(1 + \frac{2R}{R_G}\right)\frac{V_D}{2} + V_{CM}$$

$$= G\frac{V_D}{2} + V_{CM}$$

where:

V_D = Differential input voltage
= (+IN) – (–IN)

V_{CM} = Common-mode input voltage

G = Gain of instrumentation amplifier

If V_1 and V_2 can equal ±12 V maximum, the common-mode input voltage range is:

$$CMVR = \pm\left(12\,V - \frac{GV_D}{2}\right)$$

Grounding

The majority of instruments and data acquisition systems have separate grounds for analog and digital signals. Analog ground may also be divided into two or more grounds that will be tied together at one point, usually at the analog power supply ground. In addition, the digital and analog grounds may be joined—normally at the analog ground pin on the A/D converter. Following this basic practice is essential for good circuit performance.

Mixing grounds causes interactions between digital circuits and the analog signals. Since the ground returns have finite resistance and inductance, hundreds of millivolts can be developed between the system ground and the data acquisition components. Using separate ground returns minimizes the current flow in the sensitive analog return path to the system ground point. Consequently, noisy ground currents from logic gates interact with the analog signals.

Inevitably, two or more circuits will be joined together with their grounds at differential potentials. In these situations, the differential input of an instrumentation amplifier, with its high CMR, can accurately transfer analog information from one circuit to another.

Sense and Reference Terminals

The sense terminal completes the feedback path for the instrumentation amplifier output stage and is internally connected directly to the output. For SOIC devices, connect the sense terminal to the output. The output signal is specified with respect to the reference terminal, which is normally connected to analog ground. The reference may also be used for offset correction level shifting. A reference source resistance will reduce the common-mode rejection by the ratio of 25 kΩ/R_{REF}. If the reference source resistance is 1 Ω, the CMR will be reduced 88 dB (25 kΩ/1 Ω = 88 dB).

Overvoltage Protection

Instrumentation amplifiers invariably sit at the front end of instrumentation systems where there is a high probability of exposure to overloads. Voltage transients, failure of a transducer, or removal of the amplifier power supply while the signal source is connected may destroy or degrade the performance of an unprotected device. A common technique is to place limiting resistors in series with each input, but this adds noise. The AMP02 includes internal protection circuitry that limits the input current to ±4 mA for a 60 V differential overload (see Figure 5) with power off, ±2.5 mA with power on.

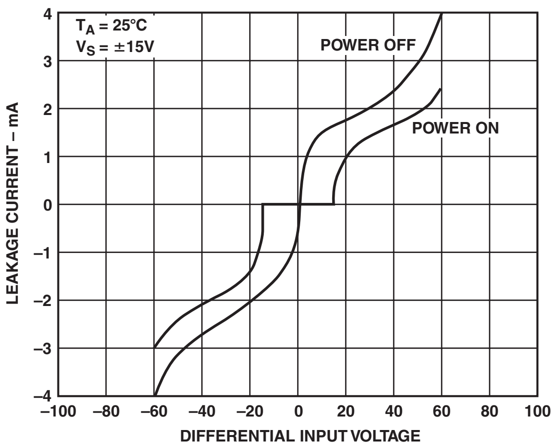


Figure 5. AMP02's Input Protection Circuitry Limits Input Current During Overvoltage Conditions

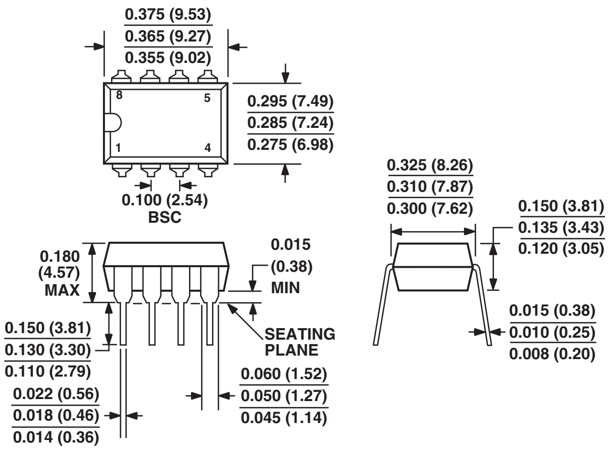
Power Supply Considerations

Achieving the rated performance of precision amplifiers in a practical circuit requires careful attention to external influences. For example, supply noise and changes in the nominal voltage directly affect the input offset voltage. A PSR of 80 dB means that a change of 100 mV on the supply (not an uncommon value) will produce a 10 µV input offset change. Consequently, care should be taken in choosing a power unit that has a low output noise level, good line and load regulation, and good temperature stability. In addition, each power supply should be properly bypassed.

OUTLINE DIMENSIONS

8-Lead Plastic Dual-in-Line Package [PDIP] (N-8)

Dimensions shown in inches and (millimeters)

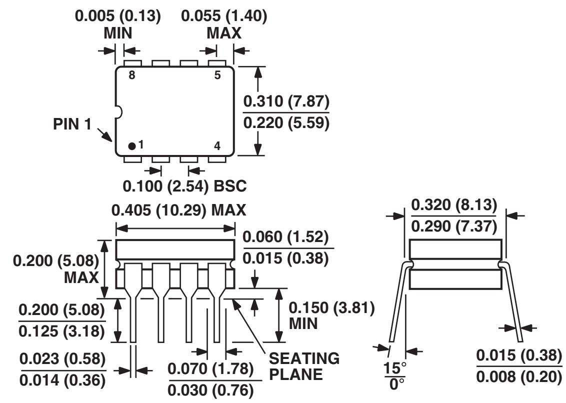


COMPLIANT TO JEDEC STANDARDS MO-095AA

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

8-Lead Ceramic DIP - Glass Hermetic Seal [CERDIP] (Q-8)

Dimensions shown in inches and (millimeters)



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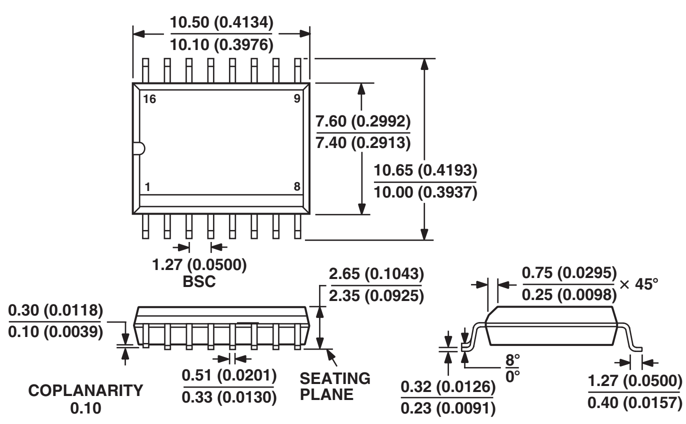
16-Lead Standard Small Outline Package [SOIC] Wide Body (R-16)

Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-013AA

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