Programmable Frequency Sweep and Output Burst Waveform Generator

Data Sheet **AD5930**

FEATURES

- Programmable frequency profile
  - No external components necessary
- Output frequency up to 25 MHz
- Burst and listen capability
- Preprogrammable frequency profile minimizes number of DSP/µcontroller writes
- Sinusoidal/triangular/square wave outputs
- Automatic or single pin control of frequency stepping
- Waveform starts at known phase
  - Increments at 0° phase or phase continuously
- Power-down mode: 20 µA
- Power supply: 2.3 V to 5.5 V
- Automotive temperature range: −40°C to +125°C
- 20-lead pb-free TSSOP

APPLICATIONS

- Frequency sweeping/radar
- Network/impedance measurements
- Incremental frequency stimulus
- Sensory applications
  - Proximity and motion
- BFSK
- Frequency bursting/pulse trains

GENERAL DESCRIPTION

The AD5930[1] is a waveform generator with programmable frequency sweep and output burst capability. Utilizing embedded digital processing that allows enhanced frequency control, the device generates synthesized analog or digital frequency-stepped waveforms. Because frequency profiles are preprogrammed, continuous write cycles are eliminated and thereby free up valuable DSP/µcontroller resources. Waveforms start from a known phase and are incremented phase continuously, which allows phase shifts to be easily determined. Consuming only 8 mA, the AD5930 provides a convenient low power solution to waveform generation.

The AD5930 can be operated in a variety of modes. In continuous output mode, the device outputs the required frequency for a defined length of time and then steps to the next frequency. The length of time the device outputs a particular frequency is either preprogrammed and the device increments the frequency automatically, or, alternatively, is incremented externally via the CTRL pin. In burst mode, the device outputs its frequency for a length of time and then returns to midscale for a further predefined length of time before stepping to the next frequency. When the MSBOUT pin is enabled, a digital output is generated.

(continued on Page 3)

FUNCTIONAL BLOCK DIAGRAM

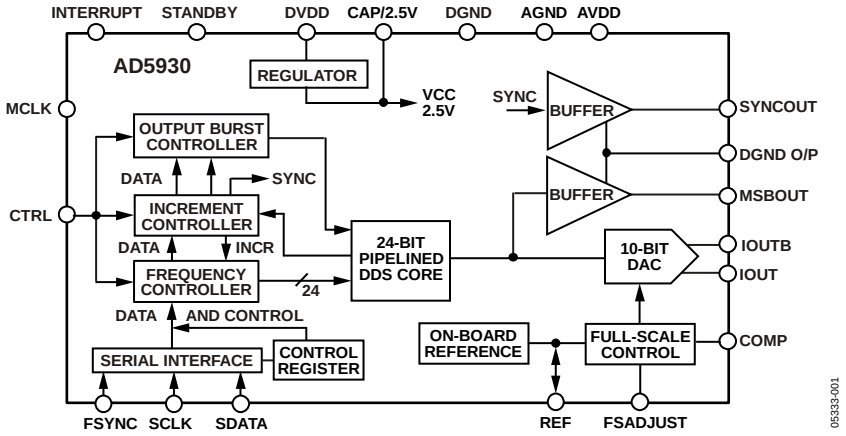

Figure 1.

[1] Protected by US Patent Number 6747583.

Document Feedback

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AD5930* Product Page Quick Links

Last Content Update: 11/01/2016

Comparable Parts

View a parametric search of comparable parts

Evaluation Kits

- AD5930 Evaluation Board

Documentation

Application Notes

- AN-1044: Programming the AD5932 for Frequency Sweep and Single Frequency Outputs
- AN-1248: SPI Interface
- AN-1389: Recommended Rework Procedure for the Lead Frame Chip Scale Package (LFCSP)
- AN-237: Choosing DACs for Direct Digital Synthesis
- AN-280: Mixed Signal Circuit Technologies
- AN-342: Analog Signal-Handling for High Speed and Accuracy
- AN-345: Grounding for Low-and-High-Frequency Circuits
- AN-419: A Discrete, Low Phase Noise, 125 MHz Crystal Oscillator for the AD9850
- AN-423: Amplitude Modulation of the AD9850 Direct Digital Synthesizer
- AN-543: High Quality, All-Digital RF Frequency Modulation Generation with the ADSP-2181 and the AD9850 DDS
- AN-557: An Experimenter's Project:
- AN-587: Synchronizing Multiple AD9850/AD9851 DDS-Based Synthesizers
- AN-605: Synchronizing Multiple AD9852 DDS-Based Synthesizers
- AN-621: Programming the AD9832/AD9835
- AN-632: Provisionary Data Rates Using the AD9951 DDS as an Agile Reference Clock for the ADN2812 Continuous-Rate CDR
- AN-769: Generating Multiple Clock Outputs from the AD9540
- AN-772: A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)
- AN-823: Direct Digital Synthesizers in Clocking Applications Time
- AN-837: DDS-Based Clock Jitter Performance vs. DAC Reconstruction Filter Performance
- AN-843: Measuring a Loudspeaker Impedance Profile Using the AD5933
- AN-847: Measuring a Grounded Impedance Profile Using the AD5933
- AN-851: A WiMax Double Downconversion IF Sampling Receiver Design
- AN-927: Determining if a Spur is Related to the DDS/DAC or to Some Other Source (For Example, Switching Supplies)
- AN-939: Super-Nyquist Operation of the AD9912 Yields a High RF Output Signal

- AN-953: Direct Digital Synthesis (DDS) with a Programmable Modulus

Data Sheet

- AD5930: Programmable Frequency Sweep and Output Burst Waveform Generator Data Sheet

Product Highlight

- Introducing Digital Up/Down Converters: VersaCOMM™ Reconfigurable Digital Converters

User Guides

- UG-822: Evaluation Board for the AD5930 Programmable Frequency Sweep and Output Burst Waveform Generator

Software and Systems Requirements

- AD5930 Evaluation Software

Tools and Simulations

- ADIsimDDS (Direct Digital Synthesis)

Reference Materials

Technical Articles

- 400-MSample DDSs Run On Only +1.8 VDC
- ADI Buys Korean Mobile TV Chip Maker
- Basics of Designing a Digital Radio Receiver (Radio 101)
- Clock Requirements For Data Converters
- DDS Applications
- DDS Circuit Generates Precise PWM Waveforms
- DDS Design
- DDS Device Produces Sawtooth Waveform
- DDS Device Provides Amplitude Modulation
- DDS IC Initiates Synchronized Signals
- DDS IC Plus Frequency-To-Voltage Converter Make Low-Cost DAC
- DDS Simplifies Polar Modulation
- Digital Potentiometers Vary Amplitude In DDS Devices
- Digital Up/Down Converters: VersaCOMM™ White Paper
- Digital Waveform Generator Provides Flexible Frequency Tuning for Sensor Measurement
- Improved DDS Devices Enable Advanced Comm Systems
- Integrated DDS Chip Takes Steps To 2.7 GHz
- Simple Circuit Controls Stepper Motors
- Speedy A/Ds Demand Stable Clocks
- Synchronized Synthesizers Aid Multichannel Systems
- The Year of the Waveform Generator
- Two DDS ICs Implement Amplitude-shift Keying
- Video Portables and Cameras Get HDMI Outputs

Design Resources

- AD5930 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

Discussions

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7/12—Rev. A to Rev. B

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2/12—Rev. 0 to Rev. A

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11/05—Revision 0: Initial Version

GENERAL DESCRIPTION

(continued from Page 1)

To program the device, the user enters the start frequency, the increment step size, the number of increments to be made, and the time interval that the part outputs each frequency. The frequency sweep profile is initiated, started, and executed by toggling the CTRL pin.

A number of different sweep profiles are offered. Frequencies can be stepped in triangular-sweep mode, which continuously sweeps up and down through the frequency range. Alternatively, in saw-sweep mode, the frequency is swept up through the frequency range, but returns to the initial frequency before executing the sweep again. In addition, a single frequency or burst can be generated without any sweep.

The AD5930 is written to via a 3-wire serial interface, which operates at clock rates up to 40 MHz. The device operates with a power supply from 2.3 V to 5.5 V. Note that AV_{DD} and DV_{DD} are independent of each other and can be operated from different voltages. The AD5930 also has a standby function, which allows sections of the device that are not being used to be powered down.

The AD5930 is available in a 20-lead pb-free TSSOP package.

SPECIFICATIONS

AV_{DD} = DV_{DD} = 2.3 V to 5.5 V, AGND = DGND = 0 V, T_A = T_{MIN} to T_{MAX}, R_{SET} = 6.8 kΩ, R_{LOAD} = 200 Ω for IOUT and IOUTB, unless otherwise noted.

Table 1.

	Y Grade[1]				
Parameter	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
SIGNAL DAC SPECIFICATIONS					
Resolution		10		Bits	
Update Rate			50	MSPS	
I_{OUT} Full-Scale[2]		3	4.0	mA	
V_{OUT} Peak-to-Peak		0.56		V	
V_{OUT} Offset		45		mV	From 0 V to the trough of the waveform
$V_{MIDSCALE}$		0.325		V	Voltage at midscale output
Output Compliance			0.8	V	AV_{DD} = 2.3 V, internal reference used[3]
DC Accuracy					
Integral Nonlinearity (INL)		±1.5		LSB	
Differential Nonlinearity (DNL)		±0.75		LSB	
DDS SPECIFICATIONS					
Dynamic Specifications					
Signal-to-Noise Ratio	53	60		dB	f_{MCLK} = 50 MHz, f_{OUT} = f_{MCLK}/4096
Total Harmonic Distortion		−60	−53	dBc	f_{MCLK} = 50 MHz, f_{OUT} = f_{MCLK}/4096
Spurious-Free Dynamic Range (SFDR)					
Wideband (0 to Nyquist)		−62	−52	dBc	f_{MCLK} = 50 MHz, f_{OUT} = f_{MCLK}/50
Narrowband (±200 kHz)		−76	−73	dBc	f_{MCLK} = 50 MHz, f_{OUT} = f_{MCLK}/50
Clock Feedthrough		−50		dBc	Up to 16 MHz out
Wake-Up Time		1.7		ms	From standby
OUTPUT BUFFER					
V_{OUT} Peak-to-Peak	0		DV_{DD}	V	Typically, square wave on MSBOUT and SYNCOUT
Output Rise/Fall Time[2]		12		ns	
VOLTAGE REFERENCE					
Internal Reference	1.15	1.18	1.26	V	
External Reference Range			1.3	V	
REFOUT Input Impedance		1		kΩ	V_{IN} @ REF pin < Internal V_{REF}
		25		kΩ	V_{IN} @ REF pin > Internal V_{REF}
Reference TC[2]		90		ppm/°C	
LOGIC INPUTS					
Input Current		0.1	±1	µA	
V_{INH}, Input High Voltage	1.7			V	DV_{DD} = 2.3 V to 2.7 V
	2.0			V	DV_{DD} = 2.7 V to 3.6 V
	2.8			V	DV_{DD} = 4.5 V to 5.5 V
V_{INL}, Input Low Voltage			0.6	V	DV_{DD} = 2.3 V to 2.7 V
			0.7	V	DV_{DD} = 2.7 V to 3.6 V
			0.8	V	DV_{DD} = 4.5 V to 5.5 V
C_{IN}, Input Capacitance[2]		3		pF	
LOGIC OUTPUTS[2]					
V_{OH}, Output High Voltage	DV_{DD} − 0.4 V			V	I_{SINK} = 1 mA
V_{OL}, Output Low Voltage			0.4	V	I_{SINK} = 1 mA
Floating-State O/P Capacitance		5		pF	

Parameter	Y Grade[1] Min	Typ	Max	Unit	Test Conditions/Comments
POWER REQUIREMENTS					f_{MCLK} = 50 MHz, $f_{OUT} = f_{MCLK}/7$
AV_{DD}/DV_{DD}	2.3		5.5	V	
I_{AA}		3.8	4	mA	
I_{DD}		2.4	2.7	mA	
$I_{AA} + I_{DD}$		6.2	6.7	mA	
Low Power Sleep Mode					Device is reset before putting into standby
		20	85	µA	All outputs powered down, MCLK = 0 V, serial interface active
		140	240	µA	All outputs powered down, MCLK active, serial interface active

[1] Operating temperature range is as follows: Y Version: −40°C to +125°C; typical specifications are at 25°C.
[2] Guaranteed by design.
[3] Minimum R_{SET} = 3.9 kΩ.

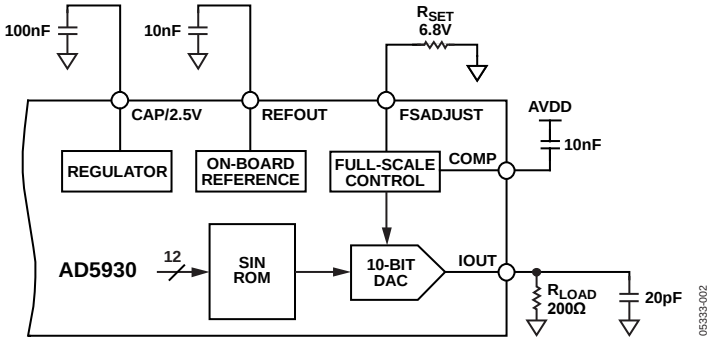

Figure 2. Test Circuit Used to Test the Specifications

TIMING CHARACTERISTICS

All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2.
See Figure 4 to Figure 7. DV_{DD} = 2.3 V to 5.5 V, AGND = DGND = 0 V, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.[1]

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Conditions/Comments
t_1	20	ns min	MCLK period
t_2	8	ns min	MCLK high duration
t_3	8	ns min	MCLK low duration
t_4	25	ns min	SCLK period
t_5	10	ns min	SCLK high time
t_6	10	ns min	SCLK low time
t_7	5	ns min	FSYNC to SCLK falling edge setup time
t_8	10	ns min	FSYNC to SCLK hold time
t_9	5	ns min	Data setup time
t_{10}	3	ns min	Data hold time
t_{11}	2 x t_1	ns min	Minimum CTRL pulse width
t_{12}	0	ns min	CTRL rising edge to MCLK falling edge setup time
t_{13}	10 x t_1	ns typ	CTRL rising edge to IOUT/IOUTB delay (initial pulse, includes initialization)
	8 x t_1	ns typ	CTRL rising edge to IOUT/IOUTB delay (initial pulse, includes initialization)
t_{14}	2 x t_1	ns typ	Frequency change to SYNC output, saw sweep, each frequency increment
t_{15}	2 x t_1	ns typ	Frequency change to SYNC output, saw sweep, end of sweep
t_{16}	2 x t_1	ns typ	Frequency change to SYNC output, triangle sweep, end of sweep
t_{17}	20	ns max	MCLK falling edge after 16th clock edge to MSB out

[1] Guaranteed by design, not production tested.

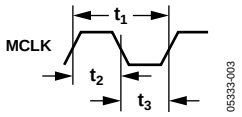

Figure 3. Master Clock

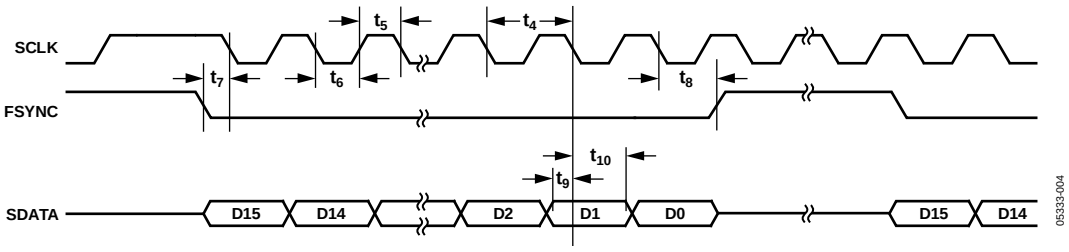

Figure 4. Serial Timing

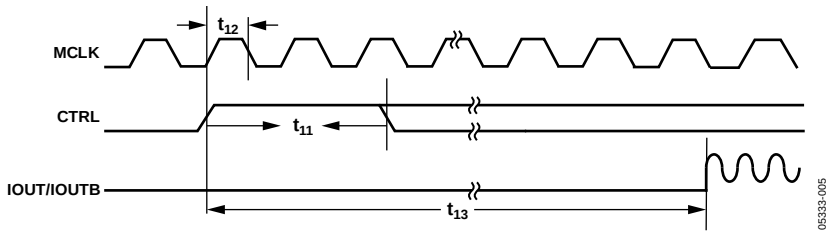

Figure 5. CTRL Timing

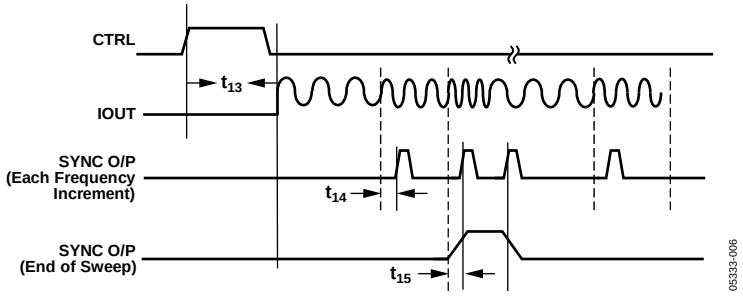

Figure 6. CTRL Timing, Saw-Sweep Mode

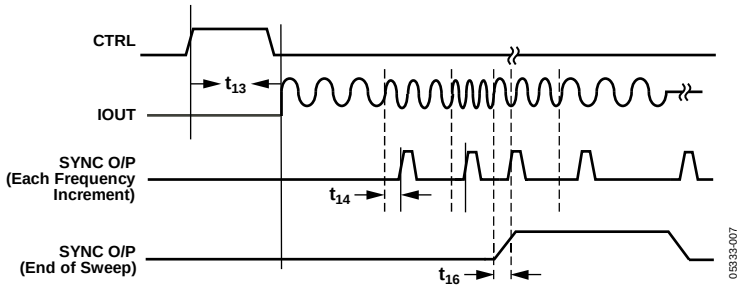

Figure 7. CTRL Timing, Triangular-Sweep Mode

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
AVDD to AGND	−0.3 V to +6.0 V
DVDD to DGND	−0.3 V to +6.0 V
AGND to DGND	−0.3 V to +0.3 V
CAP/2.5V to DGND	−0.3 V to 2.75 V
Digital I/O Voltage to DGND	−0.3 V to DVDD + 0.3 V
Analog I/O Voltage to AGND	−0.3 V to AVDD + 0.3 V
Operating Temperature Range	
Automotive (Y Version)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	+150°C
TSSOP Package (4-Layer Board)	
θ_{JA} Thermal Impedance	112°C/W
θ_{JC} Thermal Impedance	27.6°C/W
Reflow Soldering (Pb-Free)	300°C
Peak Temperature	260(+0/−5)°C
Time at Peak Temperature	10 sec to 40 sec

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

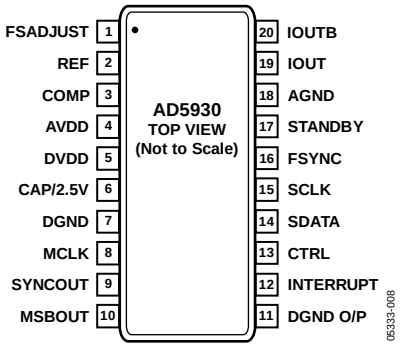

Figure 8. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	FSADJUST	Full-Scale Adjust Control. A resistor (RSET) must be connected externally between this pin and AGND. This determines the magnitude of the full-scale DAC current. The relationship between R_{SET} and the full-scale current is: $IOUT_{FULL\text{-}SCALE} = 18 \times V_{REFOUT}/R_{SET}$ where V_{REFOUT} = 1.20 V nominal and R_{SET} = 6.8 kΩ typical.
2	REF	Voltage Reference. This pin can be an input or an output. The AD5930 has an internal 1.18 V reference, which is made available at this pin. Alternatively, this reference can be overdriven by an external reference, with a voltage range as given in the Specifications section. A 10 nF decoupling capacitor should be connected between REF and AGND.
3	COMP	DAC Bias Pin. This pin is used for decoupling the DAC bias voltage to AVDD.
4	AVDD	Positive Power Supply for the Analog Section. AVDD can have a value from +2.3 V to +5.5 V. A 0.1 µF decoupling capacitor should be connected between AVDD and AGND.
5	DVDD	Positive Power Supply for the Digital Section. DVDD can have a value from +2.3 V to +5.5 V. A 0.1 µF decoupling capacitor should be connected between DVDD and DGND.
6	CAP/2.5V	Digital Circuitry. Operates from a 2.5 V power supply. This 2.5 V is generated from DVDD using an on-board regulator. The regulator requires a decoupling capacitor of typically 100 nF, which is connected from CAP/2.5V to DGND. If DVDD is equal to or less than 2.7 V, CAP/2.5V can be shorted to DVDD.
7	DGND	Ground for all Digital Circuitry. This excludes digital output buffers.
8	MCLK	Digital Clock Input. DDS output frequencies are expressed as a binary fraction of the frequency of MCLK. The output frequency accuracy and phase noise are determined by this clock.
9	SYNCOUT	Digital Output for Sweep Status Information. User selectable for end of sweep (EOS) or frequency increments through the control register (SYNCOP bit). This pin must be enabled by setting Control Register Bit SYNCOPEN to 1.
10	MSBOUT	Digital Output. The inverted MSB of the DAC data is available at this pin. This output pin must be enabled by setting bit MSBOUTEN in the control register to 1.
11	DGND O/P	Separate DGND Connection for Digital Output Buffers. Connect to DGND.
12	INTERRUPT	Digital Input. This pins acts as an interrupt during a frequency sweep. A low to high transition is sampled by the internal MCLK, which resets internal state machines. This results in the DAC output going to midscale.
13	CTRL	Digital Input. Triple function pin for initialization, start, and external frequency increments. A low-to-high transition, sampled by the internal MCLK, is used to initialize and start internal state machines, which then execute the pre-programmed frequency sweep sequence. When in auto-increment mode, a single pulse executes the entire sweep sequence. When in external increment mode, each frequency increment is triggered by a pulse.
14	SDATA	Serial Data Input. The 16-bit serial data-word is applied to this input with the register address first followed by the MSB to LSB of the data.
15	SCLK	Serial Clock Input. Data is clocked into the AD5930 on each falling SCLK edge.
16	FSYNC	Active Low Control Input. This is the frame synchronization signal for the serial data. When FSYNC is taken low, the internal logic is informed that a new word is being loaded into the device.
17	STANDBY	Active High Digital Input. When this pin is high, the internal MCLK is disabled, and the reference DAC and regulator are powered down. For optimum power saving, it is recommended to reset the AD5930 before putting it into standby, as this results in a shutdown current of typically 20 µA.

Pin No.	Mnemonic	Description
18	AGND	Ground for all Analog Circuitry.
19	IOUT	Current Output. This is a high impedance current source output. A load resistor of nominally 200 Ω should be connected between IOUT and AGND. A 20 pF capacitor to AGND is also recommended to act as a low-pass filter and to reduce clock feedthrough. In conjunction with IOUTB, a differential signal is available.
20	IOUTB	Current Output. IOUTB is the compliment of IOUT. This pin should preferably be tied through an external load resistor of 200 Ω to AGND, but can be tied directly to AGND. A 20 pF capacitor to AGND is also recommended as a low-pass filter to reduce clock feedthrough. In conjunction with IOUT, a differential signal is available.

TYPICAL PERFORMANCE CHARACTERISTICS

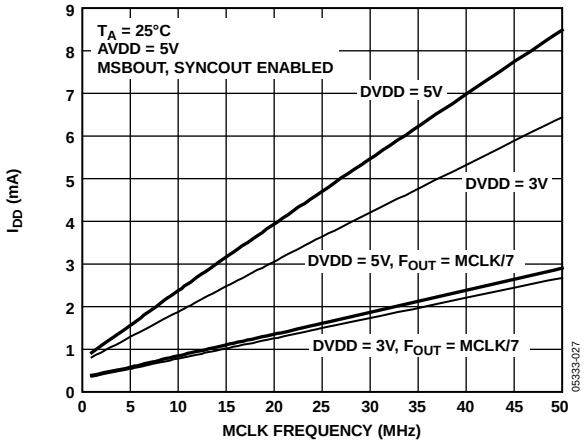

Figure 9. Current Consumption (I_{DD}) vs. MCLK Frequency

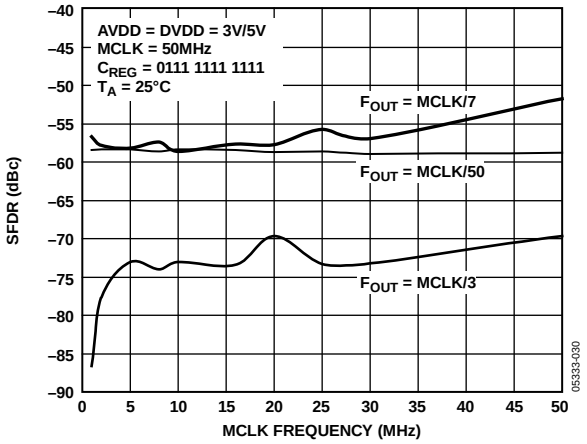

Figure 12. Wideband SFDR vs. MCLK Frequency

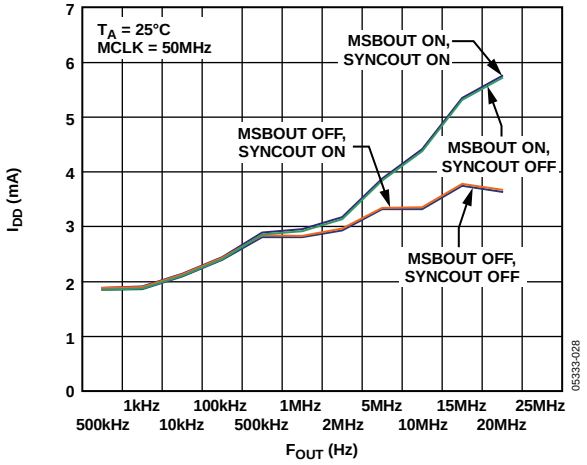

Figure 10. I_{DD} vs. F_{OUT} for Various Digital Output Conditions

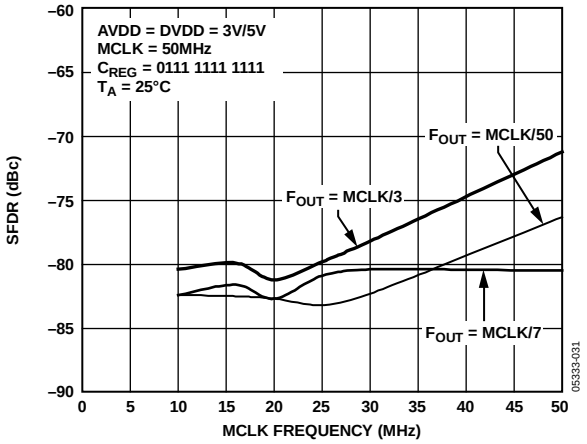

Figure 13. Narrowband SFDR vs. MCLK Frequency

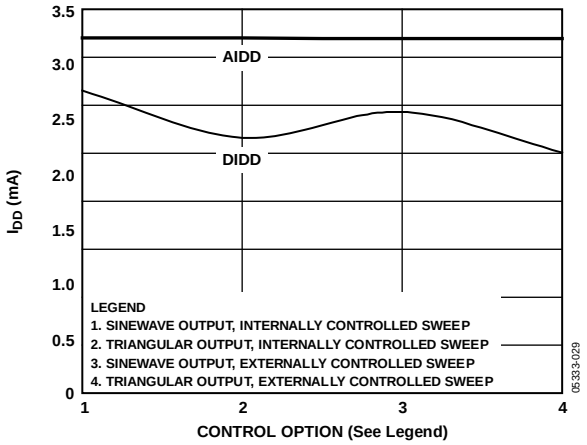

Figure 11. I_{DD} vs. Output Waveform Type and Control

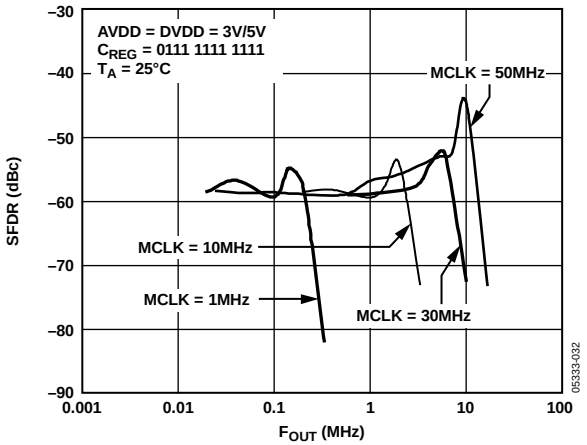

Figure 14. Wideband SFDR vs. F_{OUT} for Various MCLK Frequencies

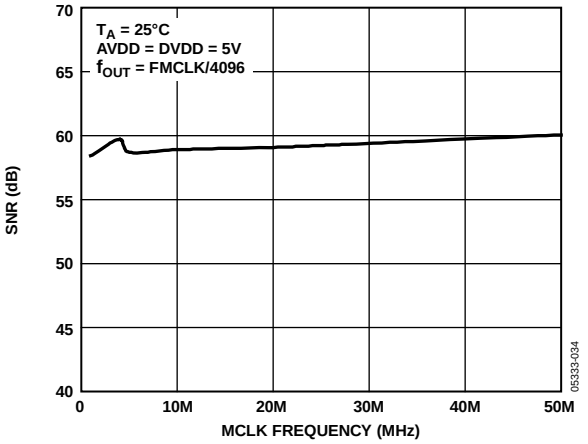

Figure 15. SNR vs. MCLK Frequency

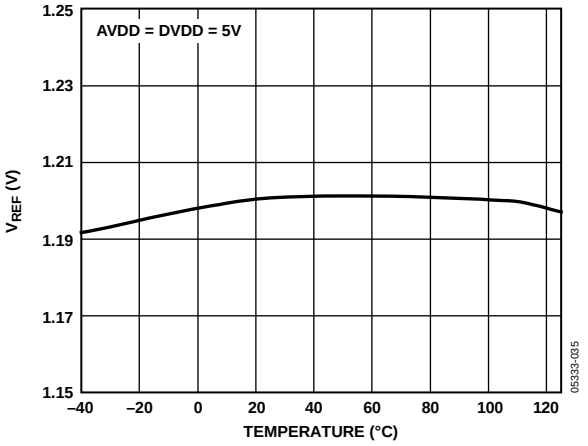

Figure 16. V_{REF} vs. Temperature

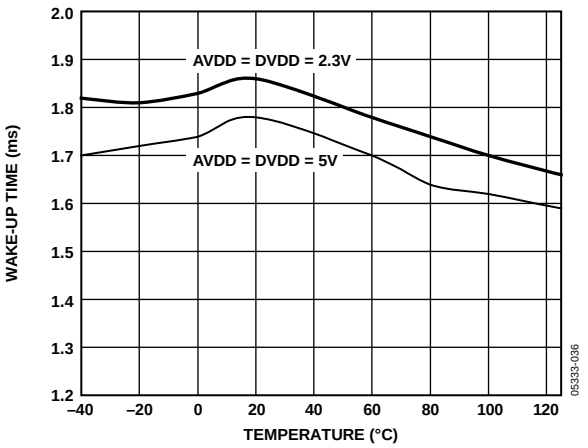

Figure 17. Wake-up Time vs. Temperature

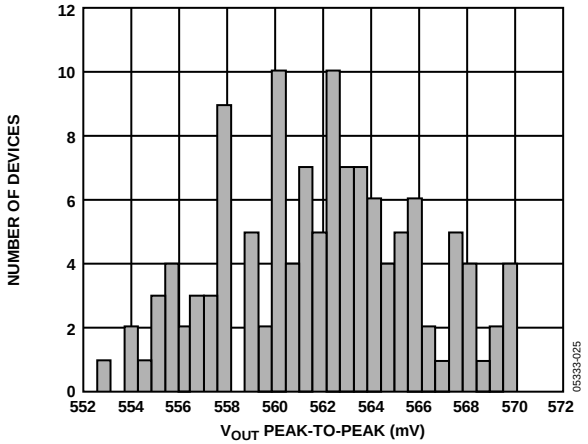

Figure 18. Histogram of V_{OUT} Peak-to-Peak

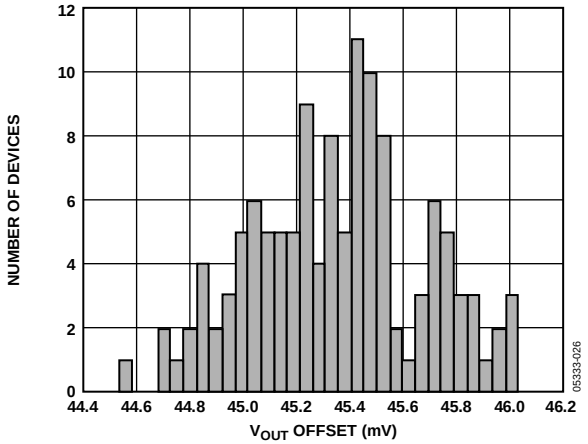

Figure 19. Histogram of V_{OUT} Offset

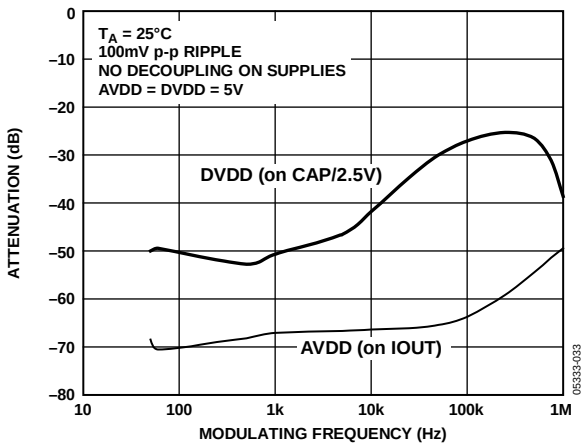

Figure 20. PSSR

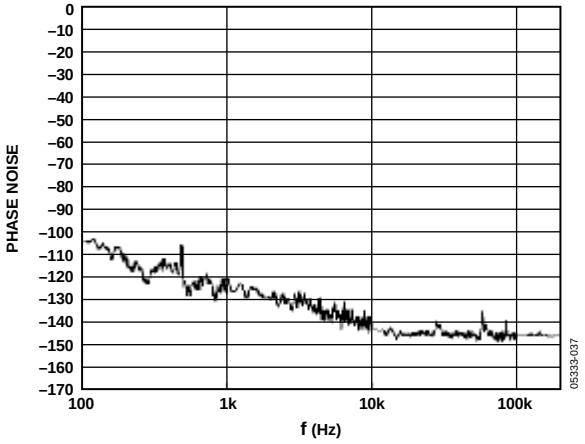

Figure 21. Output Phase Noise

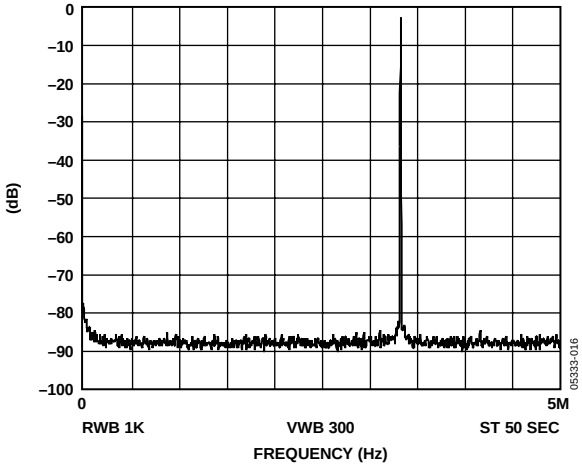

Figure 24. f_{MCLK} = 10 MHz; f_{OUT} = 3.33 MHz = f_{MCLK}/3, Frequency Word = 555555

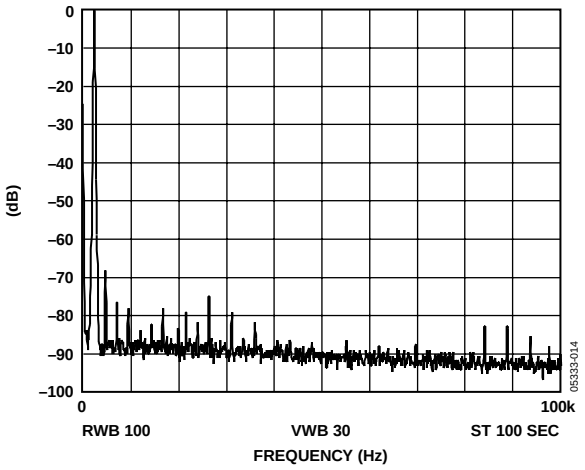

Figure 22. f_{MCLK} = 10 MHz; f_{OUT} = 2.4 kHz, Frequency Word = 000FBA

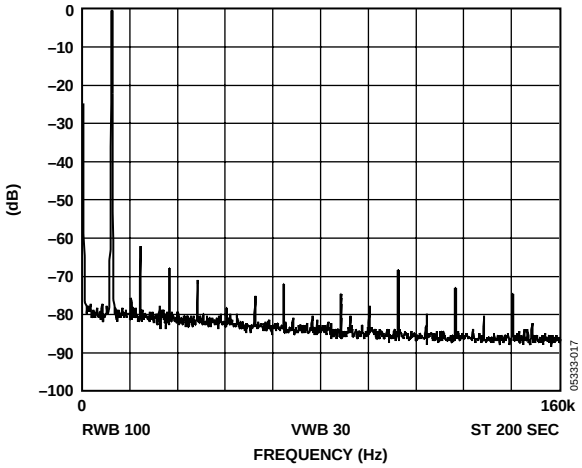

Figure 25. f_{MCLK} = 50 MHz; f_{OUT} = 12 kHz, Frequency Word = 000FBA

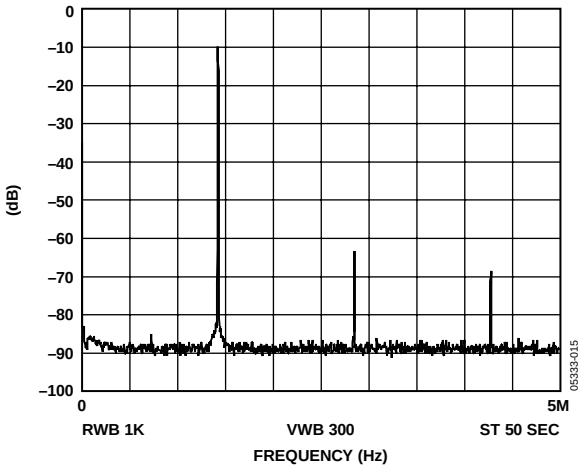

Figure 23. f_{MCLK} = 10 MHz; f_{OUT} = 1.43 MHz = f_{MCLK}/7, Frequency Word = 249249

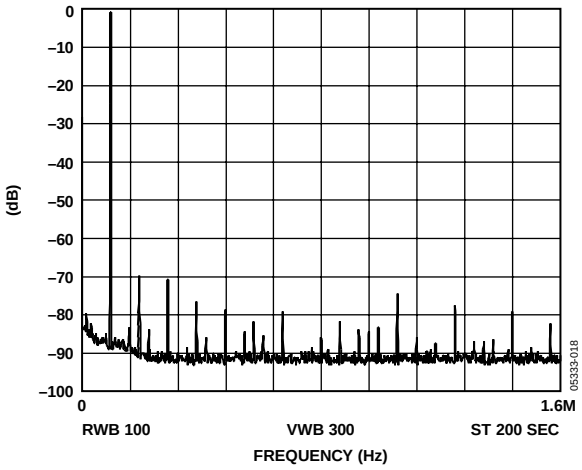

Figure 26. f_{MCLK} = 50 MHz; f_{OUT} = 120 kHz, Frequency Word = 009D49

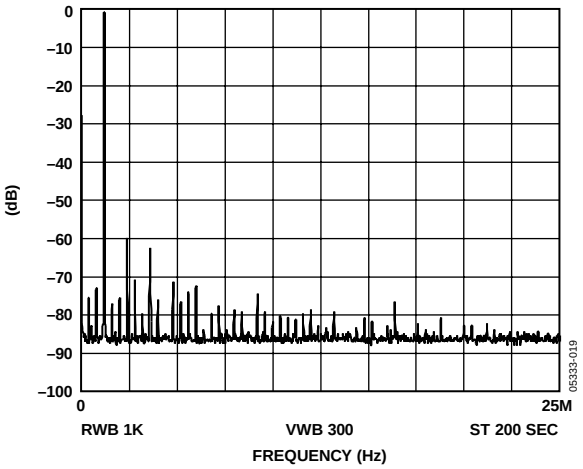

Figure 27. f_{MCLK} = 50 MHz;
f_{OUT} = 1.2 MHz, Frequency Word = 0624DD

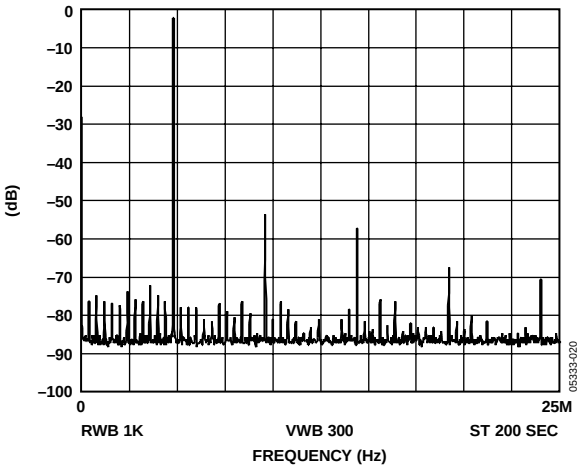

Figure 28. f_{MCLK} = 50 MHz;
f_{OUT} = 4.8 MHz, Frequency Word = 189374

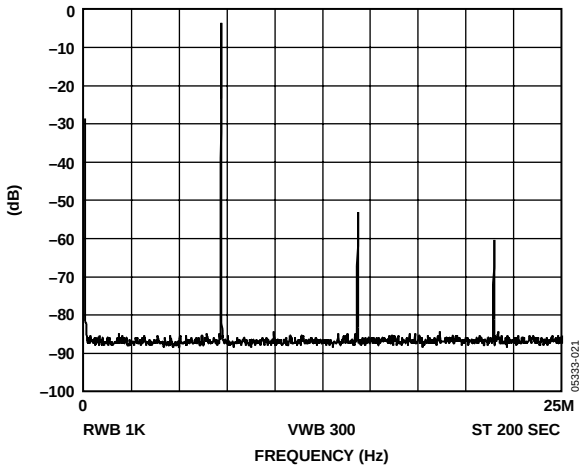

Figure 29. f_{MCLK} = 50 MHz; f_{OUT} = 7.143 MHz = f_{MCLK}/7,
Frequency Word = 2492492

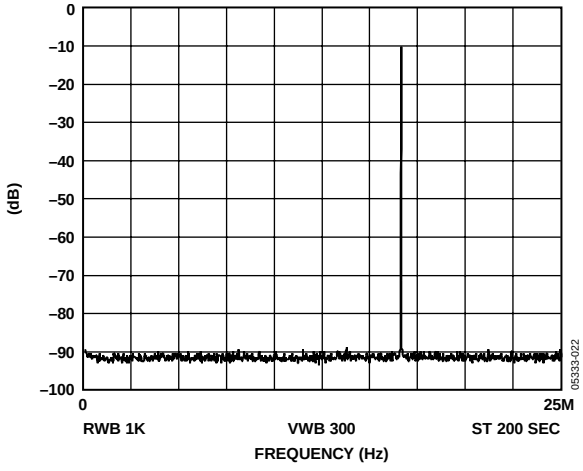

Figure 30. f_{MCLK} = 50 MHz; f_{OUT} = 16.667 MHz = f_{MCLK}/3,
Frequency Word = 5555555

TERMINOLOGY

Integral Nonlinearity (INL)
This is the maximum deviation of any code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are zero scale and full scale. The error is expressed in LSBs.

Differential Nonlinearity (DNL)
This is the difference between the measured and ideal 1 LSB change between two adjacent codes in the DAC. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity.

Output Compliance
The output compliance refers to the maximum voltage that can be generated at the output of the DAC to meet the specifications. When voltages greater than that specified for the output compliance are generated, the AD5930 may not meet the specifications listed in the data sheet.

Spurious-Free Dynamic Range (SFDR)
Along with the frequency of interest, harmonics of the fundamental frequency and images of these frequencies are present at the output of a DDS device. The SFDR refers to the largest spur or harmonic that is present in the band of interest. The wide band SFDR gives the magnitude of the largest harmonic or spur relative to the magnitude of the fundamental frequency in the 0 to Nyquist bandwidth. The narrow band SFDR gives the attenuation of the largest spur or harmonic in a bandwidth of ±200 kHz about the fundamental frequency.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of harmonics to the rms value of the fundamental. For the AD5930, THD is defined as

$$THD(\text{dB}) = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where:
V_1 is the rms amplitude of the fundamental.
V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through the sixth harmonic.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the measured output signal to the rms sum of all other spectral components below the Nyquist frequency. The value for SNR is expressed in decibels.

Clock Feedthrough
There is feedthrough from the MCLK input to the analog output. Clock feedthrough refers to the magnitude of the MCLK signal relative to the fundamental frequency in the AD5930's output spectrum.

THEORY OF OPERATION

The AD5930 is a general-purpose synthesized waveform generator capable of providing digitally programmable waveform sequences in both the frequency and time domain. The device contains embedded digital processing to provide a repetitive sweep of a user programmable frequency profile allowing enhanced frequency control. Because the device is pre-programmable, it eliminates continuous write cycles from a DSP/µcontroller in generating a particular waveform.

THE FREQUENCY PROFILE

The frequency profile is defined by the start frequency (F_{START}), the frequency increment (Δf) and the number of increments per sweep (N_{INCR}). The increment interval between frequency increments, t_{INT}, is either user programmable with the interval automatically determined by the device (auto-increment mode), or externally controlled via a hardware pin (external increment mode). For automatic update, the interval profile can either be for a fixed number of clock periods or for a fixed number of output waveform cycles.

In the auto-increment mode, a single pulse at the CTRL pin starts and executes the frequency sweep. In the external increment mode, the CTRL pin also starts the sweep, but the frequency increment interval is determined by the time interval between sequential 0/1 transitions on the CTRL pin. Furthermore, the CTRL pin can be used to directly control the burst profile, where during the input high time, the output waveform is present, and during the input low time, the output is reset to midscale.

The frequency profile can be swept in two different modes: saw sweep or triangular (up/down) sweep.

Saw-Sweep Mode

In the case of a saw sweep, the AD5930 repeatedly sweeps between sweep start to sweep end, that is, from F_{START} incrementally to

$$F_{START} + N_{INCR} \times \Delta f$$

and then returns directly to F_{START} to begin again (see Figure 31).

This gives a saw-sweep cycle time of

$$(N_{INCR} + 1) \times t_{INT}$$

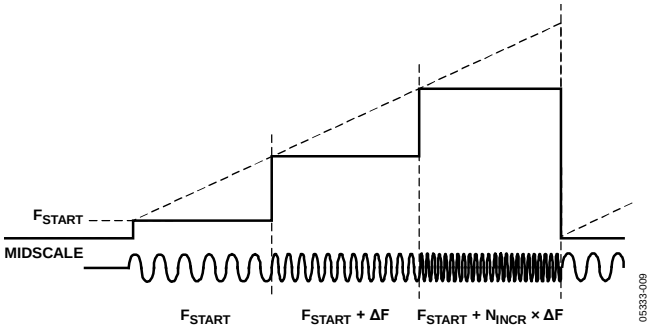

Figure 31. Saw-Sweep Profile

Triangular-Sweep Mode

In the case of a triangular sweep, the AD5930 repeatedly sweeps between sweep start to sweep end, that is, from F_{START} incrementally to

$$F_{START} + N_{INCR} \times \Delta f$$

and then returns to F_{START} in a decremented manner (see Figure 32).

The triangular-sweep cycle time is given by

$$(1 + (2 \times N_{INCR})) \times t_{INT}$$

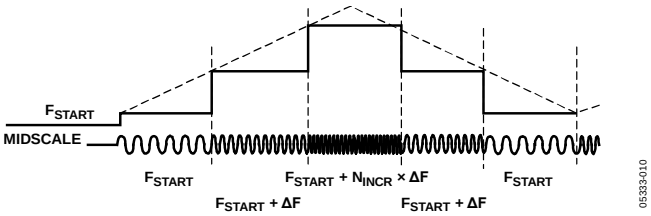

Figure 32. Triangular-Sweep Profile

OUTPUT MODES

The AD5930 offers two possible output modes: continuous output mode and burst output mode. Both of these modes are illustrated in Figure 33.

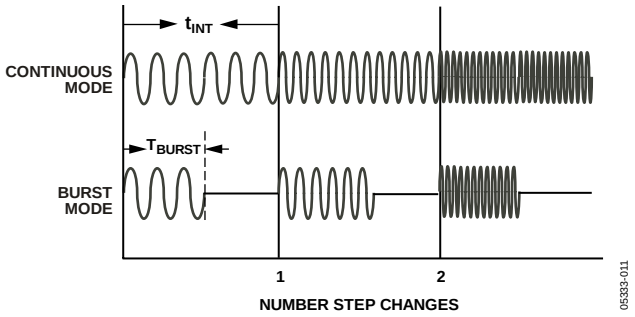

Figure 33. Continuous Mode and Burst Mode of the AD5930

Continuous Output Mode

In this mode, each frequency of the sweep is available for the length of time programmed into the time interval (t_{INT}) register. This means the frequency swept output signal is continuously available, and is therefore phase continuous at all frequency increments.

To set up the AD5930 in continuous mode, the CW/BURST bit (D7) in the control register must be set to 0. See the Activating and Controlling the Sweep section for more details.

Burst Output Mode

In this mode, the AD5930 provides a programmable burst of the waveform output for a fixed length of time (T_{BURST}) within the programmed increment interval (t_{INT}). Then for the remainder of the t_{INT} interval, the output is reset to mid-

scale and remains there until the next frequency increment. This is beneficial for applications where the user needs to burst a frequency for a set period, and then "listen" for a response before increasing to the next frequency. Note also that the beginning of each frequency increment is at midscale (Phase 0 Rad). Therefore, the phase of the signal is always known.

To set up the AD5930 in burst mode, the CW/BURST bit (D7) in the control register must be set to 1. See the Activating and Controlling the Sweep section for more details about the burst output mode.

SERIAL INTERFACE

The AD5930 has a standard 3-wire serial interface, which is compatible with SPI®, QSPI™, MICROWIRE™, and DSP interface standards.

Data is loaded into the device as a 16-bit word under the control of a serial clock input, SCLK. The timing diagram for this operation is given in Figure 4.

The FSYNC input is a level-triggered input that acts as a frame synchronization and chip enable. Data can only be transferred into the device when FSYNC is low. To start the serial data transfer, FSYNC should be taken low, observing the minimum FSYNC to SCLK falling edge setup time, t_7. After FSYNC goes low, serial data is shifted into the device's input shift register on the falling edges of SCLK for 16 clock pulses. FSYNC can be taken high after the 16th falling edge of SCLK, observing the minimum SCLK falling edge to FSYNC rising edge time, t_8. Alternatively, FSYNC can be kept low for a multiple of 16 SCLK pulses, and then brought high at the end of the data transfer. In this way, a continuous stream of 16-bit words can be loaded while FSYNC is held low. FSYNC should only go high after the 16th SCLK falling edge of the last word is loaded.

The SCLK can be continuous, or, alternatively, the SCLK can idle high or low between write operations.

POWERING UP THE AD5930

When the AD5930 is powered up, the part is in an undefined state, and therefore, must be reset before use. The eight registers (control and frequency) contain invalid data and need to be set to a known value by the user. The control register should be the first register to be programmed, as this sets up the part. Note that a write to the control register automatically resets the internal state machines and provides an analog output of midscale as it provides the same function as the INTERRUPT pin. Typically, this is followed by a serial loading of all the required sweep parameters. The DAC output remains at midscale until a sweep is started using the CTRL pin.

PROGRAMMING THE AD5930

The AD5930 is designed to provide automatic frequency sweeps when the CTRL pin is triggered. The automatic sweep is controlled by a set of registers, the addresses of which are given in Table 5. The function of each register is described in more detail in the following section.

Table 5. Register Addresses

Register Address					
D15	D14	D13	D12	Mnemonic	Name
0	0	0	0	C_{REG}	Control bits
0	0	0	1	N_{INCR}	Number of increments
0	0	1	0	Δf	Lower 12 bits of delta frequency
0	0	1	1	Δf	Higher 12 bits of delta frequency
0	1			t_{INT}	Increment interval
1	0			T_{BURST}	Burst interval
1	1	0	0	F_{START}	Lower 12 bits of start frequency
1	1	0	1	F_{START}	Higher 12 bits of start frequency
1	1	1	0		Reserved
1	1	1	1		Reserved

The Control Register

The AD5930 contains a 12-bit control register (see Table 6) that sets up the operating modes of the AD5930. The different functions and the various output options from the AD5930 are controlled by this register. Table 7 describes the individual bits of the control register.

To address the control register, D15 to D12 of the 16-bit serial word must be set to 0.

Table 6. Control Register

D15	D14	D13	D12	D11 to D0
0	0	0	0	Control Bits

Table 7. Description of Bits in the Control Register

Bit	Name	Function
D15 to D12	ADDR	Register address bits.
D11	B24	Two write operations are required to load a complete word into the F_{START} register and the Δf register. When B24 = 1, a complete word is loaded into a frequency register in two consecutive writes. The first write contains the 12 LSBs of the frequency word and the next write contains the 12 MSBs. Refer to Table 5 for the appropriate addresses. The write to the destination register occurs after both words have been loaded, so the register never holds an intermediate value. When B24 = 0, the 24-bit F_{START} /Δf register operates as two 12-bit registers, one containing the 12 MSBs and the other containing the 12 LSBs. This means that the 12 MSBs of the frequency word can be altered independent of the 12 LSBs and vice versa. This is useful if the complete 24-bit update is not required. To alter the 12 MSBs or the 12 LSBs, a single write is made to the appropriate register address. Refer to Table 5 for the appropriate addresses.
D10	DAC ENABLE	When DAC ENABLE = 1, the DAC is enabled. When DAC ENABLE = 0, the DAC is powered down. This saves power and is beneficial when only using the MSB of the DAC input data (available at the MSBOUT pin).
D9	SINE/TRI	The function of this bit is to control what is available at the IOUT/IOUTB pins. When SINE/TRI = 1, the SIN ROM is used to convert the phase information into amplitude information resulting in a sinusoidal signal at the output. When SINE/TRI = 0, the SIN ROM is bypassed, resulting in a triangular (up-down) output from the DAC.
D8	MSBOUTEN	When MSBOUTEN = 1, the MSBOUT pin is enabled. When MSBOUTEN = 0, the MSBOUT is disabled (tri-state).
D7	CW/BURST	When CW/BURST = 1, the AD5930 outputs each frequency continuously for the length of time or number of output waveform cycles specified in the appropriate register, T_{BURST}. When CW/BURST = 0, the AD5930 bursts each frequency for the length of time/number of cycles specified in the burst register, T_{BURST}. For the remainder of the time within each increment window ($T_{BURST} - t_{INT}$), the AD5930 outputs a DC value of midscale. In external increment mode, it is defined by the pulse widths on the CTRL pin.
D6	INT/EXT BURST	This bit is active when D7 = 0 and is also used in conjunction with D5. When the user is incrementing the frequency externally (D5 = 1), D6 dictates whether the user is controlling the burst internally or externally. When INT/EXT BURST = 1, the output burst is controlled externally through the CTRL pin. This is useful if the user is using an external source to both trigger the frequency increments and determine the burst interval. When INT/EXT BURST = 0, the output burst is controlled internally. The burst is pre-programmed by the user into the T_{BURST} register (the burst interval can either be clock-based or for a specified number of output cycles). When D5 = 0, this bit is ignored.
D5	INT/EXT INCR	When INT/EXT INCR = 1, the frequency increments are triggered externally through the CTRL pin. When INT/EXT INCR = 0, the frequency increments are triggered automatically.
D4	MODE	The function of this bit is to control what type of frequency sweep is carried out. When MODE = 1, the frequency profile is a saw sweep. When MODE = 0, the frequency profile is a triangular (up-down) sweep.
D3	SYNCSEL	This bit is active when D2 = 1. It is user-selectable to pulse at the end of sweep (EOS) or at each frequency increment. When SYNCSEL = 1, the SYNCOP pin outputs a high level at the end of the sweep and returns to zero at the start of the subsequent sweep. When SYNCSEL= 0, the SYNCOP outputs a pulse of $4 \times T_{CLOCK}$ only at each frequency increment.
D2	SYNCOUTEN	When SYNCOUTEN= 1, the SYNC output is available at the SYNCOP pin. When SYNCOUTEN= 0, the SYNCOP pin is disabled (tri-state).
D1	Reserved	This bit must always be set to 1.
D0	Reserved	This bit must always be set to 1.

SETTING UP THE FREQUENCY SWEEP

As stated previously in The Frequency Profile section, the AD5930 requires certain registers to be programmed to enable a frequency sweep. The following sections discuss these registers in more detail.

Start Frequency (F_{START})

To start a frequency sweep, the user needs to tell the AD5930 what frequency to start sweeping from. This frequency is stored in a 24-bit register called F_{START}. If the user wishes to alter the entire contents of the F_{START} register, two consecutive writes must be performed, one to the LSBs and the other to the MSBs. Note that for an entire write to this register, the Control Bit B24 (D11) should be set to 1 with the LSBs programmed first.

In some applications, the user does not need to alter all 24 bits of the F_{START} register. By setting the Control Bit B24 (D11) to 0, the 24-bit register operates as two 12-bit registers, one containing the 12 MSBs and the other containing the 12 LSBs. This means that the 12 MSBs of the F_{START} word can be altered independently of the 12 LSBs, and vice versa. The addresses of both the LSBs and the MSBs of this register is given in Table 8.

Table 8. F_{START} Register Bits

D15	D14	D13	D12	D11 to D0
1	1	0	0	12 LSBs of F_{START} <11…0>
1	1	0	1	12 MSBs of F_{START} <23…12>

Frequency Increments (Δf)

The value in the Δf register sets the increment frequency for the sweep and is added incrementally to the current output frequency. Note that the increment frequency can be positive or negative, thereby giving an increasing or decreasing frequency sweep.

At the start of a sweep, the frequency contained in the F_{START} register is output. Next, the frequency (F_{START} + Δf) is output. This is followed by (F_{START} + Δf + Δf) and so on. Multiplying the Δf value by the number of increments (N_{INCR}), and adding it to the start frequency (F_{START}), gives the final frequency in the sweep. Mathematically this final frequency/stop frequency is represented by

$$F_{START} + (N_{INCR} \times \Delta f).$$

The Δf register is a 23-bit register, and requires two 16-bit writes to be programmed. Table 9 gives the addresses associated with both the MSB and LSB registers of the Δf word.

Table 9. Δf Register Bits

D15	D14	D13	D12	D11	D10 to D0	Sweep Direction
0	0	1	0	12 LSBs of Δf <11…0>		N/A
0	0	1	1	0	11 MSBs of Δf <22…12>	Positive Δf (F_{START} + Δf)
0	0	1	1	1	11 MSBs of Δf <22…12>	Negative Δf (F_{START} − Δf)

Number of Increments (N_{INCR})

An end frequency, or a maximum/minimum frequency before the sweep changes direction is not required on the AD5930. Instead, this end frequency is calculated by multiplying the frequency increment value (Δf) by the number of frequency steps (N_{INCR}), and adding it to/subtracting it from the start frequency (F_{START}), that is, F_{START} + N_{INCR} × Δf. The N_{INCR} register is a 12-bit register, with the address shown in Table 10.

Table 10. N_{INCR} Register Bits

D15	D14	D13	D12	D11 to D0
0	0	0	1	12 bits of N_{INCR} <11…0>

The number of increments is programmed in binary fashion, with 000000000010 representing the minimum number of frequency increments (2 increments), and 111111111111 representing the maximum number of increments (4095).

Table 11. N_{INCR} Data Bits

D11		D0	Number of Increments
0000	0000	0010	2 frequency increments. This is the minimum number of frequency increments.
0000	0000	0011	3 frequency increments.
0000	0000	0100	4 frequency increments.
…	…	…	…
1111	1111	1110	4094 frequency increments.
1111	1111	1111	4095 frequency increments.

Increment Interval (t_{INT})

The increment interval dictates the duration of the DAC output signal for each individual frequency of the frequency sweep. The AD5930 offers the user two choices:

- The duration is a multiple of cycles of the output frequency.
- The duration is a multiple of MCLK periods.

This is selected by Bit D13 in the t_{INT} register as shown in Table 12.

Table 12. t_{INT} Register Bits

D15	D14	D13	D12	D11	D10 to D0
0	1	0	x	x	11 bits <10…0> Fixed number of output waveform cycles.
0	1	1	x	x	11 bits <10…0> Fixed number of clock periods.

Programming of this register is in binary form with the minimum number being decimal 2. Note in Table 12 that 11 bits, Bit D10 to Bit D0, of the register are available to program the time interval. As an example, if MCLK = 50 MHz, then each clock period/base interval is (1/50 MHz) = 20 ns. If each frequency needs to be output for 100 ns, then <00000000101> or decimal 5 needs to be programmed to this register. Note that the AD5930 can output each frequency for a maximum duration of 211 −1 (or 2047) times the increment interval.

Therefore, in this example, a time interval of 20 ns × 2047 = 40 µs is the maximum, with the minimum being 40 ns. For some applications, this maximum time of 40 µs may be insufficient. Therefore, to cater for sweeps that need a longer increment interval, time-base multipliers are provided. Bit D12 and Bit D11 are dedicated to the time-base multipliers (see Table 12). A more detailed table of the multiplier options is given in Table 13.

Table 13. Time-Base Multiplier Values

D12	D11	Multiplier Value
0	0	Multiply (1/MCLK) by 1
0	1	Multiply (1/MCLK) by 5
1	0	Multiply (1/MCLK) by 100
1	1	Multiply (1/MCLK) by 500

If MCLK is 50 MHz and a multiplier of 500 is used, then the base interval (T_{BASE}) is now (1/(50 MHz) x 500)) = 10 µs. Using a multiplier of 500, the maximum increment interval is 10 µs × 2^{11-1} = 20.5 ms. Therefore, the option of time-base multipliers gives the user enhanced flexibility when programming the length of the frequency window, because any frequency can be output for a minimum of 40 ns up to a maximum of 20.5 ms.

Length of Sweep Time

The length of time to complete a user-programmed frequency sweep is given by the following equation:

$$T_{SWEEP} = (1 + N_{INCR}) \times T_{BASE}$$

Burst Time Resister (T_{BURST})

As previously described in the Burst Output Mode section, the AD5930 offers the user the ability to output each frequency in the sweep for a length of time within the increment interval (t_{INT}), and then return to midscale for the remainder of the time ($t_{INT} - T_{BURST}$) before stepping to the next frequency. The burst option must be enabled. This is done by setting Bit D7 in the control register to 0.

Similar to the time interval register, the burst register can have its duration as:

- A multiple of cycles of the output frequency
- A multiple of MCLK periods

The address for this register is given in Table 14.

Table 14. T_{BURST} Register Bits

D15	D14	D13	D12	D11	D10 to D0
1	0	0	x	x	11 bits of <0…10> Fixed number of output waveform cycles.
1	0	1	x	x	11 bits of <0…10> Fixed number of clock periods.

However, note that when using both the increment interval (t_{INT}) and burst time register (T_{BURST}), the settings for Bit D13 should be the same. In instances where they differ, the AD5930 defaults to the value programmed into the t_{INT} register. Similarly, Bit 12 and Bit 11, the time-base multiplier bits, always default to the value programmed into the t_{INT} register.

ACTIVATING AND CONTROLLING THE SWEEP

After the registers have been programmed, a 0 ≥ 1 transition on the CTRL pin starts the sweep. The sweep always starts from the frequency programmed into the F_{START} register. It changes by the value in the ΔF register and increases by the number of steps in the N_{INCR} register. However, both the time interval and burst duration of each frequency can be internally controlled using the t_{INT} and T_{BURST} registers, or externally using the CTRL pin. The options available are:

- Auto-increment, auto-burst control
- External increment, auto-burst control
- External increment, external burst control

Auto-Increment, Auto-Burst Control

The values in the t_{INT} and T_{BURST} registers are used to control the sweep. The AD5930 bursts each frequency for the length of time programmed in the T_{BURST} register, and outputs midscale for the remainder of the interval time ($t_{INT} - T_{BURST}$).

To set up the AD5930 to this mode, CW/BURST (Bit D7) in the control register must be set to 0, INT/EXT BURST (Bit D6) must be set to 0, and INT/EXT INCR (Bit D5) must be set to 0. Note that if the part is only operating in continuous mode, then (Bit D7) in the control register should be set to 1.

External Increment, Auto-Burst Control

The time interval, t_{INT}, is set by the pulse rate on the CTRL pin. The first 0 ≥1 transition on the pin starts the sweep. Each subsequent 0 ≥1 transition on the CTRL pin increments the output frequency by the value programmed into the ΔF register. For each increment interval, the AD5930 outputs each frequency for the length of time programmed into the T_{BURST} register, and outputs midscale until the CTRL pin is pulsed again. Note that for this mode, the values programmed into Bit D13, Bit D12, and bit D11 of the T_{BURST} register are used.

To setup the AD5930 to this mode, CW/BURST (Bit D7) in the control register must be set to 0, INT/EXT BURST (Bit D6) must be set to 0, and INT/EXT INCR (Bit D5) must be set to 1. Note that if the part is only operating in continuous mode, then Bit D7 in the control register should be set to 1.

External Increment, External Burst Control

Both the increment interval (t_{INT}) and the burst interval (T_{BURST}) are controlled by the CTRL pin. A 0 ≥ 1 transition on the CTRL pin starts the sweep. The duration of CTRL high then dictates the length of time the AD5930 bursts that frequency. The low time of CTRL is the "listen" time, that is, how long the part remains at midscale. Bringing the CTRL pin high again initiates a frequency increment, and the pattern continues. For this mode, the settings for Bit D13, Bit D12, and Bit D11 are ignored.

To setup the AD5930 to this mode, CW/BURST (Bit D7) in the control register must be set to 0, INT/EXT BURST (Bit D6) must be set to 1, and INT/EXT INCR (Bit D5) must be set to 1. Note that if the part is only operating in continuous mode, then Bit D7 in the control register should be set to 1.

Interrupt Pin

This function is used as an interrupt during a frequency sweep. A low-to-high transition on this pin is sampled by the internal MCLK, thereby resetting internal state machines, which results in the output going to midscale.

Standby Pin

Sections of the AD5930 that are not in use can be powered down to minimize power consumption. This is done by using the STANDBY pin. For the optimum power savings, it is recommended to reset the AD5930 before entering standby, because doing so reduces the power-down current to 20 µA.

When this pin is high, the internal MCLK is disabled, and the reference, DAC, and regulator are powered down. When in this state, the DAC output of the AD5930 remains at its present value as the NCO is no longer accumulating. When the device is taken back out of standby mode, the MCLK is re-activated and the sweep continues. To ensure correct operation for new data, it is recommended that the device be internally reset using a control register write or using the INTERRUPT pin, and then restarted.

OUTPUTS FROM THE AD5930

The AD5930 offers a variety of outputs from the chip. The analog outputs are available from the IOUT/IOUTB pins, and include a sine wave and a triangle output. The digital outputs are available from the MSBOUT pin and the SYNCOUT pin.

Analog Outputs

Sinusoidal Output

The SIN ROM is used to convert the phase information from the frequency register into amplitude information, which results in a sinusoidal signal at the output. To have a sinusoidal output from the IOUT/IOUTB pins, set Bit SINE/TRI (Bit D9) to 1.

Triangle Output

The SIN ROM can be bypassed so that the truncated digital output from the NCO is sent to the DAC. In this case, the output is no longer sinusoidal. The DAC produces a 10-bit linear triangular function. To have a triangle output from the IOUT/IOUTB pins, set Bit SINE/TRI (D9) to 0. Note that the DAC ENABLE bit (D10) must be 1 (that is, the DAC is enabled) when using these pins.

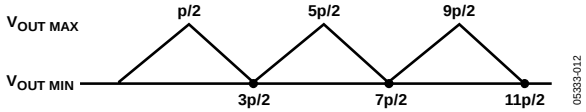

Figure 34. Triangle Output

Digital Outputs

Square Wave Output from MSBOUT

The inverse of the MSB from the NCO can be output from the AD5930. By setting the MSBOUTEN (D8) control bit to 1, the inverted MSB of the DAC data is available at the MSBOUT pin. This is useful as a digital clock source.

Figure 35. MSB Output

SYNCOUT Pin

The SYNCOUT pin can be used to give the status of the sweep. It is user selectable for the end of the sweep, or to output a 4 × T_{CLOCK} pulse at frequency increments. The timing information for both of these modes is shown in Figure 6 and Figure 7.

The SYNCOUT pin must be enabled before use. This is done using Bit D2 in the control register. The output available from this pin is then controlled by Bit D3 in the control register. See Table 5 for more information.

APPLICATIONS INFORMATION

GROUNDING AND LAYOUT

The printed circuit board that houses the AD5930 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be easily separated. A minimum etch technique is generally best for ground planes because it gives the best shielding. Digital and analog ground planes should only be joined in one place. If the AD5930 is the only device requiring an AGND to DGND connection, then the ground planes should be connected at the AGND and DGND pins of the AD5930. If the AD5930 is in a system where multiple devices require AGND to DGND connections, the connection should be made at one point only, a star ground point that should be established as close as possible to the AD5930.

Avoid running digital lines under the device as these couple noise onto the die. The analog ground plane should be allowed to run under the AD5930 to avoid noise coupling. The power supply lines to the AD5930 should use as large a track as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals, such as clocks, should be shielded with digital ground to avoid radiating noise to other sections of the board. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best, but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes, while signals are placed on the other side.

Good decoupling is important. The analog and digital supplies to the AD5930 are independent and separately pinned out to minimize coupling between analog and digital sections of the device. All analog and digital supplies should be decoupled to AGND and DGND, respectively, with 0.1 µF ceramic capacitors in parallel with 10 µF tantalum capacitors. To achieve the best from the decoupling capacitors, they should be placed as close as possible to the device, ideally right up against the device. In systems where a common supply is used to drive both the AVDD and DVDD of the AD5930, it is recommended that the system's AVDD supply be used. This supply should have the recommended analog supply decoupling between the AVDD pins of the AD5930 and AGND, and the recommended digital supply decoupling capacitors between the DVDD pins and DGND.

Proper operation of the comparator requires good layout strategy. The strategy must minimize the parasitic capacitance between V_{IN} and the SIGN BIT OUT pin by adding isolation using a ground plane. For example, in a multilayered board, the V_{IN} signal could be connected to the top layer and the SIGN BIT OUT connected to the bottom layer, so that isolation is provided between the power and ground planes.

Interfacing to Microprocessors

The AD5930 has a standard serial interface that allows the part to interface directly with several microprocessors. The device uses an external serial clock to write the data/control information into the device. The serial clock can have a frequency of 40 MHz maximum. The serial clock can be continuous, or it can idle high or low between write operations. When data/control information is being written to the AD5930, FSYNC is taken low and is held low while the 16 bits of data are being written into the AD5930. The FSYNC signal frames the 16 bits of information being loaded into the AD5930.

AD5930 TO ADSP-21467 INTERFACE

Figure 36 shows the serial interface between the AD5930 and the ADSP-21467. The ADSP-21467 should be set up to operate in the SPORT transmit alternate framing mode (TFSW = 1). The ADSP-21467 is programmed through the SPORT control register and should be configured as follows:

1. Internal clock operation (ISCLK = 1)
2. Active low framing (INVTFS = 1)
3. 16-bit word length (SLEN = 15)
4. Internal frame sync signal (ITFS = 1)
5. Generate a frame sync for each write (TFSR = 1)

Transmission is initiated by writing a word to the Tx register after the SPORT has been enabled. The data is clocked out on each rising edge of the serial clock and clocked into the AD5930 on the SCLK falling edge.

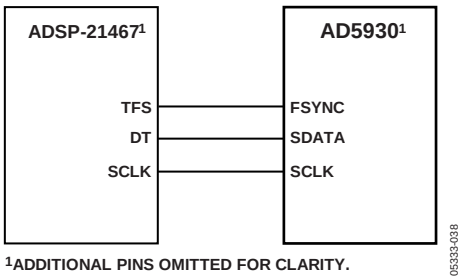

Figure 36. ADSP-21467 to AD5930 Interface

AD5930 TO 68HC11/68L11 INTERFACE

Figure 37 shows the serial interface between the AD5930 and the 68HC11/68L11 µcontroller. The µcontroller is configured as the master by setting bit MSTR in the SPCR to 1, which provides a serial clock on SCK while the MOSI output drives the serial data line SDATA. Since the µcontroller does not have a dedicated frame sync pin, the FSYNC signal is derived from a port line (PC7). The setup conditions for correct operation of the interface are as follows:

1. SCK idles high between write operations (CPOL = 0)
2. Data is valid on the SCK falling edge (CPHA = 1)

When data is being transmitted to the AD5930, the FSYNC line is taken low (PC7). Serial data from the 68HC11/68L11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. Data is transmitted MSB first. In order to load data into the AD5930, PC7 is held low after the first 8 bits are transferred and a second serial write operation is performed to the AD5930. Only after the second 8 bits have been transferred should FSYNC be taken high again.

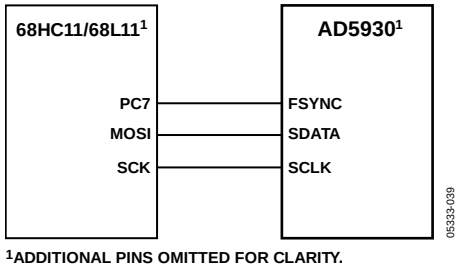

Figure 37. 68HC11/68L11 to AD5930 Interface

AD5930 TO 80C51/80L51 INTERFACE

Figure 38 shows the serial interface between the AD5930 and the 80C51/80L51 µcontroller. The µcontroller is operated in mode 0 so that TXD of the 80C51/80L51 drives SCLK of the AD5930, while RXD drives the serial data line SDATA. The FSYNC signal is again derived from a bit programmable pin on the port (P3.3 being used in the diagram). When data is to be transmitted to the AD5930, P3.3 is taken low. The 80C51/80L51 transmits data in 8-bit bytes, thus, only eight falling SCLK edges occur in each cycle. To load the remaining 8 bits to the AD5930, P3.3 is held low after the first 8 bits have been transmitted, and a second write operation is initiated to transmit the second byte of data. P3.3 is taken high following the completion of the second write operation. SCLK should idle high between the two write operations. The 80C51/80L51 outputs the serial data in an LSB first format. The AD5930 accepts the MSB first (the 4 MSBs being the control information, the next 4 bits being the address while the 8 LSBs contain the data when writing to a destination register). Therefore, the transmit routine of the 80C51/80L51 must take this into account and rearrange the bits so that the MSB is output first.

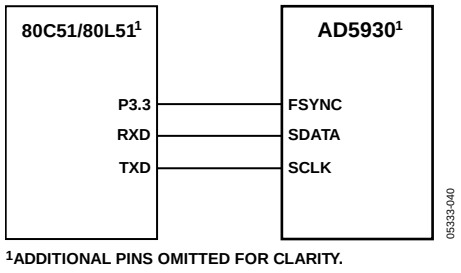

Figure 38. 80C51/80L51 to AD5930 Interface

AD5930 TO DSP56002 INTERFACE

Figure 39 shows the interface between the AD5930 and the DSP56002. The DSP56002 is configured for normal mode, asynchronous operation with a gated internal clock (SYN = 0, GCK = 1, SCKD = 1). The frame sync pin is generated internally (SC2 = 1), the transfers are 16 bits wide (WL1 = 1, WL0 = 0), and the frame sync signal frames the 16 bits (FSL = 0). The frame sync signal is available on Pin SC2, but needs to be inverted before being applied to the AD5930. The interface to the DSP56000/DSP56001 is similar to that of the DSP56002.

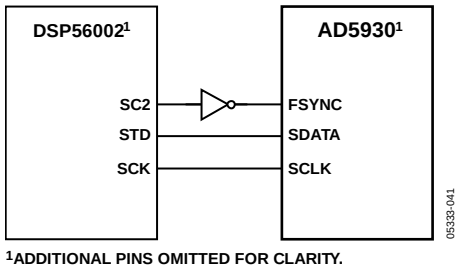

Figure 39. DSP56002 to AD5930 Interface

EVALUATION BOARD

The AD5930 evaluation board allows designers to evaluate the high performance AD5930 DDS modulator with minimum effort.

The evaluation board interfaces to the USB port of a PC. It is possible to power the entire board off the USB port. All that is needed to complete the evaluation of the chip is either a spectrum analyzer or a scope.

The DDS evaluation kit includes a populated and tested AD5930 printed circuit board. The EVAL-AD5930EB kit is shipped with a CD-ROM that includes self-installing software. The PC is connected to the evaluation board using the supplied cable. The software is compatible with Microsoft® Windows® 2000 and Windows XP.

A schematic of the evaluation board is shown in Figure 40 and Figure 41.

Using the AD5930 Evaluation Board

The AD5930 evaluation kit is a test system designed to simplify the evaluation of the AD5930. An application note is also available with the evaluation board and gives full information on operating the evaluation board.

Prototyping Area

An area is available on the evaluation board for the user to add additional circuits to the evaluation test set. Users may want to build custom analog filters for the output or add buffers and operational amplifiers to be used in the final application.

XO vs. External Clock

The AD5930 can operate with master clocks up to 50 MHz. A 50 MHz oscillator is included on the evaluation board. However, this oscillator can be removed and, if required, an external CMOS clock can be connected to the part.

SCHEMATIC

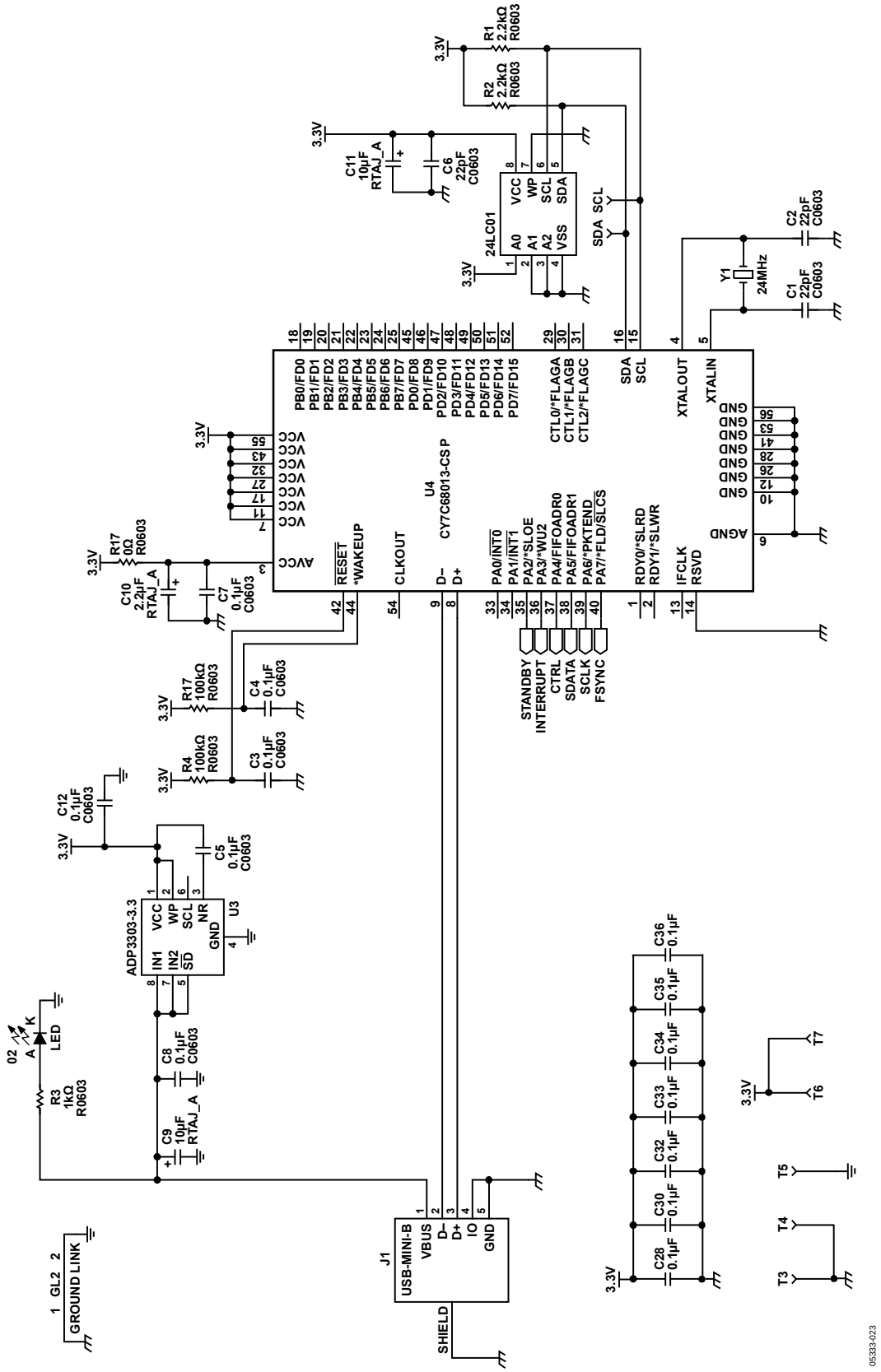

Figure 40. Page 1 of EVAL-AD5930EB Schematic

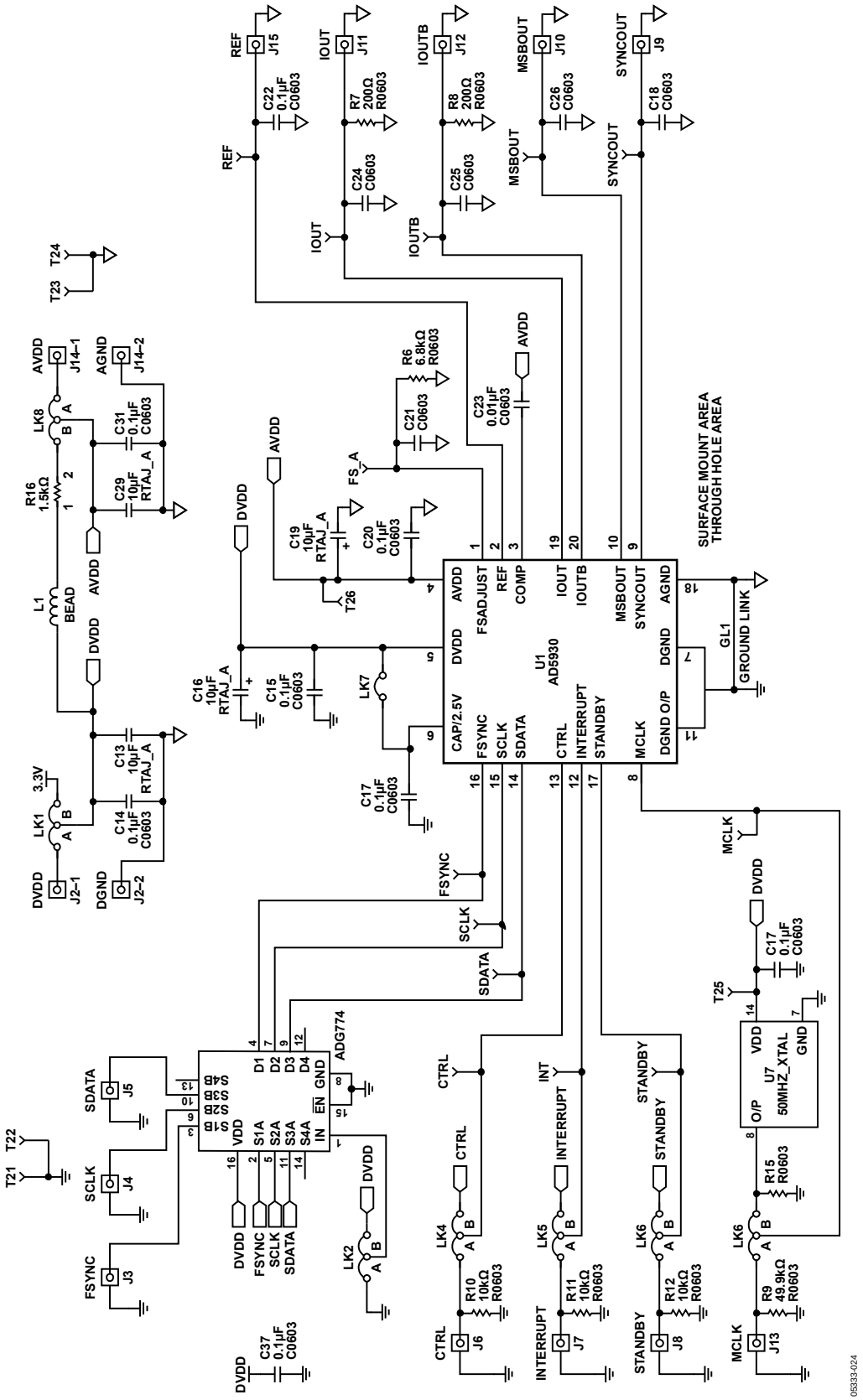

Figure 41. Page 2 of EVAL-AD5930EB Schematic

OUTLINE DIMENSIONS

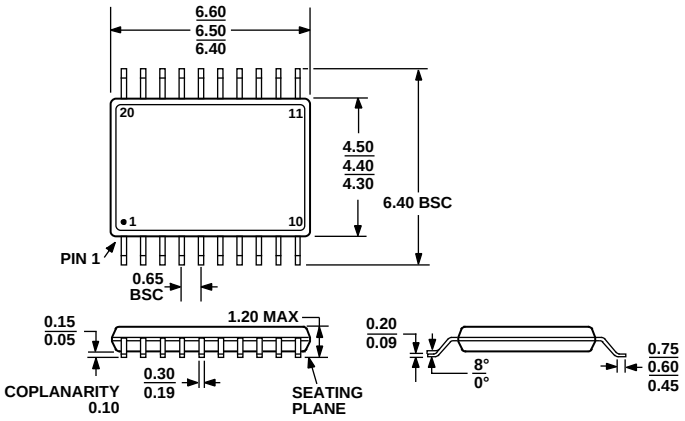

Figure 42. 20-Lead Thin Shrink Small Outline Package (TSSOP)
(RU-20)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD5930YRUZ	−40°C to +125°C	20-Lead Thin Shrink Small Outline Package [TSSOP]	RU-20
AD5930YRUZ-REEL7	−40°C to +125°C	20-Lead Thin Shrink Small Outline Package [TSSOP]	RU-20
EVAL-AD5930EBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

D05333-0-7/15(C)