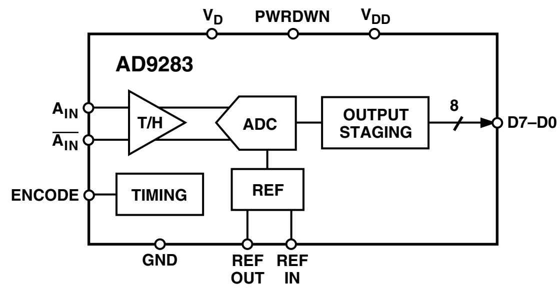
8-Bit, 50 MSPS/80 MSPS/100 MSPS 3 V A/D Converter

AD9283

FEATURES
- 8-Bit, 50, 80, and 100 MSPS ADC
- Low Power: 90 mW at 100 MSPS
- On-Chip Reference and Track/Hold
- 475 MHz Analog Bandwidth
- SNR = 46.5 dB @ 41 MHz at 100 MSPS
- 1 V p-p Analog Input Range
- Single 3.0 V Supply Operation (2.7 V–3.6 V)
- Power-Down Mode: 4.2 mW

APPLICATIONS
- Battery Powered Instruments
- Hand-Held Scopemeters
- Low Cost Digital Oscilloscopes

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9283 is an 8-bit monolithic sampling analog-to-digital converter with an on-chip track-and-hold circuit and is optimized for low cost, low power, small size and ease of use. The product operates at a 100 MSPS conversion rate, with outstanding dynamic performance over its full operating range.

The ADC requires only a single 3.0 V (2.7 V to 3.6 V) power supply and an encode clock for full performance operation. No external reference or driver components are required for many applications. The digital outputs are TTL/CMOS compatible and a separate output power supply pin supports interfacing with 3.3 V or 2.5 V logic.

The encoder input is TTL/CMOS compatible. A power-down function may be exercised to bring total consumption to 4.2 mW. In power-down mode, the digital outputs are driven to a high impedance state.

Fabricated on an advanced CMOS process, the AD9283 is available in a 20-lead surface mount plastic package (SSOP) specified over the industrial temperature range (–40°C to +85°C).

REV. C

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 www.analog.com
Fax: 781/326-8703

AD9283* Product Page Quick Links

Last Content Update: 11/01/2016

Comparable Parts

View a parametric search of comparable parts

Documentation

Application Notes

- AN-282: Fundamentals of Sampled Data Systems
- AN-302: Exploit Digital Advantages in an SSB Receiver
- AN-345: Grounding for Low-and-High-Frequency Circuits
- AN-501: Aperture Uncertainty and ADC System Performance
- AN-715: A First Approach to IBIS Models: What They Are and How They Are Generated
- AN-737: How ADIsimADC Models an ADC
- AN-741: Little Known Characteristics of Phase Noise
- AN-756: Sampled Systems and the Effects of Clock Phase Noise and Jitter
- AN-835: Understanding High Speed ADC Testing and Evaluation
- AN-905: Visual Analog Converter Evaluation Tool Version 1.0 User Manual
- AN-935: Designing an ADC Transformer-Coupled Front End

Data Sheet

- AD9283: 8-Bit, 50 MSPS/80 MSPS/100 MSPS 3 V A/D Converter Data Sheet

User Guides

- UG-173: High Speed ADC USB FIFO Evaluation Kit (HSC-ADC-EVALB-DCZ)

Tools and Simulations

- Visual Analog
- AD9283 IBIS Models

Reference Materials

Technical Articles

- Correlating High-Speed ADC Performance to Multicarrier 3G Requirements
- DNL and Some of its Effects on Converter Performance
- MS-2210: Designing Power Supplies for High Speed ADC

Design Resources

- AD9283 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

Discussions

View all AD9283 EngineerZone Discussions

Sample and Buy

Visit the product page to see pricing options

Technical Support

Submit a technical question or find your regional support number

AD9283–SPECIFICATIONS (V_{DD} = 3.0 V, V_D = 3.0 V; single-ended input; external reference, unless otherwise noted)

Parameter	Temp	Test Level	AD9283BRS-100 Min	AD9283BRS-100 Typ	AD9283BRS-100 Max	AD9283BRS-80 Min	AD9283BRS-80 Typ	AD9283BRS-80 Max	AD9283BRS-50 Min	AD9283BRS-50 Typ	AD9283BRS-50 Max	Unit
RESOLUTION				8			8			8		Bits
DC ACCURACY												
Differential Nonlinearity	25°C	I		±0.5	+1.25		±0.5	+1.25		±0.5	+1.25	LSB
	Full	VI			+1.50			+1.50			+1.50	LSB
Integral Nonlinearity	25°C	I	–1.25	±0.75	+1.25	–1.25	±0.75	+1.25	–1.25	±0.75	+1.25	LSB
	Full	VI			+2.25			+1.50			+1.50	LSB
No Missing Codes	Full	VI	Guaranteed			Guaranteed			Guaranteed			
Gain Error[1]	25°C	I	–6	±2.5	+6	–6	±2.5	+6	–6	±2.5	+6	% FS
	Full	VI	–8		+8	–8		+8	–8		+8	% FS
Gain Tempco[1]	Full	VI		80			80			80		ppm/°C
ANALOG INPUT												
Input Voltage Range (With Respect to A_{IN})	Full	V		±512			±512			±512		mV p-p
Common-Mode Voltage	Full	V		±200			±200			±200		mV
Input Offset Voltage	25°C	I	–35	±10	+35	–35	±10	+35	–35	±10	+35	mV
	Full	VI		±40			±40			±40		mV
Reference Voltage	Full	VI	1.2	1.25	1.3	1.2	1.25	1.3	1.2	1.25	1.3	V
Reference Tempco	Full	VI		±130			±130			±130		ppm/°C
Input Resistance	25°C	I	7	10	13	7	10	13	7	10	13	kΩ
	Full	VI	5		16	5		16	5		16	kΩ
Input Capacitance	25°C	V		2			2			2		pF
	Full	VI										µA
Analog Bandwidth, Full Power	25°C	V		475			475			475		MHz
SWITCHING PERFORMANCE												
Maximum Conversion Rate	Full	VI	100			80			50			MSPS
Minimum Conversion Rate	25°C	IV			1			1			1	MSPS
Encode Pulsewidth High (t_{EH})	25°C	IV	4.3		1000	5.0		1000	8.0		1000	ns
Encode Pulsewidth Low (t_{EL})	25°C	IV	4.3		1000	5.0		1000	8.0		1000	ns
Aperture Delay (t_A)	25°C	V		0			0			0		ns
Aperture Uncertainty (Jitter)	25°C	V		5			5			5		ps rms
Output Valid Time (t_V)[2]	Full	VI	2.0	3.0		2.0	3.0		2.0	3.0		ns
Output Propagation Delay (t_{PD})[2]	Full	VI		4.5	7.0		4.5	7.0		4.5	7.0	ns
DIGITAL INPUTS												
Logic "1" Voltage	Full	VI	2.0			2.0			2.0			V
Logic "0" Voltage	Full	VI			0.8			0.8		0.8		V
Logic "1" Current	Full	VI			±1			±1			±1	µA
Logic "0" Current	Full	VI			±1			±1			±1	µA
Input Capacitance	25°C	V		2.0			2.0			2.0		pF
DIGITAL OUTPUTS												
Logic "1" Voltage	Full	VI	2.95			2.95			2.95			V
Logic "0" Voltage	Full	VI			0.05			0.05			0.05	V
Output Coding			Offset Binary Code			Offset Binary Code			Offset Binary Code			
POWER SUPPLY												
Power Dissipation[3, 4]	Full	VI		90	120		90	115		80	100	mW
Power-Down Dissipation	Full	VI		4.2	7		4.2	7		4.2	7	mW
Power Supply Rejection Ratio (PSRR)	25°C	I			18			18			18	mV/V

Parameter	Temp	Test Level	AD9283BRS-100 Min	Typ	Max	AD9283BRS-80 Min	Typ	Max	AD9283BRS-50 Min	Typ	Max	Unit
DYNAMIC PERFORMANCE[5]												
Transient Response	25°C	V		2			2			2		ns
Overvoltage Recovery Time	25°C	V		2			2			2		ns
Signal-to-Noise Ratio (SNR) (Without Harmonics)												
f_{IN} = 10.3 MHz	25°C	I		46.5			47		44	47		dB
f_{IN} = 27 MHz	25°C	I		46.5		44	47			47		dB
f_{IN} = 41 MHz	25°C	I	43.5	46.5			47					dB
f_{IN} = 76 MHz	25°C	V		46.0								dB
Signal-to-Noise Ratio (SINAD) (With Harmonics)												
f_{IN} = 10.3 MHz	25°C	I		45			47		43.5	46.5		dB
f_{IN} = 27 MHz	25°C	I		45.5		43.5	46.5			46		dB
f_{IN} = 41 MHz	25°C	I	42.5	45			42					dB
f_{IN} = 76 MHz	25°C	V		42.5								dB
Effective Number of Bits												
f_{IN} = 10.3 MHz	25°C	I		7.3			7.5			7.6		Bits
f_{IN} = 27 MHz	25°C	I		7.4			7.5			7.5		Bits
f_{IN} = 41 MHz	25°C	I		7.3			7.5					Bits
f_{IN} = 76 MHz	25°C	V		6.9								Bits
2nd Harmonic Distortion												
f_{IN} = 10.3 MHz	25°C	I		57			60		55	60		dBc
f_{IN} = 27 MHz	25°C	I		60		55	60			56		dBc
f_{IN} = 41 MHz	25°C	I	50	58			55					dBc
f_{IN} = 76 MHz	25°C	V		46								dBc
3rd Harmonic Distortion												
f_{IN} = 10.3 MHz	25°C	I		54.5			70		55	70		dBc
f_{IN} = 27 MHz	25°C	I		55		55	62.5			60		dBc
f_{IN} = 41 MHz	25°C	I	47	52.5			60					dBc
f_{IN} = 76 MHz	25°C	V		53								dBc
Two-Tone Intermod Distortion (IMD)												
f_{IN} = 10.3 MHz	25°C	V		52			52			52		dBc

NOTES

[1]Gain error and gain temperature coefficient are based on the ADC only (with a fixed 1.25 V external reference).

[2]t_V and t_{PD} are measured from the 1.5 V level of the ENCODE input to the 50%/50% levels of the digital outputs swing. The digital output load during test is not to exceed an ac load of 10 pF or a dc current of ±40 µA.

[3]Power dissipation measured with encode at rated speed and a dc analog input.

[4]Typical thermal impedance for the RS style (SSOP) 20-lead package: θ_{JC} = 46°C/W, θ_{CA} = 80°C/W, θ_{JA} = 126°C/W.

[5]SNR/harmonics based on an analog input voltage of –0.7 dBFS referenced to a 1.024 V full-scale input range.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_D, V_{DD} . . . . 4 V
Analog Inputs . . . . –0.5 V to V_D + 0.5 V
Digital Inputs . . . . –0.5 V to V_{DD} + 0.5 V
VREF IN . . . . –0.5 V to V_D + 0.5 V
Digital Output Current . . . . 20 mA
Operating Temperature . . . . –55°C to +125°C
Storage Temperature . . . . –65°C to +150°C
Maximum Junction Temperature . . . . 150°C
Maximum Case Temperature . . . . 150°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Ranges	Package Descriptions	Package Options
AD9283BRS -50, -80, -100	–40°C to +85°C	20-Lead SSOP	RS-20
AD9283/PCB	25°C	Evaluation Board	

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9283 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

EXPLANATION OF TEST LEVELS

Test Level

I 100% production tested.

II 100% production tested at 25°C and sample tested at specified temperatures.

III Sample tested only.

IV Parameter is guaranteed by design and characterization testing.

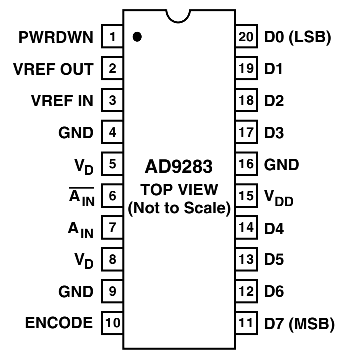
V Parameter is a typical value only.

VI 100% production tested at 25°C; guaranteed by design and characterization testing for industrial temperature range; 100% production tested at temperature extremes for military devices.

Table I. Output Coding (VREF = 1.25 V)

Step	$A_{IN}-\overline{A_{IN}}$	Digital Output
255	0.512	1111 1111
•	•	•
•	•	•
128	0.002	1000 0000
127	–0.002	0111 1111
•	•	•
•	•	•
0	–0.512	0000 0000

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin Number	Mnemonic	Function
1	PWRDWN	Power-Down Function Select; Logic HIGH for Power-Down Mode (Digital Outputs Go to High Impedance State)
2	VREF OUT	Internal Reference Output (1.25 V typ); Bypass with 0.1 µF to Ground
3	VREF IN	Reference Input for ADC (1.25 V typ)
4, 9, 16	GND	Ground
5, 8	V_D	Analog 3 V Power Supply
6	$\overline{A_{IN}}$	Analog Input for ADC (Can Be Left Open if Operating in Single-Ended Mode, but Recommend Connection to a 0.1 µF Capacitor and a 25 Ω Resistor in Series to Ground for Better Input Matching)
7	A_{IN}	Analog Input for ADC
10	ENCODE	Encode Clock for ADC (ADC Samples on Rising Edge of ENCODE)
11–14, 17–20	D7–D4, D3–D0	Digital Outputs of ADC
15	V_{DD}	Digital output power supply. Nominally 2.5 V to 3.6 V

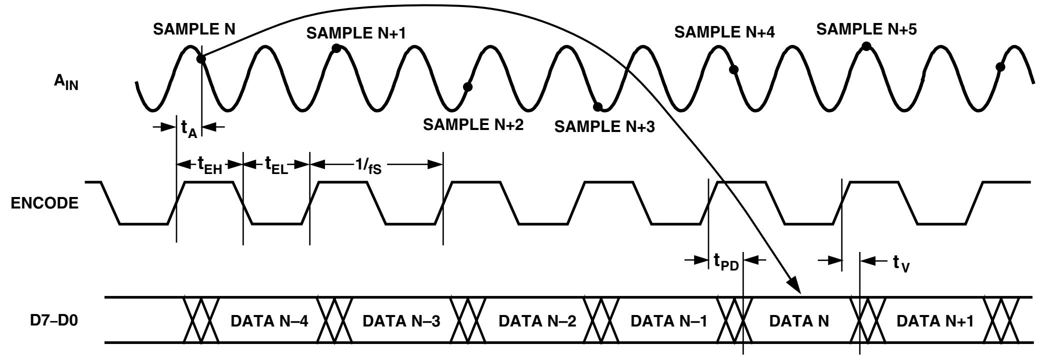


Figure 1. Timing Diagram

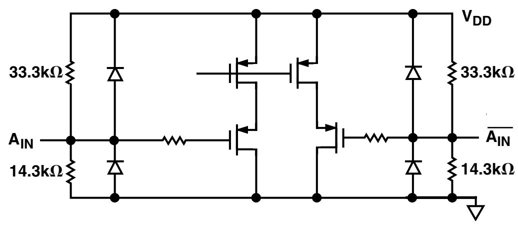


Figure 2. Equivalent Analog Input Circuit

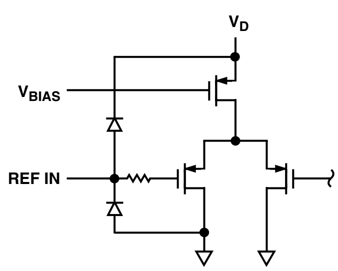


Figure 3. Equivalent Reference Input Circuit

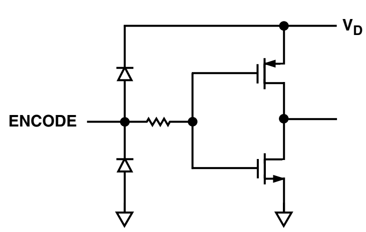


Figure 4. Equivalent Encode Input Circuit

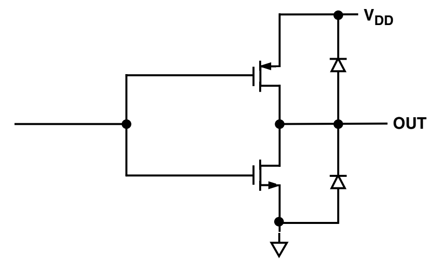


Figure 5. Equivalent Digital Output Circuit

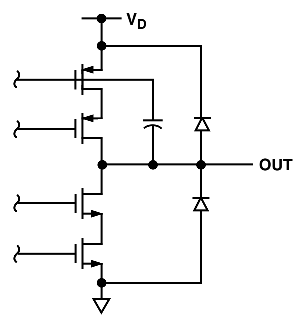
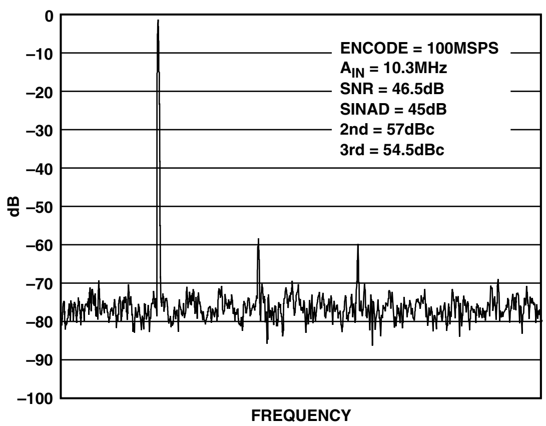
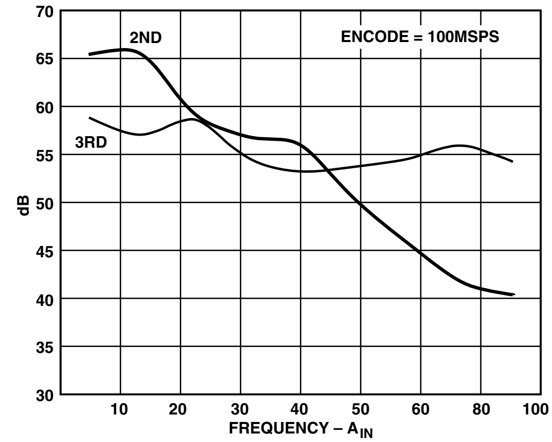


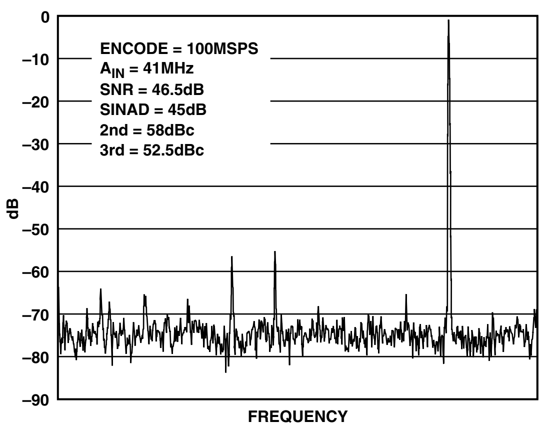
Figure 6. Equivalent Reference Output Circuit



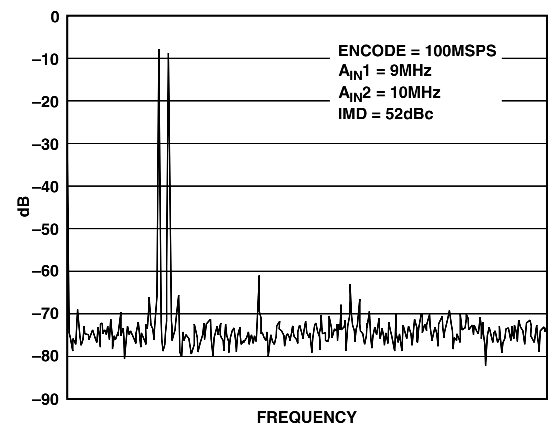
TPC 1. Spectrum: f_S = 100 MSPS, f_{IN} = 10.3 MHz



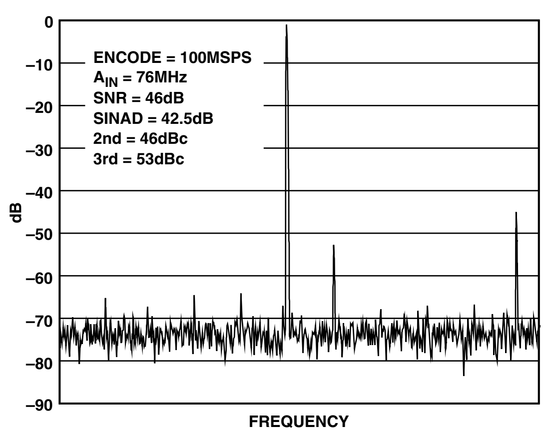
TPC 4. Harmonic Distortion vs. A_{IN} Frequency



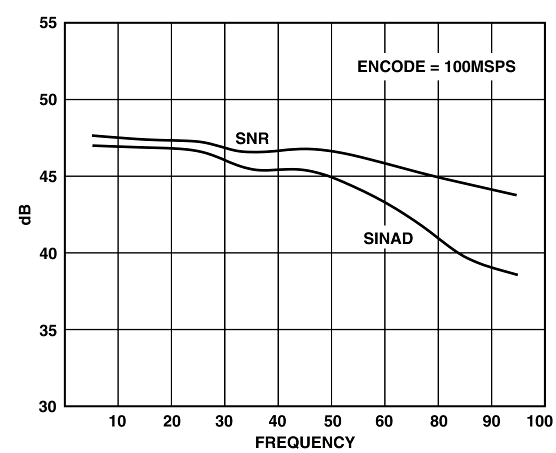
TPC 2. Spectrum: f_S = 100 MSPS, f_{IN} = 40 MHz



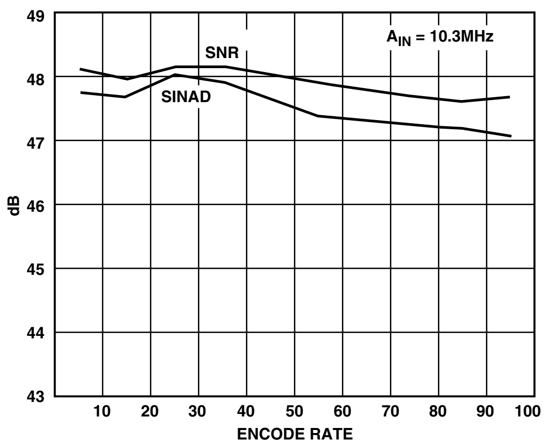
TPC 5. Two-Tone Intermodulation Distortion



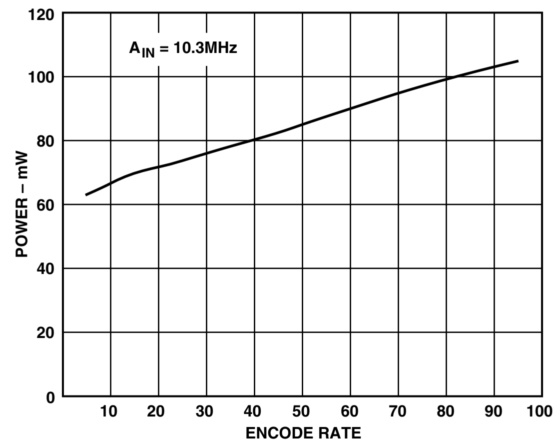
TPC 3. Spectrum: f_S = 100 MSPS, f_{IN} = 76 MHz



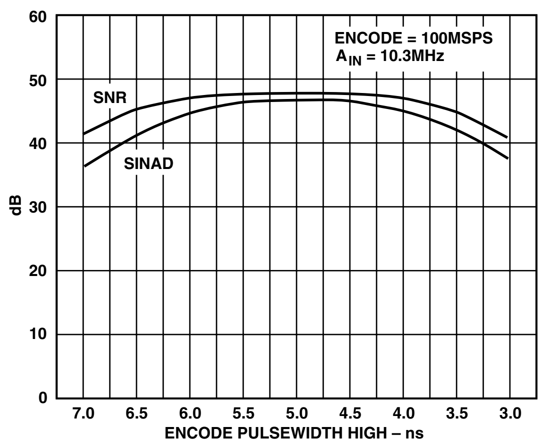
TPC 6. SINAD/SNR vs. A_{IN} Frequency



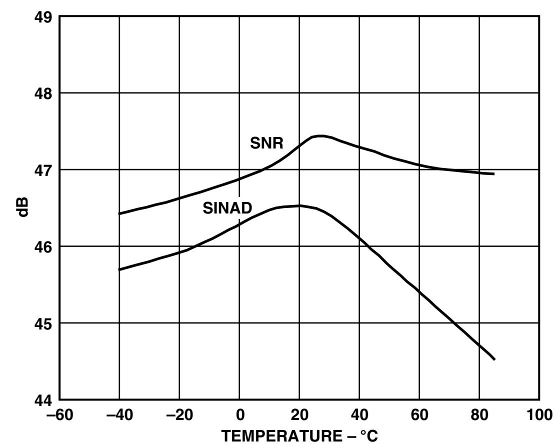
TPC 7. SINAD/SNR vs. Encode Rate



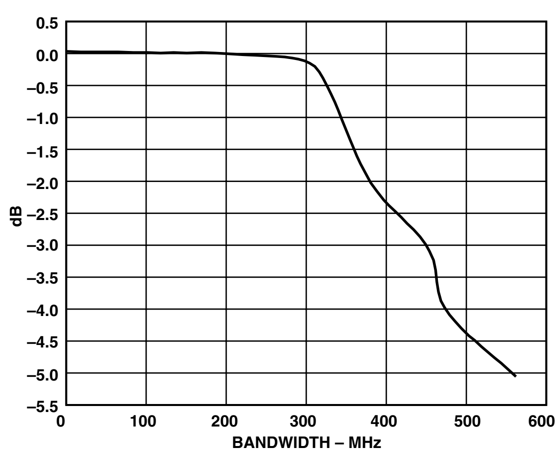
TPC 10. Analog Power Dissipation vs. Encode Rate



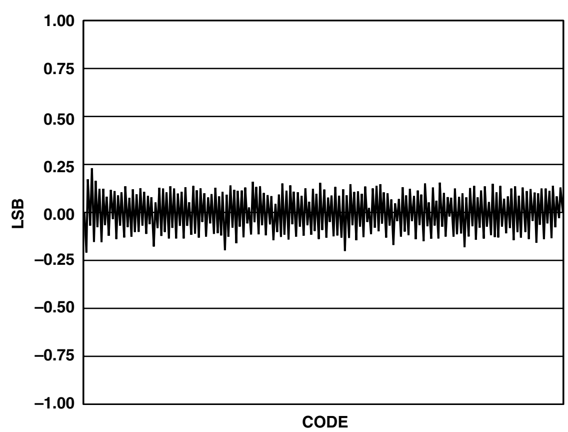
TPC 8. SINAD/SNR vs. Encode Pulsewidth High



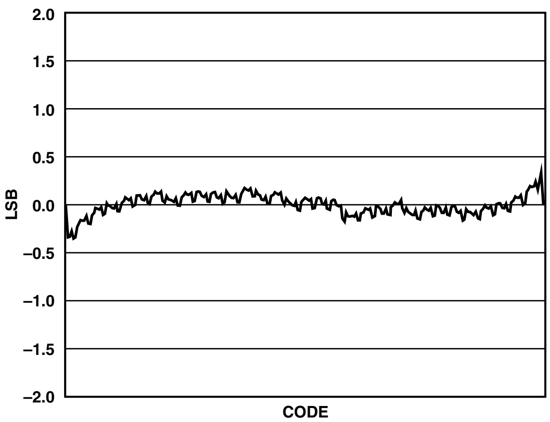
TPC 11. SINAD/SNR vs. Temperature



TPC 9. ADC Frequency Response: f_S = 100 MSPS



TPC 12. Differential Nonlinearity



TPC 13. Integral Nonlinearity

APPLICATIONS

Theory of Operation

The analog signal is applied differentially or single-endedly to the inputs of the AD9283. The signal is buffered and fed forward to an on-chip sample-and-hold circuit. The ADC core architecture is a bit-per-stage pipeline type converter utilizing switch capacitor techniques. The bit-per-stage blocks determine the 5 MSBs and drive a FLASH converter to encode the 3 LSBs. Each of the 5 MSB stages provides sufficient overlap and error correction to allow optimization of performance with respect to comparator accuracy. The output staging block aligns the data, carries out the error correction and feeds the data to the eight output buffers. The AD9283 includes an on-chip reference (nominally 1.25 V) and generates all clocking signals from one externally applied encode command. This makes the ADC easy to interface with and requires very few external components for operation.

ENCODE Input

The ENCODE input is fully TTL/CMOS compatible with a nominal threshold of 1.5 V. Care was taken on the chip to match clock line delays and maintain sharp clock logic transitions. Any high speed A/D converter is extremely sensitive to the quality of the sampling clock provided by the user. This ADC uses an on-chip sample-and-hold circuit which is essentially a mixer. Any timing jitter on the ENCODE will be combined with the desired signal and degrade the high frequency performance of the ADC. The user is advised to give commensurate thought to the clock source.

Analog Input

The analog input to the ADC is fully differential and both inputs are internally biased. This allows the most flexible use of ac or dc and differential or single-ended input modes. For peak performance the inputs are biased at $0.3 \times V_D$. See the specification table for allowable common-mode range when dc coupling the input. The inputs are also buffered to reduce the load the user needs to drive. For best dynamic performance, the impedances at A_{IN} and $\overline{A_{IN}}$ should be matched. The importance of this increases with sampling rate and analog input frequency. The nominal input range is 1.024 V p-p.

Digital Outputs

The digital outputs are TTL/CMOS compatible. The output buffers are powered from a separate supply, allowing adjustment of the output voltage swing to ease interfacing with 2.5 V or 3.3 V logic. The AD9283 goes into a low power state within two clock cycles following the assertion of the PWRDWN input. PWRDWN is asserted with a logic high. During power-down the outputs transition to a high impedance state. The time it takes to achieve optimal performance after disabling the power-down mode is approximately 15 clock cycles. Care should be taken when loading the digital outputs of any high speed ADC. Large output loads create current transients on the chip that can degrade the converter's performance.

Voltage Reference

A stable and accurate 1.25 V voltage reference is built into the AD9283 (VREF OUT). In normal operation, the internal reference is used by strapping Pins 2 and 3 of the AD9283 together. The input range can be adjusted by varying the reference voltage applied to the AD9283. No degradation in performance occurs when the reference is adjusted ±5%. The full-scale range of the ADC tracks reference voltage changes linearly. Whether used or not, the internal reference (Pin 2) should be bypassed with a 0.1 µF capacitor to ground.

Timing

The AD9283 provides latched data outputs with four pipeline delays. Data outputs are available one propagation delay (t_{PD}) after the rising edge of the encode command (Figure 1. Timing Diagram). The minimum guaranteed conversion rate to the ADC is 1 MSPS. The dynamic performance of the converter will degrade at encode rates below this sample rate.

Evaluation Board

The AD9283 evaluation board offers an easy way to test the AD9283. It only requires a 3 V supply, an analog input and encode clock to test the AD9283. The board is shipped with the 100 MSPS grade ADC.

The analog input to the board accepts a 1 V p-p signal centered at ground. J1 should be used (Jump E3–E4, E18–E19) to drive the ADC through Transformer T1. J2 should be used for single-ended input drive (Jump E19–E21).

Both J1 and J2 are terminated to 50 Ω on the PCB. Each analog path is ac-coupled to an on-chip resistor divider which provides the required dc bias.

A (TTL/CMOS Level) sample clock is applied to connector J3 which is terminated through 50 Ω on the PCB. This clock is buffered by U5 which also provides the clocks for the 574 latches, DAC, and the off-card latch clock CLKCON. (Timing can be modified at E17.)

There is a reconstruction DAC (AD9760) on the PCB. The DAC is on the board to assist in debug only—the outputs should not be used to measure performance of the ADC.

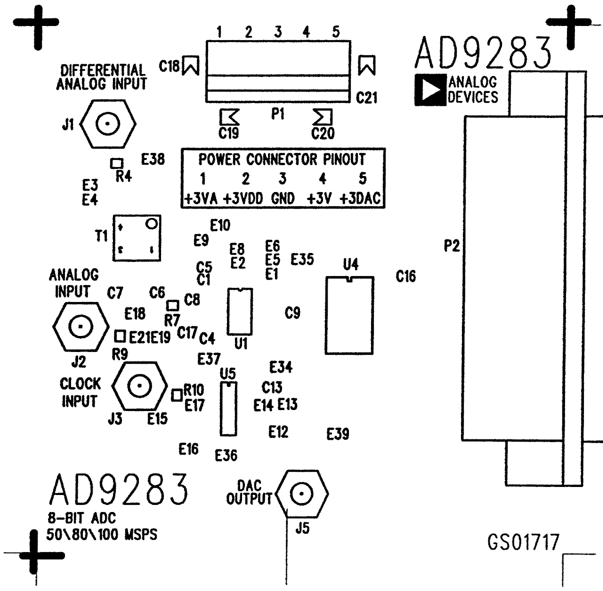


Figure 7. Printed Circuit Board Top Side Silkscreen

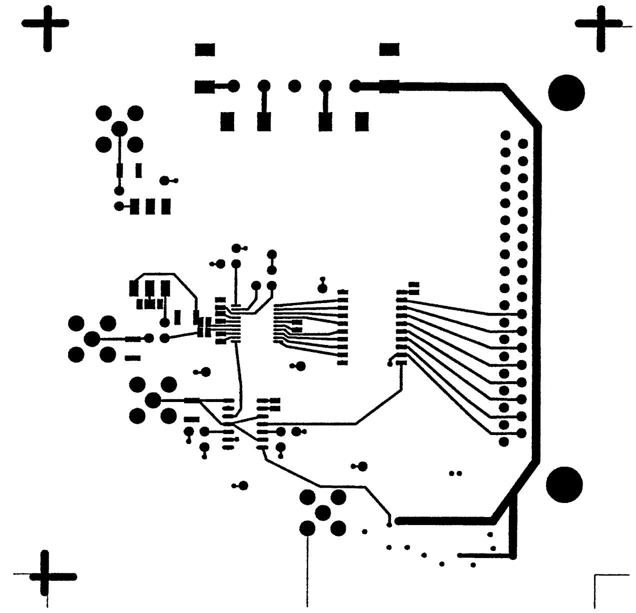


Figure 9. Printed Circuit Board Top Side Copper

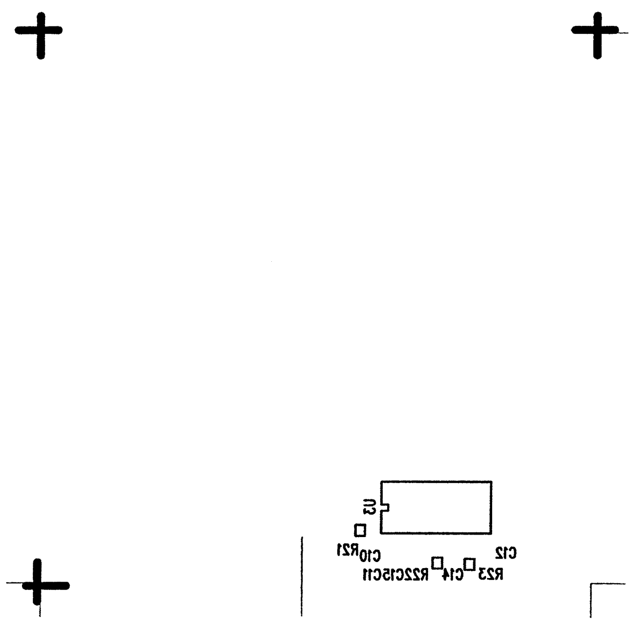


Figure 8. Printed Circuit Board Bottom Side Silkscreen

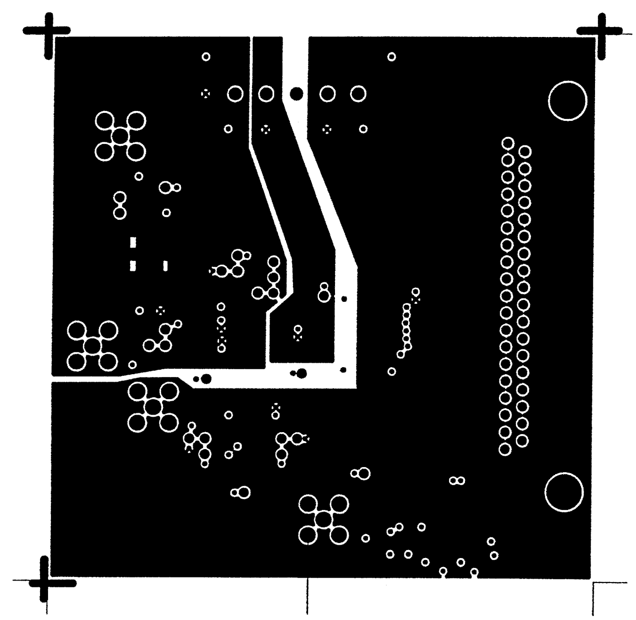


Figure 10. Printed Circuit Board "Split" Power Layer

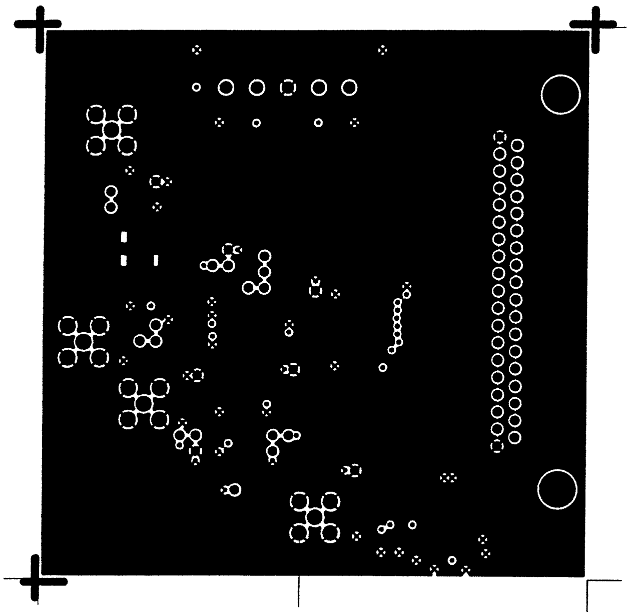


Figure 11. Printed Circuit Board Ground Layer

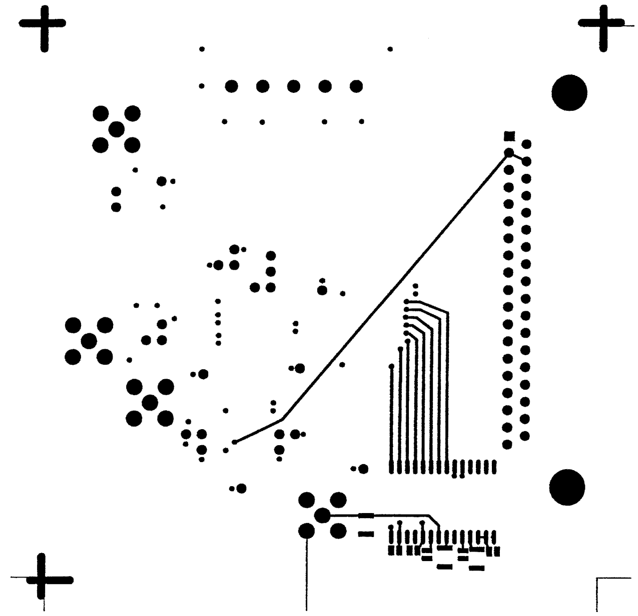


Figure 12. Printed Circuit Board Bottom Side Copper

EVALUATION BOARD BILL OF MATERIALS — GS01717

#	Qty	REFDES	Device	Package	Value
1	15	C1, C4–C17	Ceramic Cap	0603	0.1 µF
2	4	C18–C21	Tantalum Cap	BCAPTAJD	10 µF
3	24	E1–E6, E8–E10, E12–E19, E21, E34–E39	W-HOLE		
4	4	J1, J2, J3, J5	Connector	SMB	
5	1	P1	5-Pin Connector		Wieland Connector (P/N #25.602.2553.0 Top P/N #Z5.530.0525.0 Bottom)
6	1	P2	37-Pin Connector		AMP-747462-2
7	5	R4, R9, R10, R21, R22	Resistor	1206	50 Ω
8	1	R7	Resistor	1206	25 Ω
9	1	R23	Resistor	1206	2 kΩ
10	1	T1	Transformer		Mini-Circuits T1-1T-KK81
11	1	U1	AD9283	SSOP-20	
12	1	U3	AD9760	SOIC-28	
13	1	U4	74ACQ574	SOIC-20	
14	1	U5	SN74LVC86	SO14	

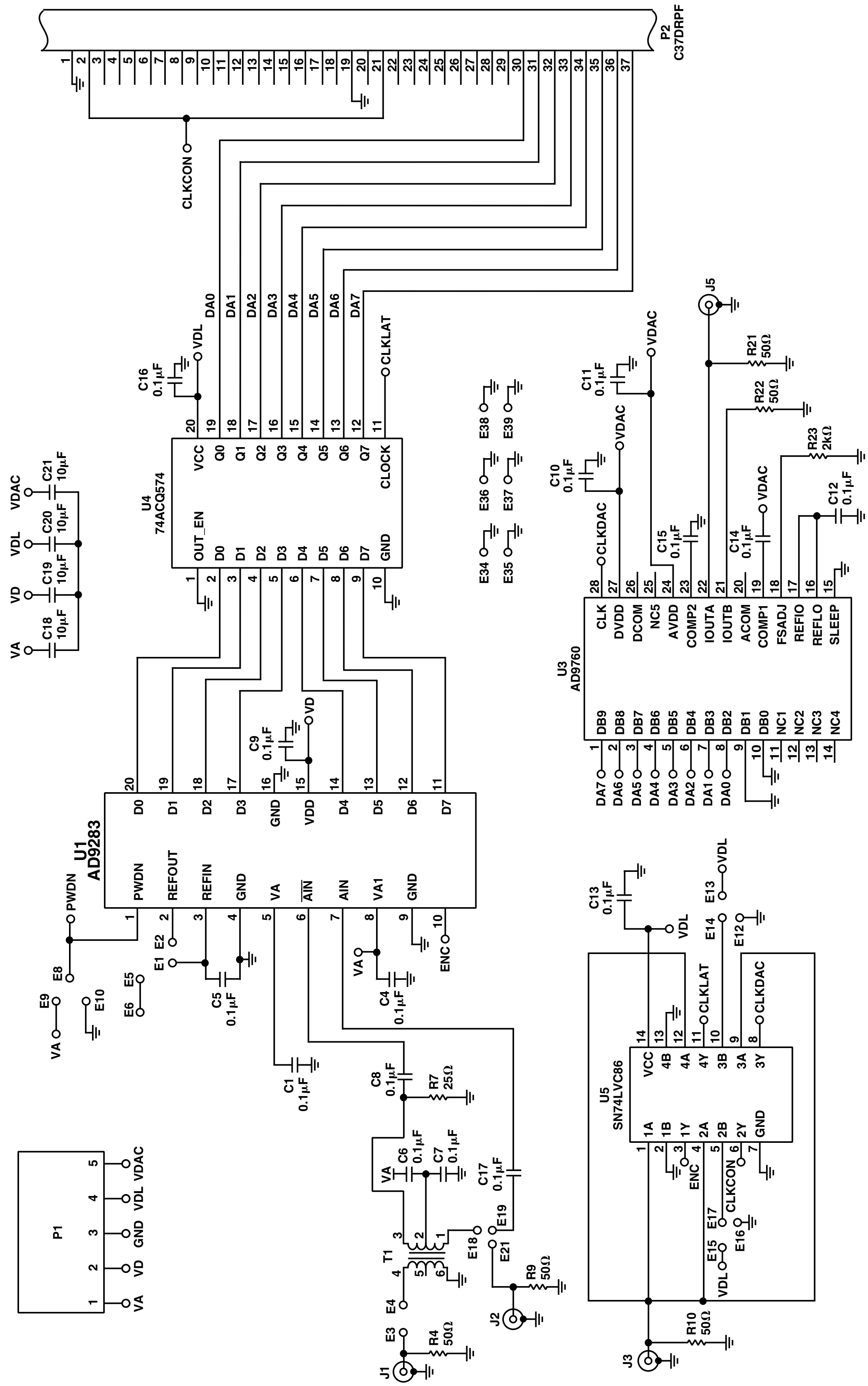
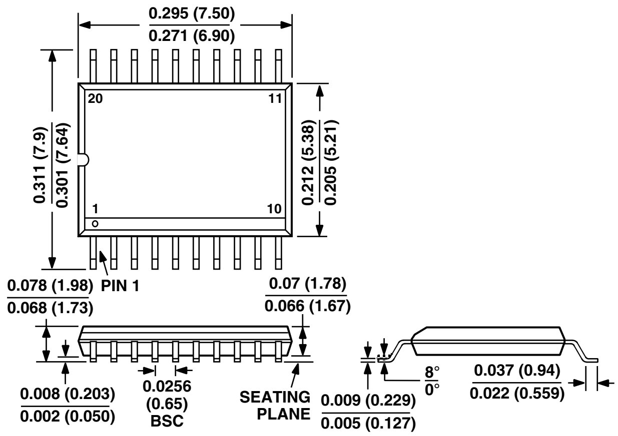


Figure 13. Printed Circuit Board Schematic

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

20-Lead Shrink Small Outline Package (SSOP)
(RS-20)



Revision History

Location	Page
Data Sheet changed from REV. B to REV. C.	
Edits to ABSOLUTE MAXIMUM RATINGS	3

C00584b–0–10/01(C)

PRINTED IN U.S.A.