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# FPF1005-FPF1006 IntelliMAX™ Advanced Load Management Products

## Features

- 1.2 to 5.5V Input Voltage Range
- Typical  $R_{DS(ON)} = 50m\Omega @ V_{IN} = 5.5V$
- Typical  $R_{DS(ON)} = 55m\Omega @ V_{IN} = 3.3V$
- ESD Protected, above 2000V HBM

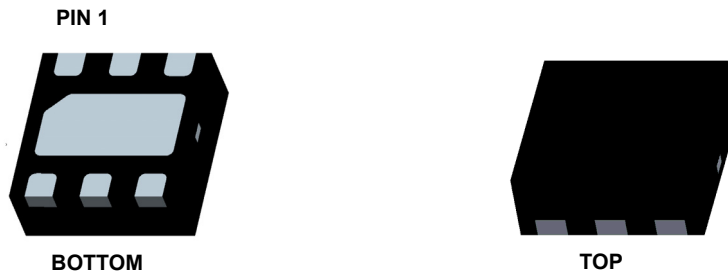
## Applications

- PDAs
- Cell Phones
- GPS Devices
- MP3 Players
- Digital Cameras
- Peripheral Ports
- Hot Swap Supplies
- RoHS Compliant

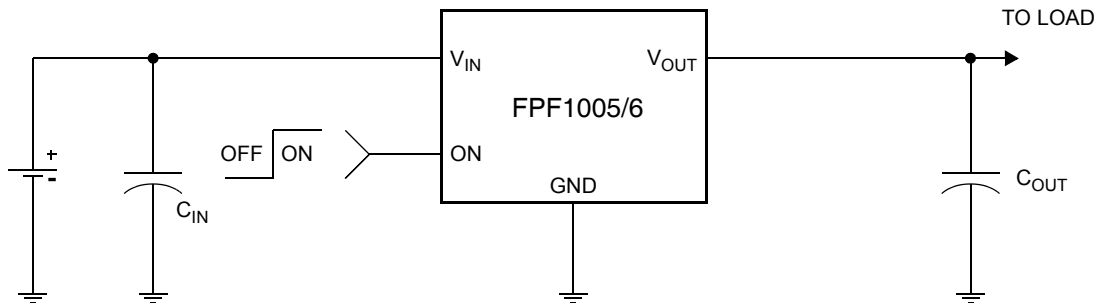
## General Description

The FPF1005 & FPF1006 are low  $R_{DS}$  P-Channel MOSFET load switches with CMOS controlled turn-on targeting small package load switch applications. The input voltage range operates from 1.2V to 5.5V. Switch control is by a logic input (ON) capable of interfacing directly with low voltage control signals. In FPF1006, 120 $\Omega$  on-chip load resistor is added for output quick discharge when switch is turned off.

Both FPF1005 & FPF1006 are available in a small 2X2 MicroFET-6 pin plastic package.



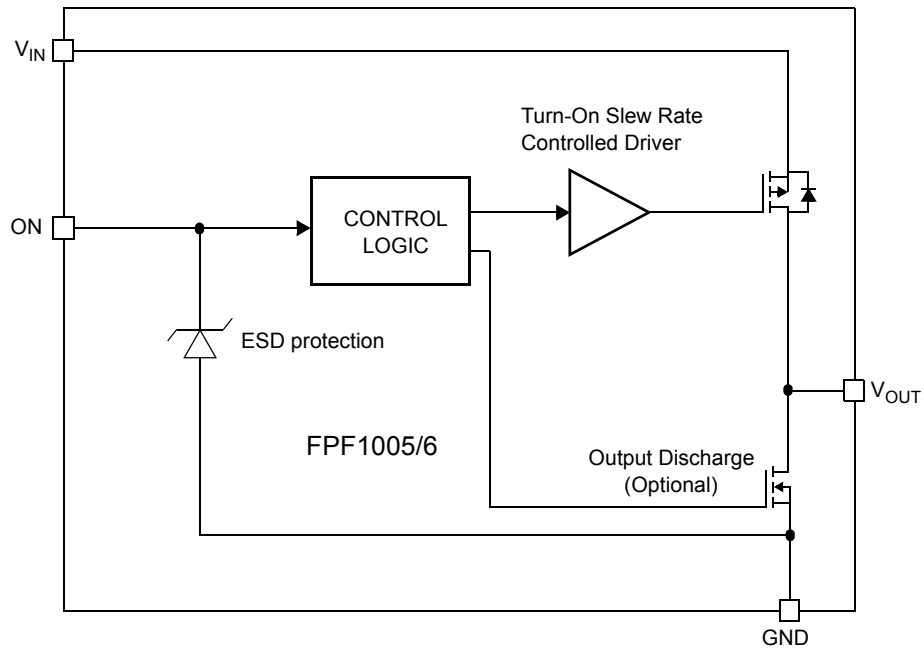
## Typical Application Circuit



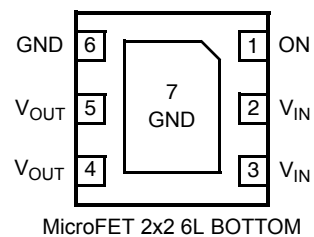
## Ordering Information

Part	Switch	Input Buffer	Output Discharge	ON Pin Activity
FPF1005	55m $\Omega$ , PMOS	Schmitt	NA	Active HI
FPF1006	55m $\Omega$ , PMOS	Schmitt	120 $\Omega$	Active HI

## Functional Block Diagram



## Pin Configuration



## Pin Description

Pin	Name	Function
4, 5	$V_{OUT}$	Switch Output: Output of the power switch
2, 3	$V_{IN}$	Supply Input: Input to the power switch and the supply voltage for the IC
6, 7	GND	Ground
1	ON	ON/OFF Control Input

## Absolute Maximum Ratings

Parameter	Min	Max	Unit
$V_{IN}$ , $V_{OUT}$ , ON to GND	-0.3	6	V
Maximum Continuous Switch Current		1.5	A
Power Dissipation @ $T_A = 25^\circ\text{C}$ (Note 1)		1.2	W
Operating Temperature Range	-40	85	$^\circ\text{C}$
Storage Temperature	-65	150	$^\circ\text{C}$
Thermal Resistance, Junction to Ambient		86	$^\circ\text{C/W}$
Electrostatic Discharge Protection	HBM	2000	V
	MM	200	V

## Recommended Operating Range

Parameter	Min	Max	Unit
$V_{IN}$	1.2	5.5	V
Ambient Operating Temperature, $T_A$	-40	85	$^\circ\text{C}$

## Electrical Characteristics

$V_{IN} = 1.2$  to  $5.5\text{V}$ ,  $T_A = -40$  to  $+85^\circ\text{C}$  unless otherwise noted. Typical values are at  $V_{IN} = 3.3\text{V}$  and  $T_A = 25^\circ\text{C}$ .

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>Basic Operation</b>						
Operating Voltage	$V_{IN}$		1.2		5.5	V
Quiescent Current	$I_Q$	$I_{OUT} = 0\text{mA}$ , $V_{IN} = V_{ON}$			1	$\mu\text{A}$
Off Supply Current	$I_{Q(off)}$	$V_{ON} = \text{GND}$ , $\text{OUT} = \text{open}$			1	$\mu\text{A}$
Off Switch Current	$I_{SD(off)}$	$V_{ON} = \text{GND}$ , $V_{OUT} = 0\text{V}$ @ $V_{IN} = 5.5\text{V}$ , $T_A = 85^\circ\text{C}$			1	$\mu\text{A}$
		$V_{ON} = \text{GND}$ , $V_{OUT} = 0\text{V}$ @ $V_{IN} = 3.3\text{V}$ , $T_A = 25^\circ\text{C}$		10	100	nA
On-Resistance	$R_{ON}$	$V_{IN} = 5.5\text{V}$ , $T_A = 25^\circ\text{C}$		50	70	m $\Omega$
		$V_{IN} = 3.3\text{V}$ , $T_A = 25^\circ\text{C}$		55	80	
		$V_{IN} = 1.5\text{V}$ , $T_A = 25^\circ\text{C}$		95	135	
		$V_{IN} = 1.2\text{V}$ , $T_A = 25^\circ\text{C}$		165	250	
Output Pull Down Resistance	$R_{PD}$	$V_{IN} = 3.3\text{V}$ , $V_{ON} = 0\text{V}$ , $T_A = 25^\circ\text{C}$ , FPF1006		75	120	$\Omega$
ON Input Logic Low Voltage	$V_{IL}$	$V_{IN} = 5.5\text{V}$			1.25	V
		$V_{IN} = 4.5\text{V}$			1.10	
		$V_{IN} = 1.5\text{V}$			0.50	
ON Input Logic High Voltage	$V_{IH}$	$V_{IN} = 5.5\text{V}$	2.00			V
		$V_{IN} = 4.5\text{V}$	1.75			
		$V_{IN} = 1.5\text{V}$	0.75			
ON Input Leakage		$V_{ON} = V_{IN}$ or GND	-1		1	$\mu\text{A}$
<b>Dynamic</b>						
Turn on delay	$t_{ON}$	$V_{IN} = 3.3\text{V}$ , $R_L = 500\Omega$ , $C_L = 0.1\mu\text{F}$ , $T_A = 25^\circ\text{C}$		10		$\mu\text{s}$
Turn off delay	$t_{OFF}$	$V_{IN} = 3.3\text{V}$ , $R_L = 500\Omega$ , $C_L = 0.1\mu\text{F}$ , $T_A = 25^\circ\text{C}$ , FPF1005		50		$\mu\text{s}$
		$V_{IN} = 3.3\text{V}$ , $R_L = 500\Omega$ , $C_L = 0.1\mu\text{F}$ , $R_{L\_CHIP} = 120\Omega$ , $T_A = 25^\circ\text{C}$ , FPF1006		10		$\mu\text{s}$
$V_{OUT}$ Rise Time	$t_R$	$V_{IN} = 3.3\text{V}$ , $R_L = 500\Omega$ , $C_L = 0.1\mu\text{F}$ , $T_A = 25^\circ\text{C}$		10		$\mu\text{s}$
$V_{OUT}$ Fall Time	$t_F$	$V_{IN} = 3.3\text{V}$ , $R_L = 500\Omega$ , $C_L = 0.1\mu\text{F}$ , $T_A = 25^\circ\text{C}$ , FPF1005		100		$\mu\text{s}$
		$V_{IN} = 3.3\text{V}$ , $R_L = 500\Omega$ , $C_L = 0.1\mu\text{F}$ , $R_{L\_CHIP} = 120\Omega$ , $T_A = 25^\circ\text{C}$ , FPF1006		10		$\mu\text{s}$

**Note 1:** Package power dissipation on 1square inch pad, 2 oz. copper board

### Typical Characteristics

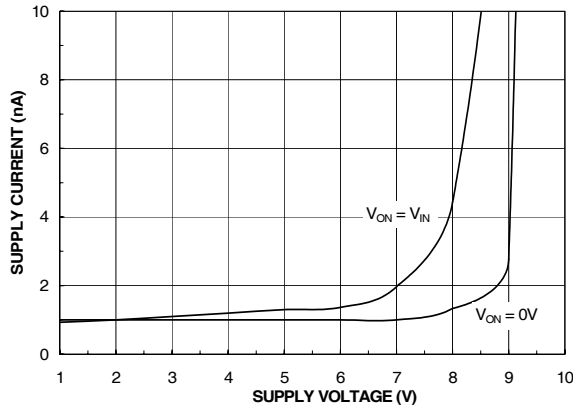


Figure 1. Quiescent Current vs.  $V_{IN}$

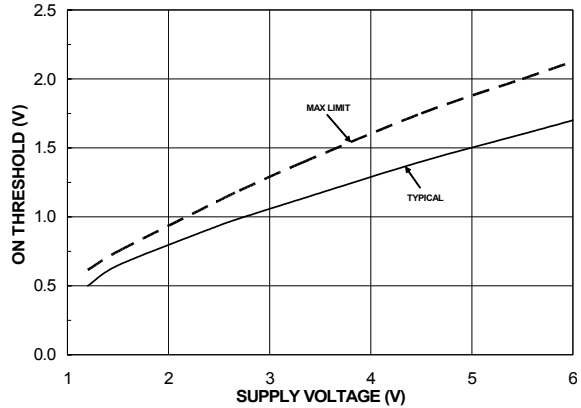


Figure 2. ON Threshold vs.  $V_{IN}$

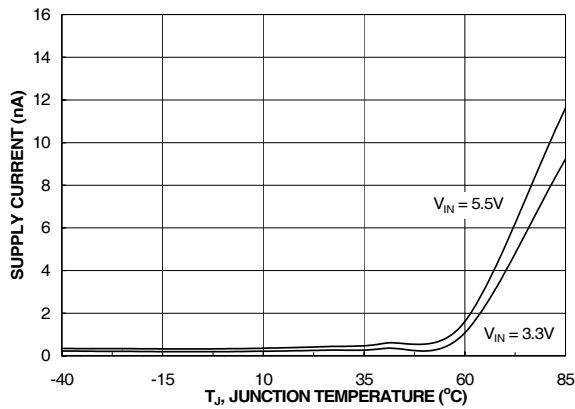


Figure 3. Quiescent Current vs. Temperature

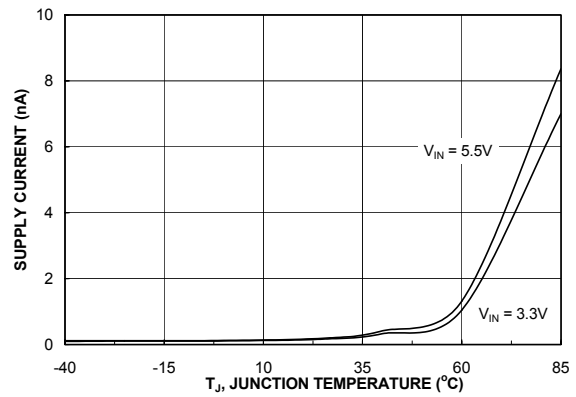


Figure 4. Quiescent Current (off) vs. Temperature

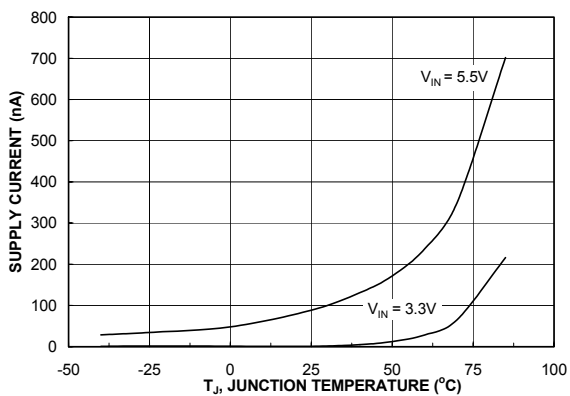


Figure 5.  $I_{\text{SWITCH-OFF}}$  Current vs. Temperature

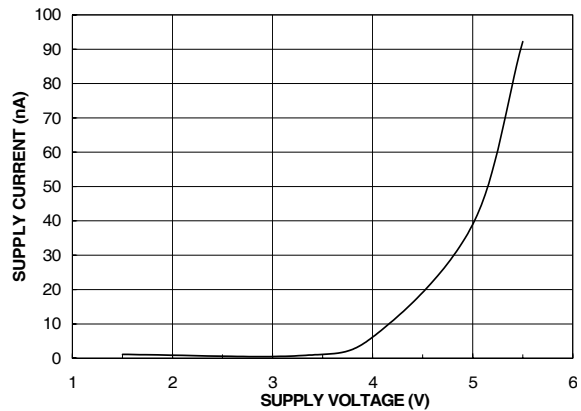


Figure 6.  $I_{\text{SWITCH-OFF}}$  Current vs.  $V_{IN}$

## Typical Characteristics

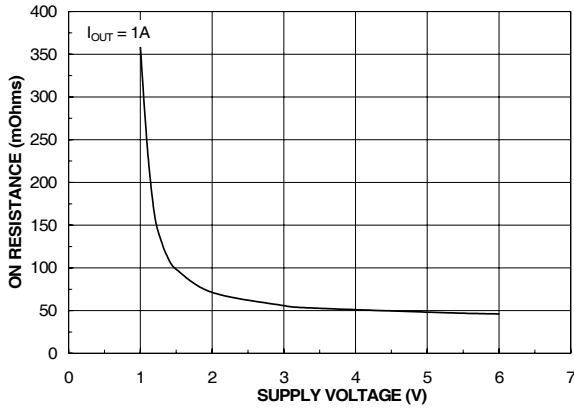


Figure 7.  $R_{ON}$  vs.  $V_{IN}$

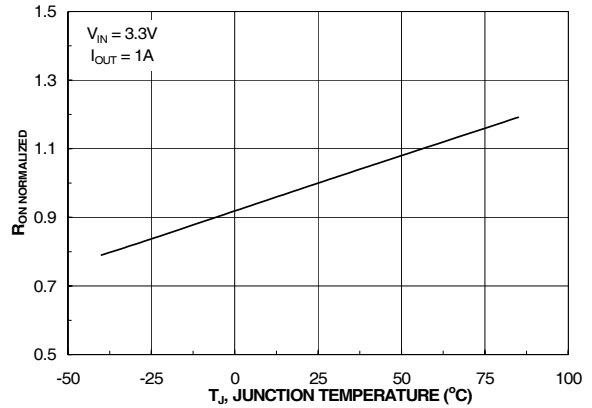


Figure 8.  $R_{ON}$  vs. Temperature

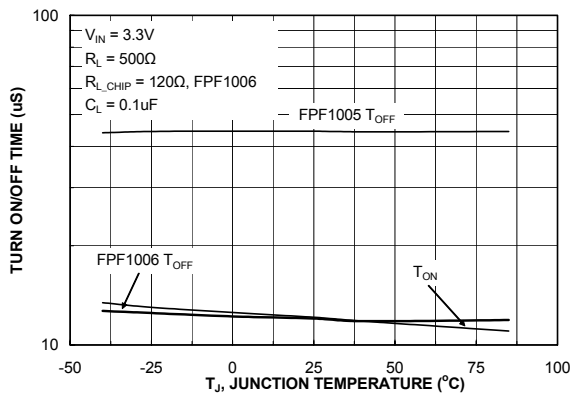


Figure 9.  $T_{ON}/T_{OFF}$  vs. Temperature

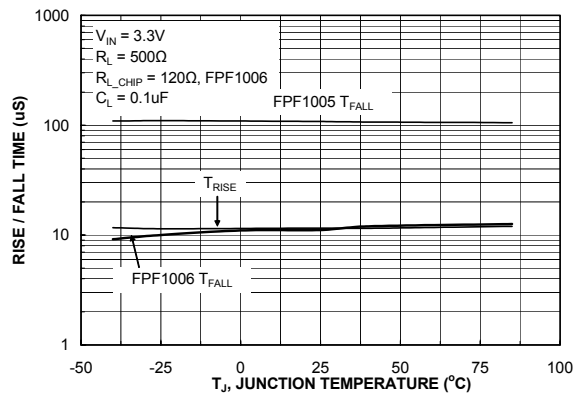


Figure 10.  $T_{RISE}/T_{FALL}$  vs. Temperature

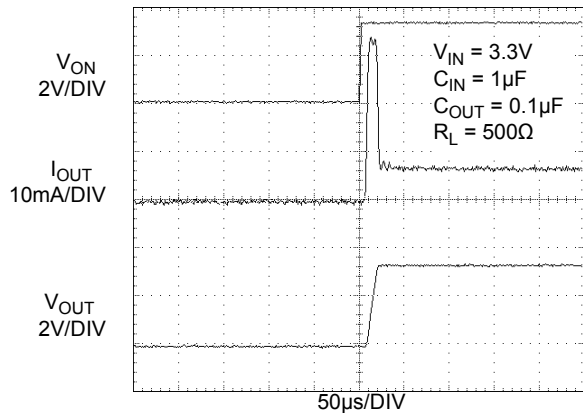


Figure 11. FPF1005  $T_{ON}$  Response

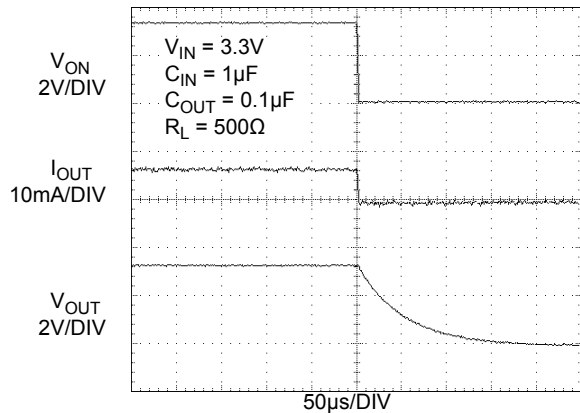


Figure 12. FPF1005  $T_{OFF}$  Response

## Typical Characteristics

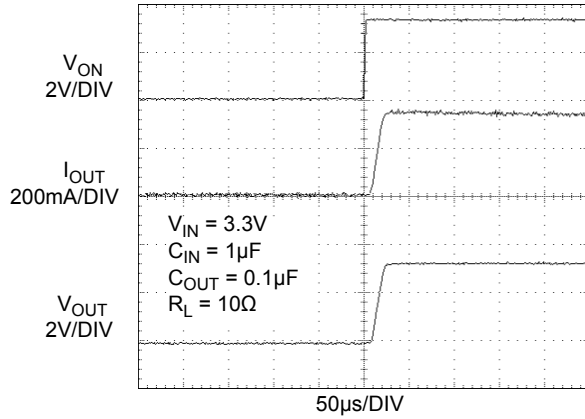


Figure 13. FPF1005  $T_{ON}$  Response

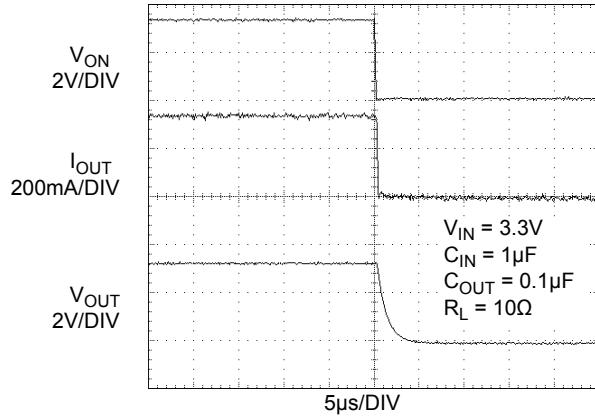


Figure 14. FPF1005  $T_{OFF}$  Response

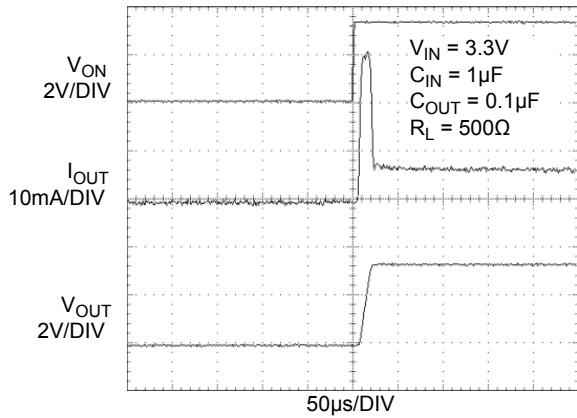


Figure 15. FPF1006  $T_{ON}$  Response

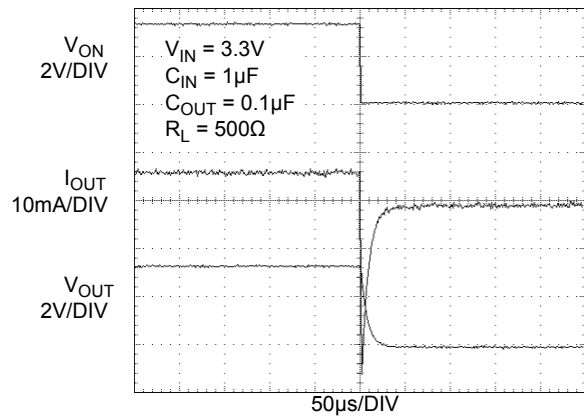


Figure 16. FPF1006  $T_{OFF}$  Response

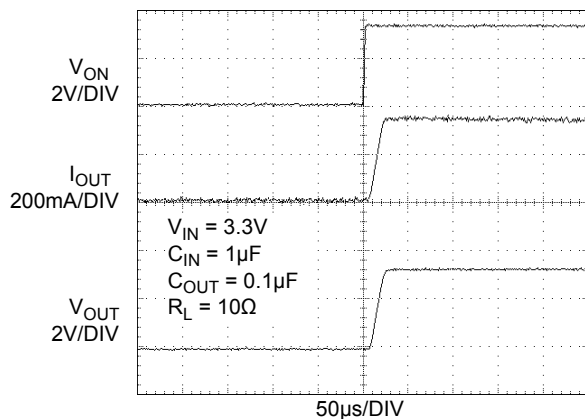


Figure 17. FPF1006  $T_{ON}$  Response

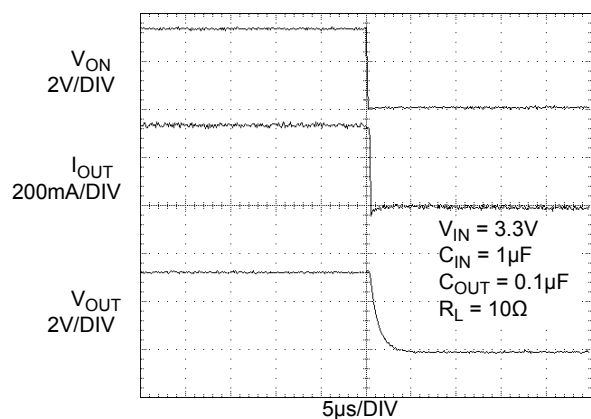


Figure 18. FPF1006  $T_{OFF}$  Response

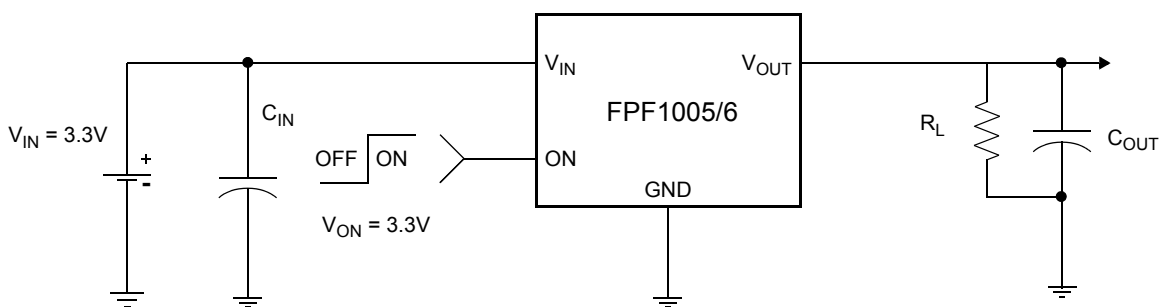
## Description of Operation

The FPF1005 & FPF1006 are low  $R_{DS(ON)}$  P-Channel load switches with controlled turn-on. The core of each device is a 55mΩ P-Channel MOSFET and a controller capable of functioning over a wide input operating range of 1.2-5.5V. The ON pin, an active HI TTL compatible input, controls the state of the switch. The FPF1006 contains a 120Ω on-chip load resistor for quick output discharge when the switch is turned off.

However,  $V_{OUT}$  pin of FPF1006 should not be connected directly to the battery source due to the discharge mechanism of the load switch.

## Application Information

### Typical Application



### Input Capacitor

To limit the voltage drop on the input supply caused by transient in-rush currents when the switch turns-on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between  $V_{IN}$  and GND. A 1μF ceramic capacitor,  $C_{IN}$ , placed close to the pins is usually sufficient. Higher values of  $C_{IN}$  can be used to further reduce the voltage drop during higher current application.

### Output Capacitor

A 0.1μF capacitor,  $C_{OUT}$ , should be placed between  $V_{OUT}$  and GND. This capacitor will prevent parasitic board inductance from forcing  $V_{OUT}$  below GND when the switch turns-off. Due to the integral body diode in the PMOS switch, a  $C_{IN}$  greater than  $C_{OUT}$  is highly recommended. A  $C_{OUT}$  greater than  $C_{IN}$  can cause  $V_{OUT}$  to exceed  $V_{IN}$  when the system supply is removed. This could result in current flow through the body diode from  $V_{OUT}$  to  $V_{IN}$ .

### Board Layout

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal and short-circuit operation. Using wide traces or large copper planes for all pins ( $V_{IN}$ ,  $V_{OUT}$ , ON and GND) will help minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.



## Evaluation Board Layout

FPF1005/6 Demo board has the components and circuitry to demonstrate the load switch functions. Thermal performance of the load switch can be improved significantly by connecting the middle pad (pin 7) to the GND area of the PCB.

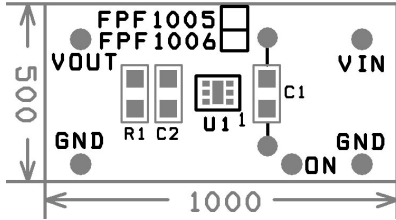


Figure 19. Demo board silk screen top and component assembly drawing.

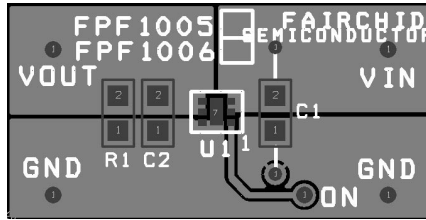


Figure 20. Demo board top and surface mount top layers view. (Pin 7 is connected to GND).

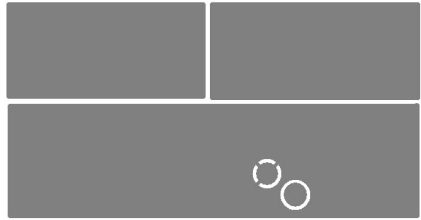
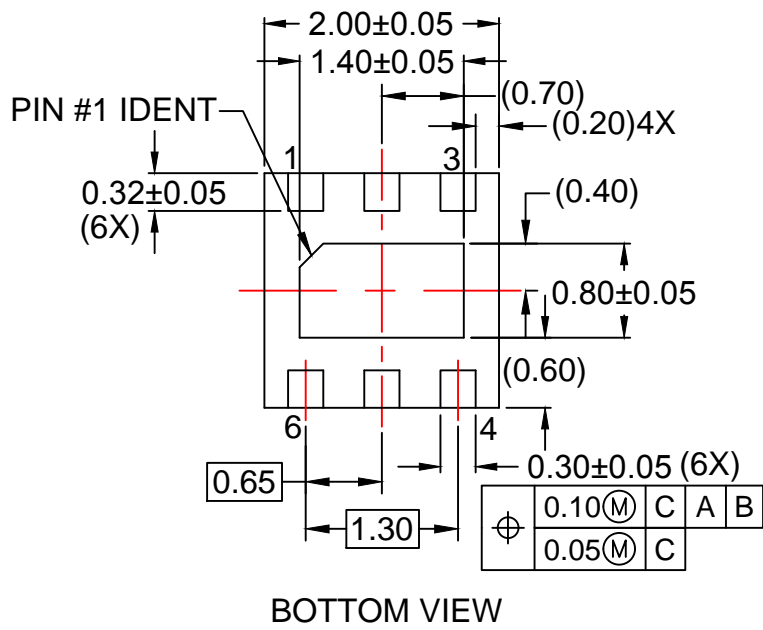
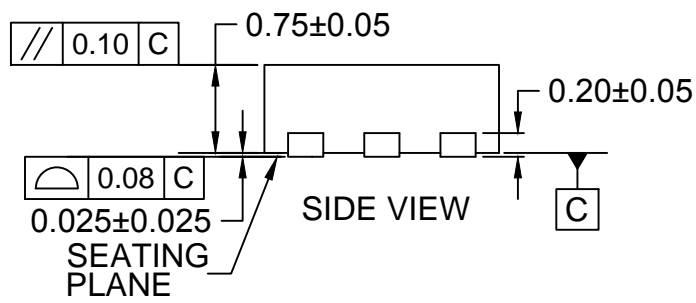
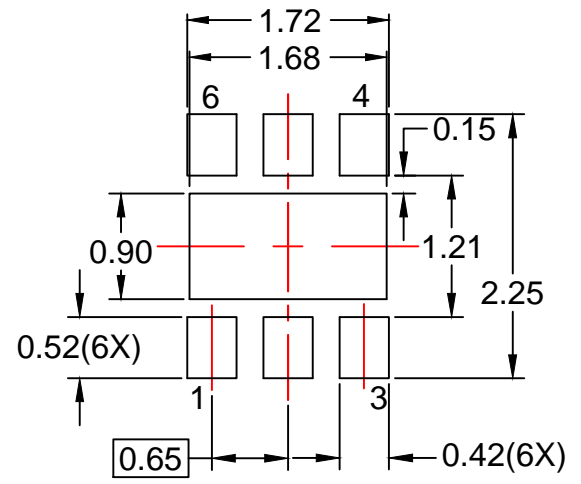
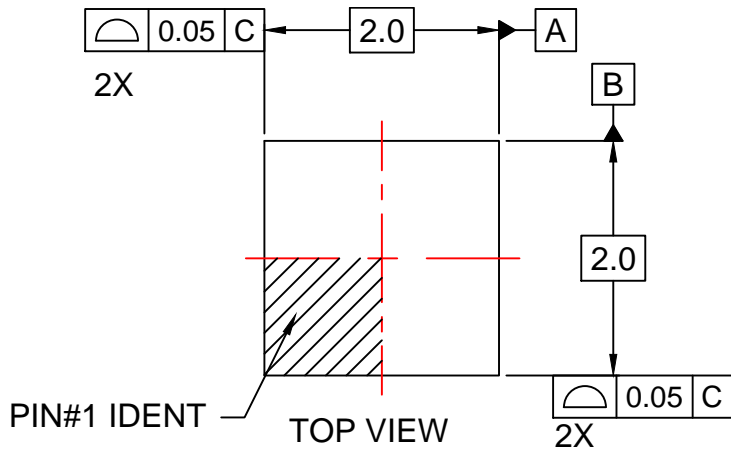


Figure 21. Demo board bottom layer view.



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- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
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