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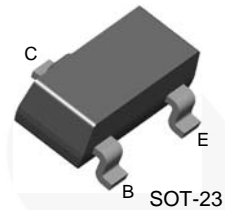
November 2014

# MMBT5401

## PNP Epitaxial Silicon Transistor

### Features

- PNP General-Purpose Amplifier
- This device is designed as a general-purpose amplifier and switch for applications requiring high voltage.



### Ordering Information

Part Number	Marking	Package	Packing Method
MMBT5401	2L	SOT-23 3L	Tape and Reel, 3000 pcs, 7 inch Reel
MMBT5401_D87Z	2L	SOT-23 3L	Tape and Reel, 10000 pcs, 13 inch Reel

### Absolute Maximum Ratings<sup>(1),(2)</sup>

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at  $T_A = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Value	Unit
$V_{CEO}$	Collector-Emitter Voltage	-150	V
$V_{CBO}$	Collector-Base Voltage	-160	V
$V_{EBO}$	Emitter-Base Voltage	-5.0	V
$I_C$	Collector Current - Continuous	-600	mA
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

#### Notes:

1. These ratings are based on a maximum junction temperature of  $150^\circ\text{C}$ .
2. These are steady-state limits. Fairchild Semiconductor should be consulted on applications involving pulsed or low-duty-cycle operations.

**Thermal Characteristics<sup>(3)</sup>**

Values are at  $T_A = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Max.	Unit
$P_D$	Total Device Dissipation	350	mW
	Derate Above $25^\circ\text{C}$	2.8	mW/ $^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	357	$^\circ\text{C}/\text{W}$

**Note:**

3. PCB size: FR-4, 76 mm x 114 mm x 1.57 mm (3.0 inch x 4.5 inch x 0.062 inch) with minimum land pattern size.

**Electrical Characteristics**

Values are at  $T_A = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Max.	Unit
$BV_{CEO}$	Collector-Emitter Breakdown Voltage <sup>(4)</sup>	$I_C = -1.0\text{ mA}, I_B = 0$	-150		V
$BV_{CBO}$	Collector-Base Breakdown Voltage	$I_C = -100\ \mu\text{A}, I_E = 0$	-160		V
$BV_{EBO}$	Emitter-Base Breakdown Voltage	$I_E = -10\ \mu\text{A}, I_C = 0$	-5.0		V
$I_{CBO}$	Collector Cut-Off Current	$V_{CB} = -120\text{ V}, I_E = 0$		-50	nA
		$V_{CB} = -120\text{ V}, I_E = 0,$ $T_A = 100^\circ\text{C}$		-50	$\mu\text{A}$
$I_{EBO}$	Emitter Cut-Off Current	$V_{EB} = -3.0\text{ V}, I_C = 0$		-50	nA
$h_{FE}$	DC Current Gain <sup>(4)</sup>	$I_C = -0.1\text{ mA}, V_{CE} = -5.0\text{ V}$	50		
		$I_C = -10\text{ mA}, V_{CE} = -5.0\text{ V}$	60	240	
		$I_C = -50\text{ mA}, V_{CE} = -5.0\text{ V}$	50		
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage <sup>(4)</sup>	$I_C = -10\text{ mA}, I_B = -1.0\text{ mA}$		-0.2	V
		$I_C = -50\text{ mA}, I_B = -5.0\text{ mA}$		-0.5	
$V_{BE(sat)}$	Base-Emitter Saturation Voltage <sup>(4)</sup>	$I_C = -10\text{ mA}, I_B = -1.0\text{ mA}$		-1.0	V
		$I_C = -50\text{ mA}, I_B = -5.0\text{ mA}$		-1.0	
$f_T$	Current Gain Bandwidth Product	$I_C = -10\text{ mA}, V_{CE} = -10\text{ V},$ $f = 100\text{ MHz}$	100	300	MHz
$C_{ob}$	Output Capacitance	$V_{CB} = -10\text{ V}, I_E = 0,$ $f = 1\text{ MHz}$		6.0	pF
$N_F$	Noise Figure	$I_C = -250\ \mu\text{A}, V_{CE} = -5.0\text{ V},$ $R_S = 1.0\text{ k}\Omega,$ $f = 10\text{ Hz to }15.7\text{ kHz}$		8.0	dB

**Note:**

4. Pulse test: Pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$

Typical Performance Characteristics

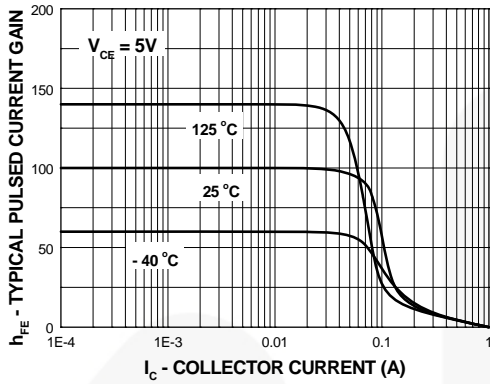


Figure 1. Typical Pulsed Current Gain vs. Collector Current

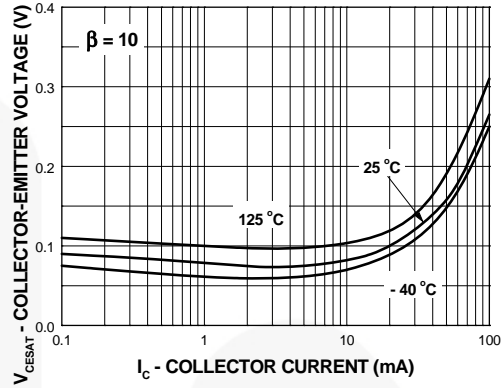


Figure 2. Collector-Emitter Saturation Voltage vs. Collector Current

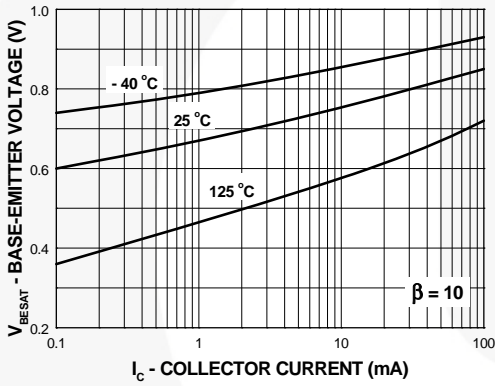


Figure 3. Base-Emitter Saturation Voltage vs. Collector Current

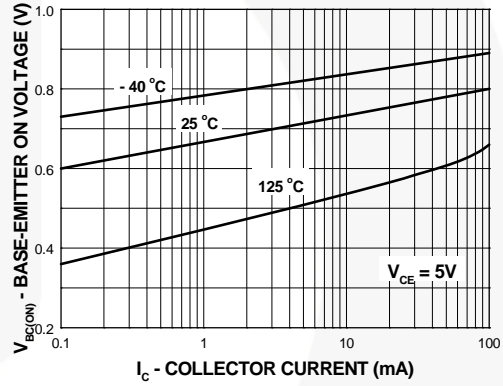


Figure 4. Base-Emitter On Voltage vs. Collector Current

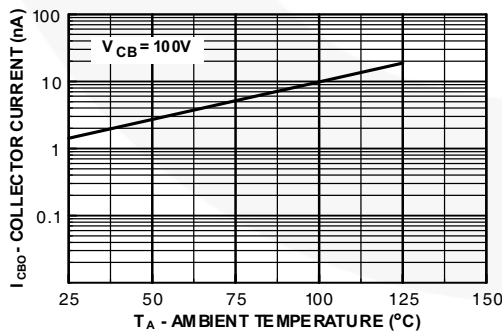


Figure 5. Collector-Cutoff Current vs. Ambient Temperature

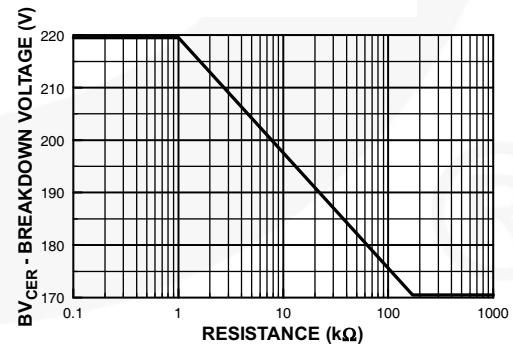


Figure 6. Collector-Emitter Breakdown Voltage with Resistance Between Emitter-Base

Typical Performance Characteristics (Continued)

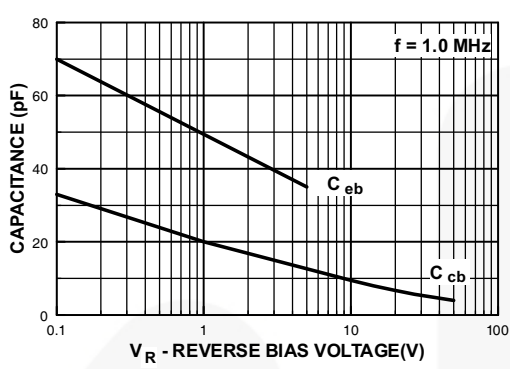


Figure 7. Input and Output Capacitance vs. Reverse Voltage

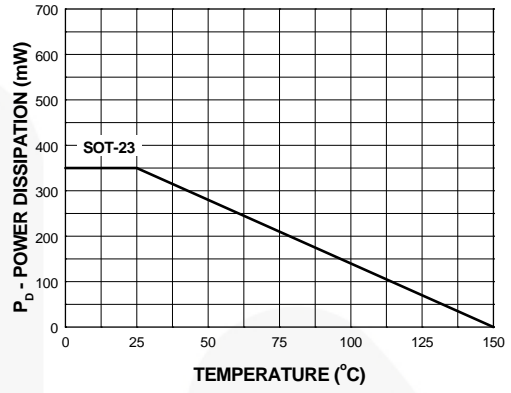
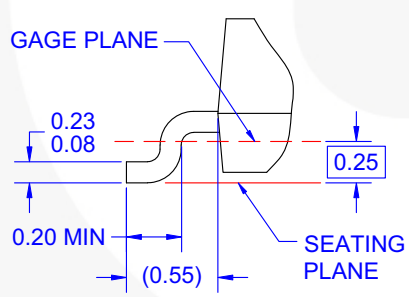
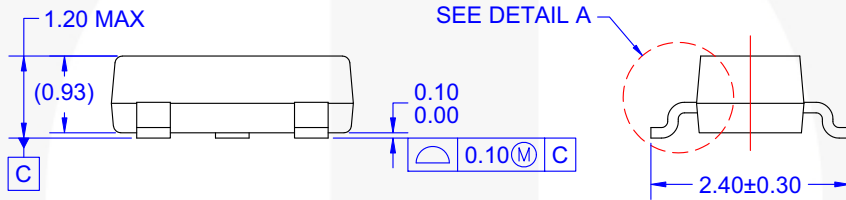
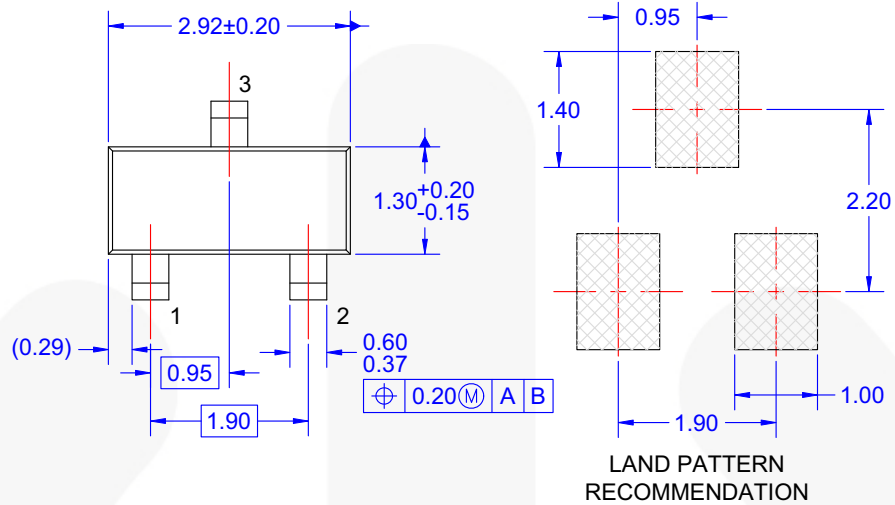


Figure 8. Power Dissipation vs. Ambient Temperature

Physical Dimensions



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) REFERENCE JEDEC REGISTRATION TO-236, VARIATION AB, ISSUE H.
  - B) ALL DIMENSIONS ARE IN MILLIMETERS.
  - C) DIMENSIONS ARE INCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
  - D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 1994.
  - E) DRAWING FILE NAME: MA03DREV10

**DETAIL A**  
SCALE: 2X

Figure 9. 3-LEAD, SOT23, JEDEC TO-236, LOW PROFILE



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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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