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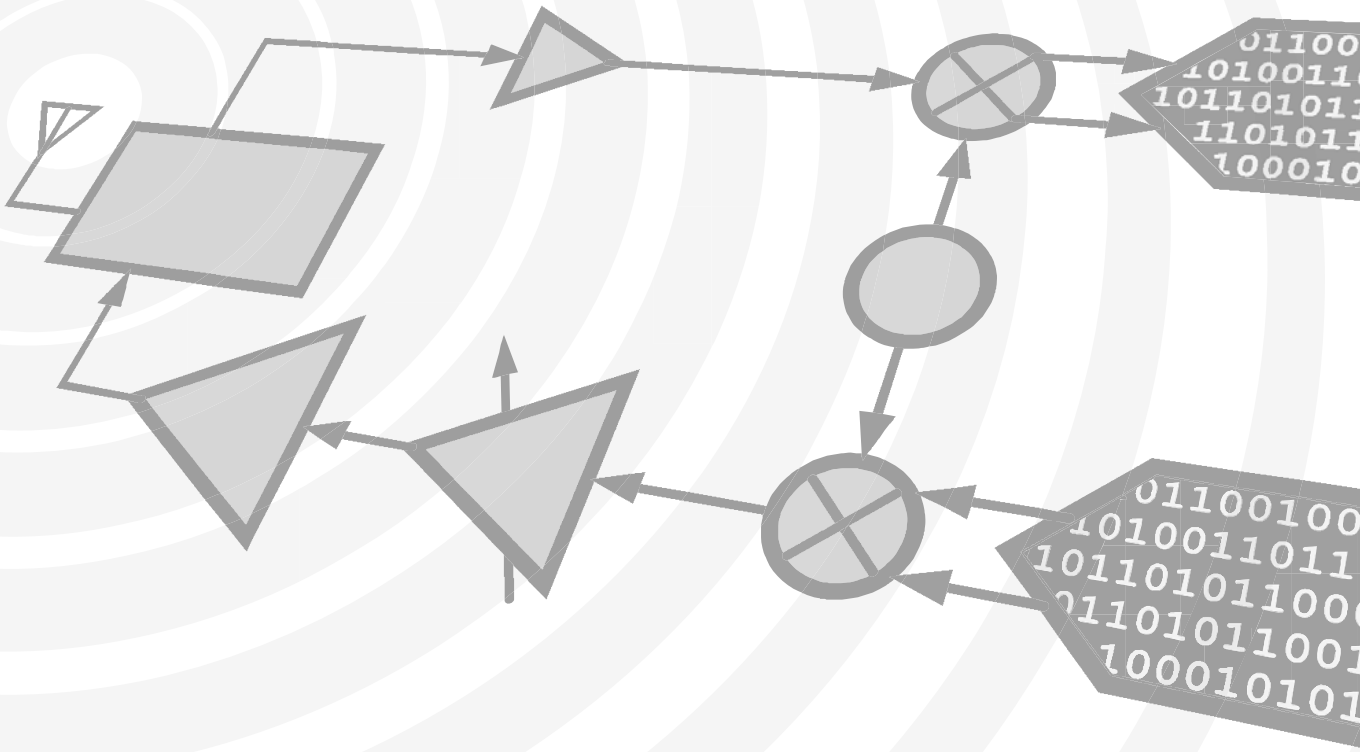

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Comparable Parts

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Evaluation Kits

- HMC860LP3E Evaluation Board

Documentation

Data Sheet

- HMC860 Data Sheet

Reference Materials

Quality Documentation

- Package/Assembly Qualification Test Report: 16L 3x3mm QFN Package (QTR: 11003 REV: 02)
- Package/Assembly Qualification Test Report: LP2, LP2C, LP3, LP3B, LP3C, LP3D, LP3F, LP3G (QTR: 2014-0364)
- Semiconductor Qualification Test Report: BiCMOS-A (QTR: 2013-00235)

Technical Articles

- Hittite Launches New DC Power Conditioning Product Line

Design Resources

- HMC860 Material Declaration
- PCN-PDN Information
- Quality And Reliability
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HMC860LP3E

QUAD LOW NOISE HIGH PSRR LINEAR VOLTAGE REGULATOR

Typical Applications

The HMC860LP3E is ideal for:

- Test Instrumentation
- Military Radios, Radar and ECM
- Basestation Infrastructure
- Ultra Low Noise Frequency Generation
- Fractional-N Synthesizer Supply
- Mixed-Signal Circuit Supply

Features

Ultra Low Noise:
3nV/√Hz at 10 kHz, 7nV/√Hz at 1 kHz

High Power Supply Rejection Ratio (PSRR)
80 dB at 1 kHz, 60 dB at 1 MHz

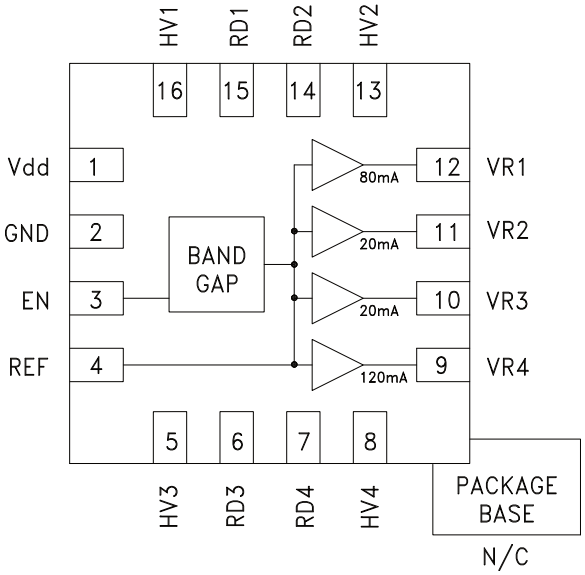
Four Voltage Outputs:
VR1 @ 3V / 80 mA
VR2, VR3 @ 3V / 20 mA
VR4 @ 4.5V / 120 mA

Adjustable Outputs: 2.5V to 5.2V

Low Power-Down Current: <1 µA

16 Lead 3x3 mm SMT Package: 9mm²

Functional Diagram



General Description

The HMC860LP3E is a BiCMOS ultra low noise quad-output voltage regulator. It features a low noise band-gap reference externally decoupled for best in-close noise performance. High Power Supply Rejection Ratio (PSRR) in the 0.1 MHz to 10 MHz range provides excellent rejection of preceding switching regulator noise. The four voltage outputs are ideal for frequency generation subsystems including Hittite's broad line of PLLs with Integrated VCOs.

Each output voltage can be adjusted higher or lower than the default value by using one external resistor. Each output can be set to 5V by grounding the corresponding HV pin. The regulator can be powered down by the TTL-compatible Enable input. The HMC860LP3E is housed in a 3x3mm QFN SMT package.

Electrical Specifications, T_A = +25 °C

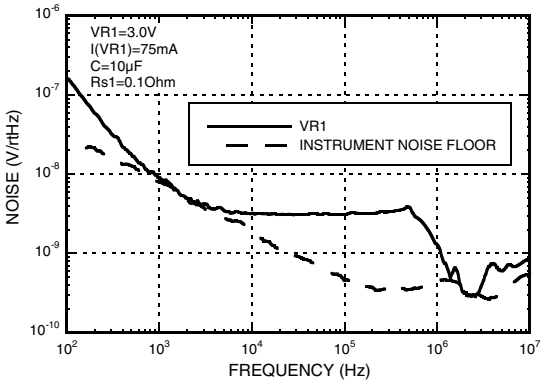
Parameter	Conditions	Min	Typ	Max	Units
Default Output Voltage VR1, VR2, VR3	Vdd = 5.5V; Maximum load current	3	3.05	3.1	V
Default Output Voltage VR4	Vdd = 5.5V; Maximum load current	4.4	4.5	4.6	V
Output Voltage Tolerance	Vdd = 5.5V; Maximum load current			2	%
Input Voltage Range (Default)	Default output voltage configuration	4.8		5.6	V
Input Voltage Range	E.g.: VR1 = VR2 = VR3 = VR4 = 3.05V; Vdd, min = 3.35V	Max (VRx) + 0.3V		5.6	V
Output Voltage Range VR1 to VR4	Set by external resistors. Vdd = Max(VRx)+0.3V	2.5		5.2	V

Electrical Specifications (Continued)

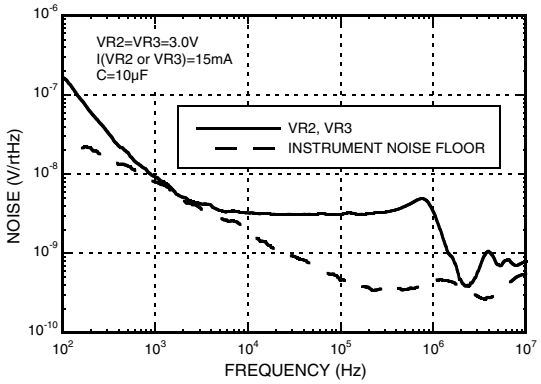
Parameter	Conditions	Min	Typ	Max	Units
Reference Voltage VREF	Vdd = 5.5V; REF cannot source/sink external current		1.21		V
Output Current VR1 [1]	T_A = -40°C to +85°C			80	mA
Output Current VR2, VR3 [1]	T_A = -40°C to +85°C			20	mA
Output Current VR4 [1]	T_A = -40°C to +85°C			120	mA
Total Output Current	T_A = -40°C to +85°C			240	mA
Output Noise Spectral Density 10 Hz 100 Hz 1 kHz 10 kHz 100 kHz	Vdd = 5.5V; VRx = 3.05V; VR4 = 4.5V Measured on Application Schematic Maximum Load Current		2200 157 7 3 3		nV/√Hz
Integrated Output Noise 100 Hz to 100 kHz	Vdd = 5.5V; VRx = 3.05V		1.5		µVrms
Load Regulation, VR1	Vdd = 5.5V		0.01		% / mA
Load Regulation, VR2 & VR3	Vdd = 5.5V		0.02		% / mA
Load Regulation, VR4	Vdd = 5.5V		0.02		% / mA
PSRR 0 Hz (DC Line Regulation) 1 kHz 100 kHz 1 MHz 10 MHz 50 MHz	Vdd = 5.5V; Maximum load current		 36 80 65 60 35 45		dB
Output Voltage Variation vs. Package Base Temperature 25°C to 85°C -40°C to 25°C	Vdd = 5.5V; Maximum load current		 0.015 0.045		 % / °C % / °C
Current Consumption (I_{GND})	Ven = Vdd = 5.5V; Maximum Load Current		1.9	2.3	mA
Power Down Current	Vdd = 5.5V; EN = Low; VRx outputs are floating (high - impedance) in Power-Down mode			1	µA
Start-Up Transient Time	0 to 90% of final voltage; Cref=1 µF; Cload=10 µF; Vdd = 5.5V		25		ms
EN Turn-On Delay	0 to 90% of final output voltage Cref = 1 µF; Cload = 10 µF; Vdd = 5.5V EN transition from 0 to Vdd		25		ms
Enable Input EN High Level		2		Vdd + 0.3	V
Enable Input EN Low Level		0		0.8	V
Output Load Capacitance	To guarantee stability, noise and PSRR performance	10			µF
Output Capacitor ESR	Required if no series resistor is used at the output. See “Stability” section.	0.2		2	Ohm
Output series resistance	Required if ESR is insufficient for one or more output capacitors. See “Stability” section.	0.1		1	Ohm

[1] The regulator does not include short-circuit or over-temperature protection circuitry. The outputs will withstand short-circuit conditions for a duration of less than 10s.

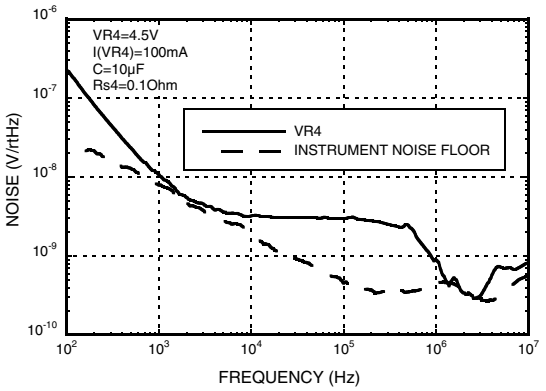
VR1 Noise Spectral Density, Vdd = 5.5V



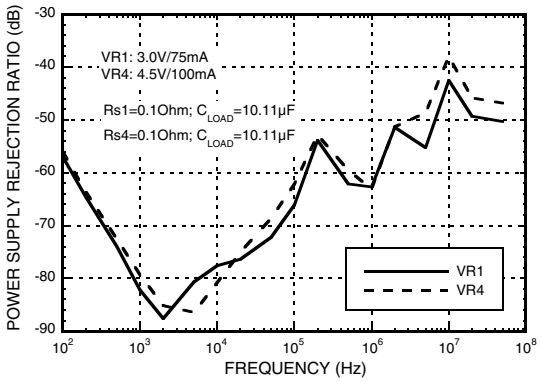
VR2, VR3 Noise Spectral Density, Vdd = 5.5V



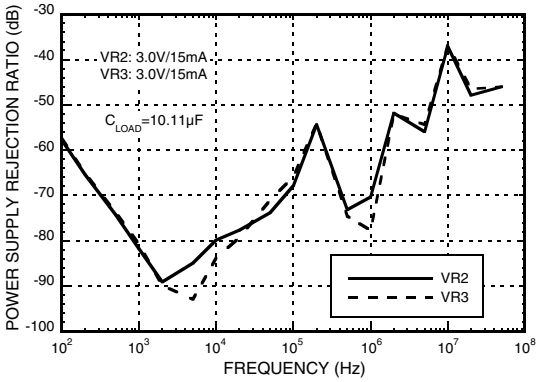
VR4 Noise Spectral Density, Vdd = 5.5V



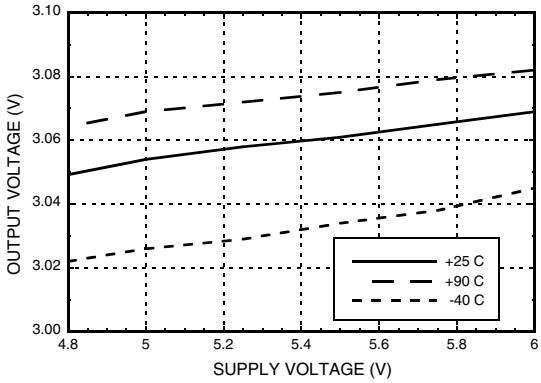
VR1, VR4 Power Supply Rejection Ratio (PSRR), Vdd = 5.5V



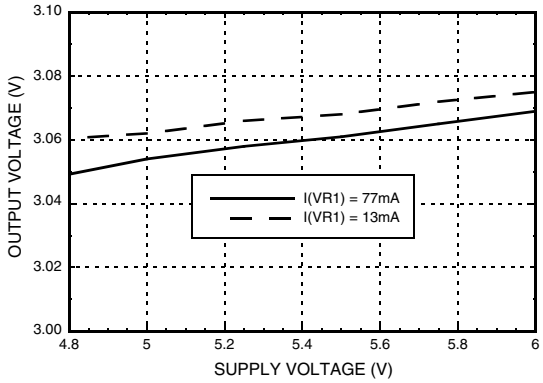
VR2, VR3 Power Supply Rejection Ratio (PSRR), Vdd = 5.5V



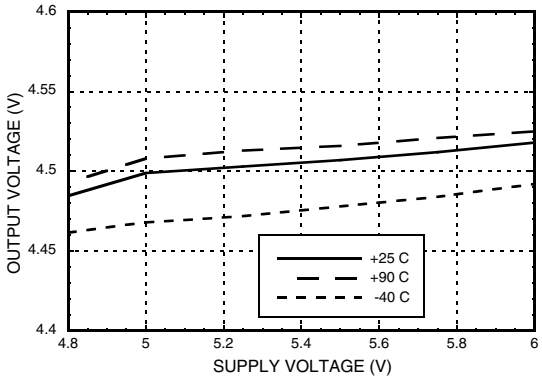
VR1 Voltage vs. Supply, I(VR1) = 75 mA



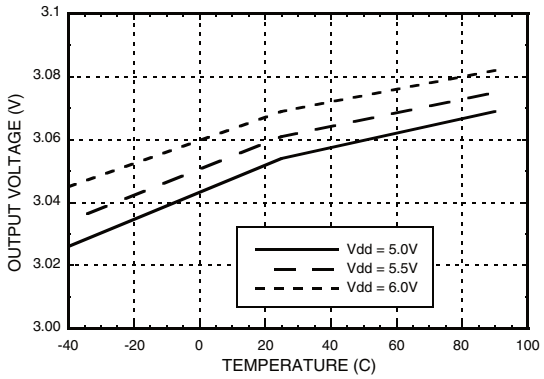
VR1 Voltage vs. Supply, T = 25 °C



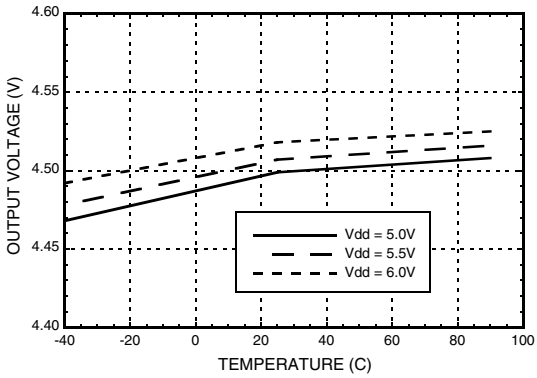
VR4 Voltage vs. Supply, I(VR4) = 100 mA



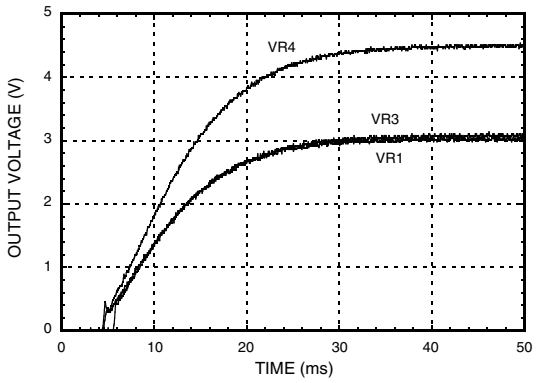
VR1 Voltage vs. Temperature, I(VR1) = 75 mA



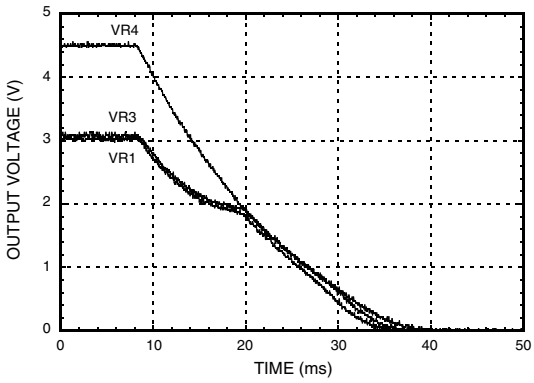
VR4 Voltage vs. Temperature, I(VR4) = 100 mA



Supply Turn-On Transient, T = 90 °C



Supply Turn-Off Transient, T = 90 °C



HMC860LP3E

QUAD LOW NOISE HIGH PSRR LINEAR VOLTAGE REGULATOR

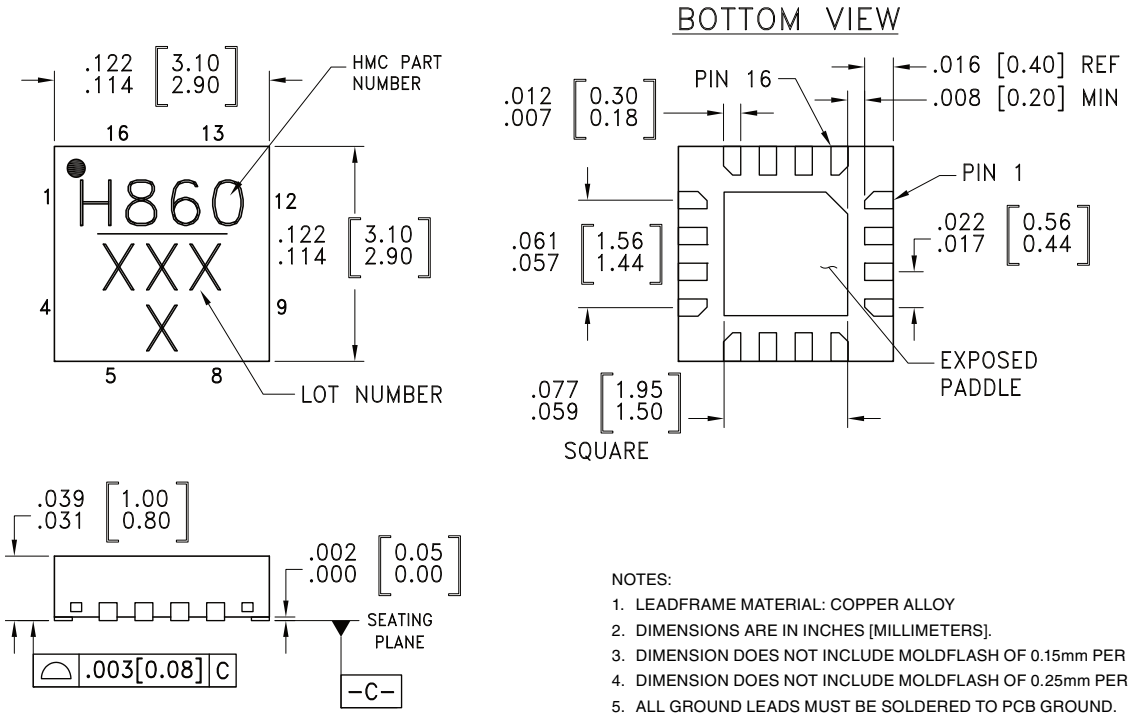
Absolute Maximum Ratings

Vdd to GND Voltage	+6.5V / -0.3V
EN to GND Voltage	Vdd + 0.5V / -0.3V
RDx / HVx to GND Voltage	Vdd + 0.5V / -0.3V
Thermal Resistance (Junction to ground paddle)	30 °C/W
Maximum Junction Temperature	+125 °C
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 1C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The absolute maximum ratings apply individually only and not in combination.

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



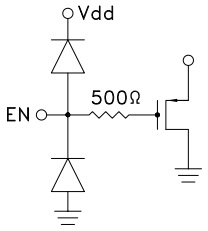
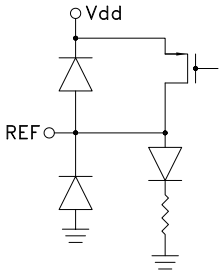
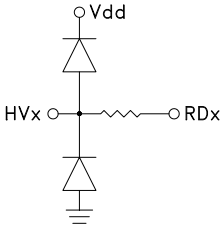
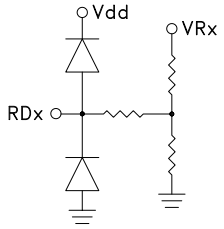
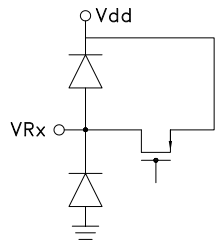
NOTES:
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS].
3. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.15mm PER SIDE.
4. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.25mm PER SIDE.
5. ALL GROUND LEADS MUST BE SOLDERED TO PCB GROUND.
6. CLASSIFIED AS MOISTURE SENSITIVITY LEVEL (MSL) 1.

Package Information

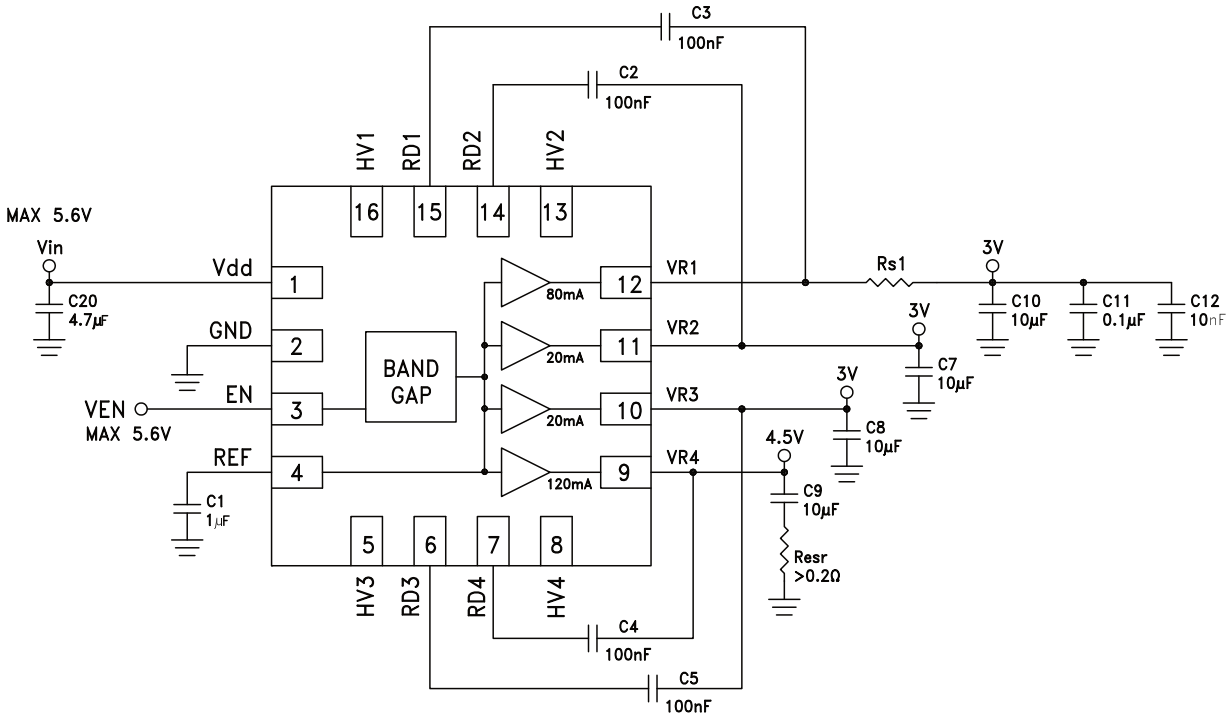
Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [1]
HMC860LP3E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H860 XXX X

[1] 4-Digit lot number XXXX
[2] Max peak reflow temperature of 260 °C

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1	Vdd	Unregulated power supply input	
2	GND	Supply Ground	
3	EN	Enable Input, TTL Logic Level. The VRx outputs are floating (high impedance) when EN = Low.	
4	REF	Reference voltage (bandgap) output. Cannot be used to source/sink current to/from external circuits	
5	HV3	Sets VR3 to 5V output when connected to ground, otherwise no connection.	
8	HV4	Sets VR4 to 5V output when connected to ground, otherwise no connection.	
13	HV2	Sets VR2 to 5V output when connected to ground, otherwise no connection.	
16	HV1	Sets VR1 to 5V output when connected to ground, otherwise no connection.	
6	RD3	Resistive feedback for VR3, see “Output Voltage Adjust” section.	
7	RD4	Resistive feedback for VR4, see “Output Voltage Adjust” section.	
14	RD2	Resistive feedback for VR2, see “Output Voltage Adjust” section.	
15	RD1	Resistive feedback for VR1, see “Output Voltage Adjust” section.	
9	VR4	Regulator #4 Output	
10	VR3	Regulator #3 Output	
11	VR2	Regulator #2 Output	
12	VR1	Regulator #1 Output	
Package Base	N/C	Should contact PCB metallic area for best thermal dissipation. Can be connected to Ground.	

Application Schematic



The specified noise performance requires the 1µF decoupling capacitor between pins REF and GND (C1) and the 100nF capacitors connected between output VRx (x=1,2,3,4) and the respective RDx pin (C2, C3, C4 and C5). If noise performance is not critical for a particular output, the 100nF capacitor can be omitted for the respective regulator. In this case, noise spectral density will typically increase by a factor of 20X at 10kHz. The 1µF REF capacitor causes a 25ms typical turn-on start-up time.

Stability

Two approaches are recommended to manage the stability of the high-current regulators VR1 and VR4. If only one decoupling capacitor is used at the output, the capacitor series resistance Resr must be between 0.2 Ohm and 2 Ohm to insure stability across all loading conditions. This is shown at output VR4 in the application schematic. Note that ceramic capacitors typically have much lower Resr (as low as 0.02 Ohm at resonance) hence they will need a series resistor to insure stability.

In the case when several capacitors are connected at the output (which is often the case with noise and spurious sensitive circuits), an alternate approach is to insert a small resistor in series with the load but after the 100nF feedback capacitor. This is shown by Rs1 at the VR1 output in the application schematic. The minimum resistor value is 0.1 Ohm, while the maximum value is set by the acceptable output voltage drop.

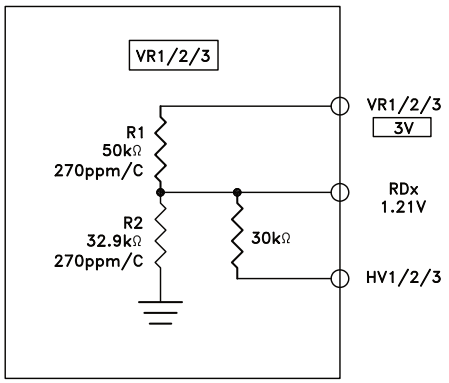
Due to the lower current, regulators VR2 and VR3 do not have special stability requirements. Typical 10µF ceramic capacitor ESR of 0.02 Ohm is sufficient for their stability.

Output Voltage Adjust

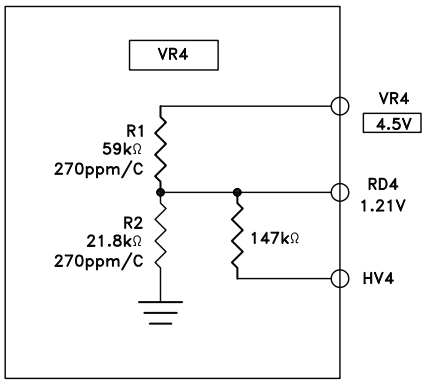
There are several ways to adjust the output voltage for each regulator. A 5V setting for any output can be achieved by grounding the respective HVx (x=1,2,3,4) pin. Any other value requires an external resistor, connected between RDx and GND for a voltage higher than the default, or between VRx and RDx for a voltage lower than the default. The figures below show the values of the internal resistive dividers that set the default output voltage a. for 3V and b. for 4.5V and two examples of two different voltage settings: c. shows a default 3V output changed to 3.3V by connecting a 220k Ohm resistor between RDx and GND, while d. shows the same output adjusted to 2.5V by connecting a 120k Ohm resistor between VRx and RDx.

The internal resistors have a temperature coefficient (TempCo) of +270ppm/°C. When the default output voltage is modified by using an external resistor with a different TempCo, the temperature behavior of the respective output will differ from this specification, although the difference will likely be very small.

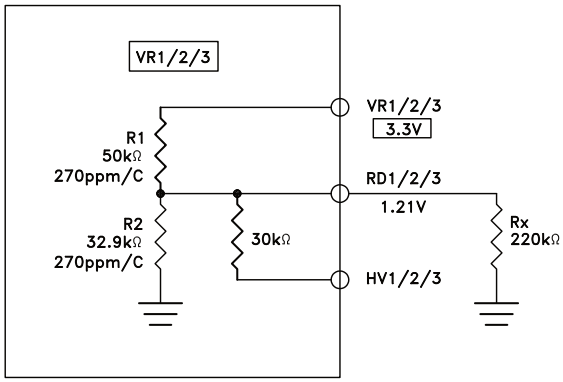
a.



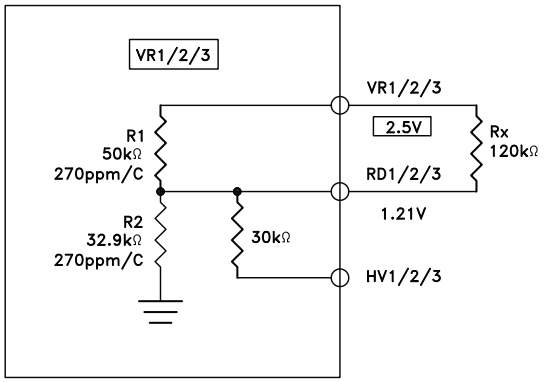
b.



c.



d.



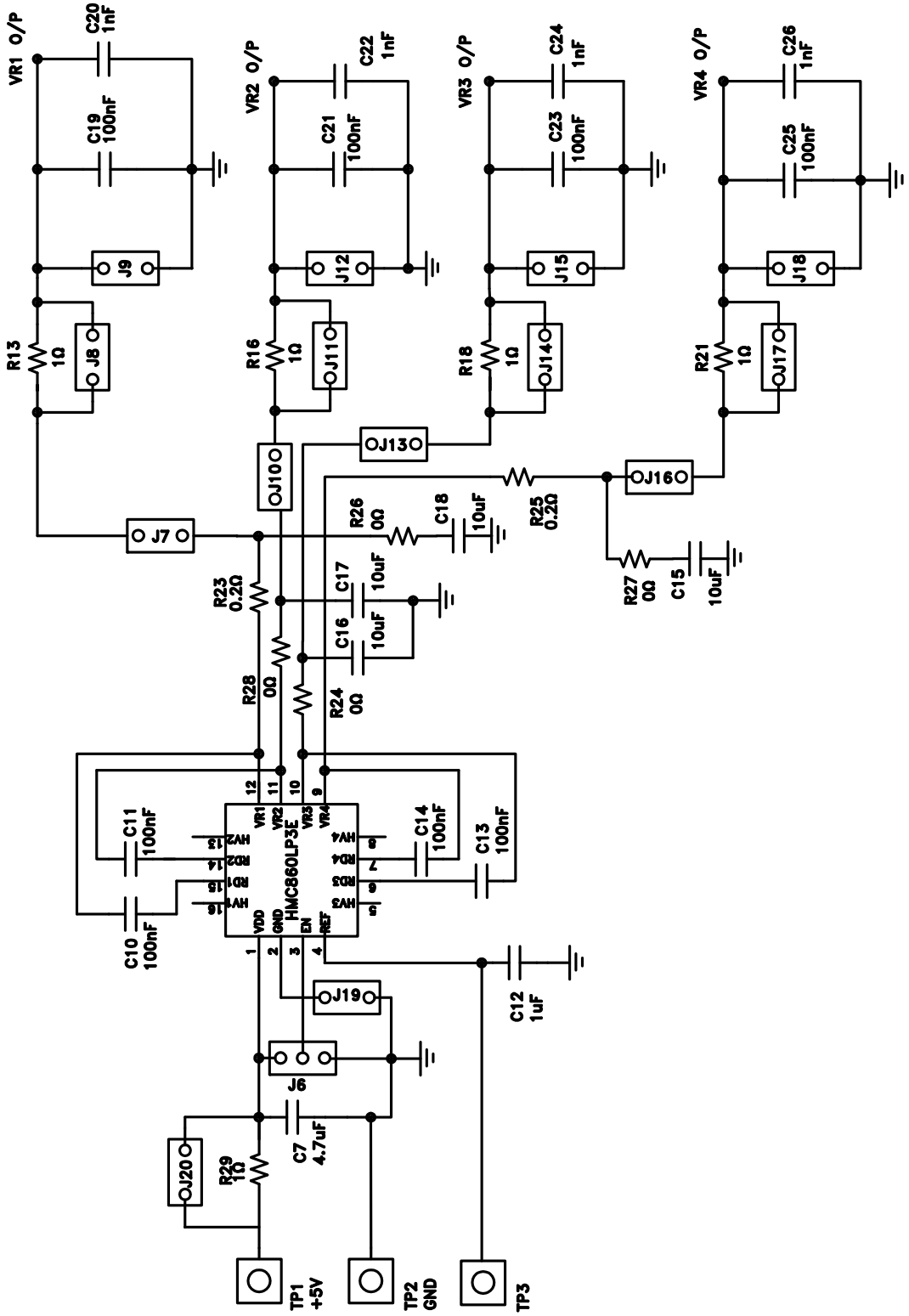
$$VRX \approx VREF \times \left(1 + \frac{R1 \times (R2 + RX)}{(R2 \times RX)}\right)$$

For VRx > VRx_default;
X = 1, 2, 3, 4
VREF=1.21 Resistor values in KΩ
VRx_default = 3V for VR1, VR2 & VR3
VRx_default = 4.5V for VR4

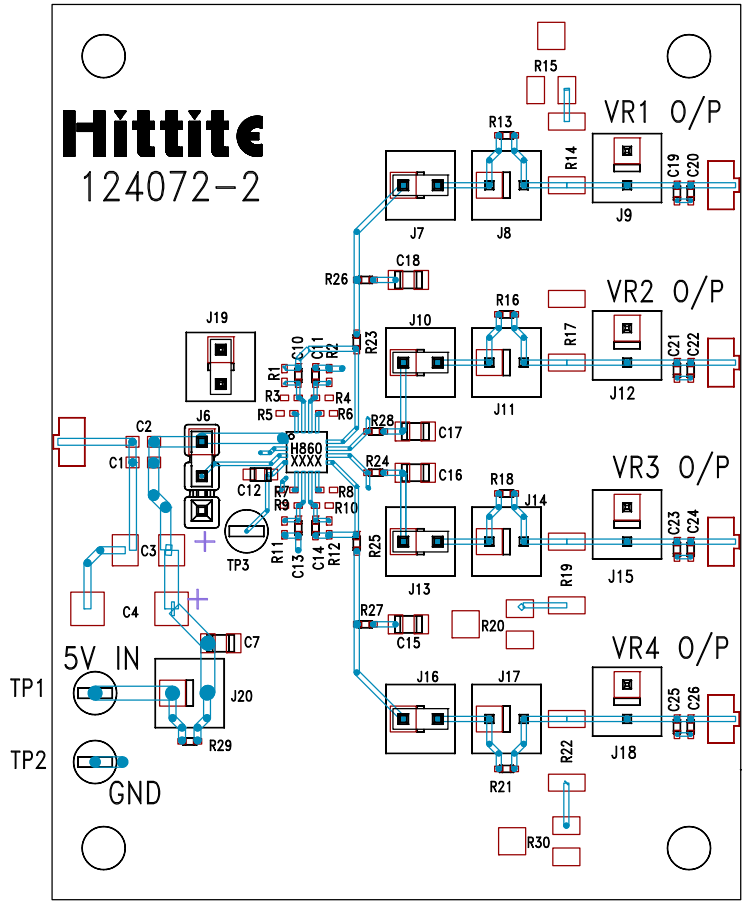
$$VRX \approx VREF \times \left(1 + \frac{R1 \times RX}{R2 \times (R1 + RX)}\right)$$

For VRx < VRx_default;
X = 1, 2, 3, 4
VREF=1.21 Resistor values in KΩ

Evaluation Schematic



Evaluation PCB



List of Materials for Evaluation PCB 124352 [1]

Item	Description
J7 - J20	2 Pos Vertical TIN
C7	4.7 µF Capacitor, 0805 Pkg.
C10, C11, C13, C14, C19, C21, C23, C25	100 nF Capacitor, 0402 Pkg.
C12	1.0 µF Capacitor, 0603 Pkg.
C15 - C18	10 µF Capacitor, 0805 Pkg.
C20, C22, C24, C26	1000 pF Capacitor, 0402 Pkg.
R13, R16, R18, R21, R29	1 Ohm Resistor, 0402 Pkg.
R23, R25	0.2 Ohm Resistor, 0402 Pkg.
R24, R26 - R28	0 Ohm Resistor, 0402 Pkg.
TP1 - TP3	Test Point PC Compact
U1	HMC860LP3E Quad Regulator

Item	Description
PCB [2]	124072 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350 or FR4

A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.