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FAIRCHILD SEMICONDUCTOR®

August 2010

NC7NZ04
TinyLogic® UHS Inverter

Features

- Ultra-High Speed: t_{PD} 2.4ns (Typical) into 50pF at 5V V_{CC}
- High Output Drive: ±24mA at 3V V_{CC}
- Broad V_{CC} Operating Range: 1.65V to 5.5V
- Power-Down, High-Impedance Inputs / Outputs
- Over-Voltage Tolerance Inputs Facilitate 5V to 3V Translation
- Proprietary Noise / EMI Reduction Circuitry
- Space-Saving MicroPak™ and US8 Surface Mount Packages

Description

The NC7NZ04 is a triple inverter from Fairchild's Ultra-High Speed (UHS) series of TinyLogic®. The device is fabricated with advanced CMOS technology to achieve ultra-high speed with high output drive while maintaining low static power dissipation over a broad V_{CC} operating range. The device is specified to operate over the 1.65V to 5.5V V_{CC} operating range. The inputs and output are high impedance when V_{CC} is 0V. Inputs tolerate voltages up to 7V, independent of V_{CC} operating voltage.

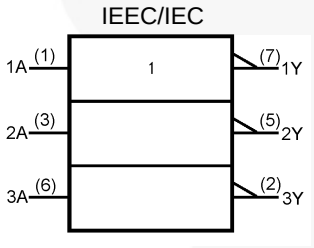


Figure 1. Logic Symbol

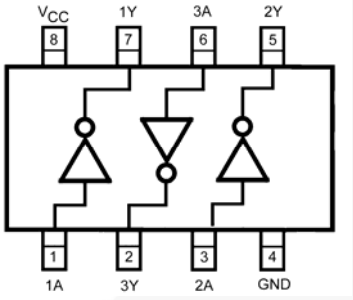


Figure 2. Connection Diagram

Ordering Information

Part Number	Top Mark	Package	Packing Method
NC7NZ04K8X	NZ04	8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide	3000 Units on Tape & Reel
NC7NZ04L8X	T3	8-Lead MicroPak™, 1.6mm Wide	5000 Units on Tape & Reel

MicroPak™ is a trademarks of Fairchild Semiconductor Corporation.

Pin Configurations

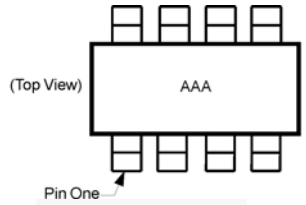


Figure 3. US8

Notes:
1. AAA represents product code top mark (see ordering table).
2. Orientation of top mark determines pin one location. Reading the top product code mark left to right, pin one is the lower left pin.

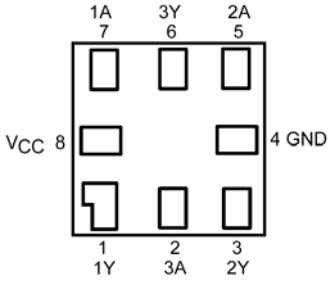


Figure 4. MicroPak™ (Top Through View)

Pin Definitions

Pin # US8	Pin # MicroPak™	Name	Description
1	7	1A	Input
2	6	3Y	Output
3	5	2A	Input
4	4	GND	Ground
5	3	2Y	Output
6	2	3A	Input
7	1	1Y	Output
8	8	V_{CC}	Supply Voltage

Function Table

Y= /A

Inputs	Output
A	**Y**
L	H
H	L

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage		-0.5	7.0	V
V_{IN}	DC Input Voltage		-0.5	7.0	V
V_{OUT}	DC Output Voltage		-0.5	7.0	V
I_{IK}	DC Input Diode Current	V_{IN} < -0.5V		-50	mA
		V_{IN} > 6.0V		+20	
I_{OK}	DC Output Diode Current	V_{OUT} < -0.5V		-50	mA
		V_{OUT} > 6V, V_{CC}=GND		+20	
I_{OUT}	DC Output Current			±50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current			±50	mA
T_{STG}	Storage Temperature Range		-65	+150	°C
T_J	Junction Temperature Under Bias			+150	°C
T_L	Junction Lead Temperature (Soldering, 10 Seconds)			+260	°C
P_D	Power Dissipation at +85°C			250	mW
ESD	Human Body Model, JEDEC:JESD22-A114			4000	V
	Charge Device Model, JEDEC:JESD22-C101			2000	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{CC}	Supply Voltage Operating		1.65	5.50	V
	Supply Voltage Data Retention		1.5	5.5	
V_{IN}	Input Voltage		0	5.5	V
V_{OUT}	Output Voltage		0	V_{CC}	V
T_A	Operating Temperature		-40	+85	°C
t_r, t_f	Input Rise and Fall Times	V_{CC} at 1.8V, 2.5V ± 0.2V	0	20	ns/V
		V_{CC} at 3.3V ± 0.3V	0	10	
		V_{CC} at 5.0V ± 0.5V	0	5	
θ_{JA}	Thermal Resistance	US8		250	°C/W
		MicroPak™		287	

Note:

3. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC}	Conditions	T_A=25°C			T_A=-40 to 85°C		Units
				Min.	Typ.	Max.	Min.	Max.	
V_{IH}	HIGH Level Input Voltage	1.80 ± 0.15		0.75V_{CC}			0.75V_{CC}		V
		2.30 to 5.50		0.70V_{CC}			0.70V_{CC}		
V_{IL}	LOW Level Input Voltage	1.80 ± 0.15				0.25V_{CC}		0.25V_{CC}	V
		2.30 to 5.50				0.30V_{CC}		0.30V_{CC}	
V_{OH}	HIGH Level Output Voltage	1.65	V_{IN}=V_{IL}, I_{OH}=-100µA	1.55	1.65		1.55		V
		2.30		2.20	2.30		2.20		
		3.00		2.90	3.00		2.90		
		4.50		4.40	4.50		4.40		
		1.65	I_{OH}=-4mA	1.29	1.52		1.29		
		2.30	I_{OH}=-8mA	1.90	2.15		1.90		
		3.00	I_{OH}=-16mA	2.40	2.80		2.40		
		3.00	I_{OH}=-24mA	2.30	2.68		2.30		
		4.50	I_{OH}=-32mA	3.80	4.20		3.80		
V_{OL}	LOW Level Output Voltage	1.65	V_{IN}=V_{IH}, I_{OL}=100µA		0.00	0.10		0.10	V
		2.30			0.00	0.10		0.10	
		3.00			0.00	0.10		0.10	
		4.50			0.00	0.10		0.10	
		1.65	I_{OL}=4mA		0.80	0.24		0.24	
		2.30	I_{OL}=8mA		0.10	0.30		0.30	
		3.00	I_{OL}=16mA		0.15	0.40		0.40	
		3.00	I_{OL}=24mA		0.22	0.55		0.55	
		4.50	I_{OL}=32mA		0.22	0.55		0.55	
I_{IN}	Input Leakage Current	0 to 5.5	0 ≤ V_{IN} ≤ 5.5V			±1		±1	µA
I_{OFF}	Power-Off Leakage Current	0	V_{IN} or V_{OUT}=5.5V			1		10	µA
I_{CC}	Quiescent Supply Current	1.65 to 5.50	V_{IN}=5.5V, GND			1		10	µA

AC Electrical Characteristics

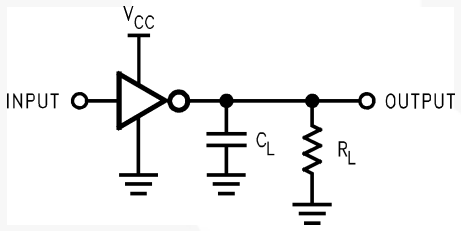
Symbol	Parameter	V_{CC}	Conditions	T_A=25°C			T_A=-40 to 85°C		Units	Figure
				Min.	Typ.	Max.	Min.	Max.		
t_{PLH}, t_{PHL}	Propagation Delay	1.80 ± 0.15	C_L=15pF, R_L=1MΩ	1.8	4.4	9.5	2.0	10.0	ns	Figure 5 Figure 6
		2.50 ± 0.20		0.8	2.9	5.1	0.8	5.6		
		3.30 ± 0.30		0.5	2.1	3.4	0.5	3.8		
		5.00 ± 0.50		0.5	1.8	2.8	0.5	3.1		
		3.30 ± 0.30	C_L=50pF, R_L=500Ω	1.2	2.9	4.5	1.2	5.0		
		5.00 ± 0.50		0.8	2.4	3.6	0.8	4.0		
C_{IN}	Input Capacitance	0			2.5				pF	
C_{PD}	Power Dissipation Capacitance(4)	3.30			9				pF	Figure 7
		5.00			11					

Note:

4. C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output lading and operating at 50% duty cycle. C_{PD} is related to I_{CCD} dynamic operating current by the expression: $I_{CCD}=(C_{PD})(V_{CC})(f_{IN})+(I_{CC}static)$.

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC}	T_A=25°c	Unit
				Typ.	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	C_L=50pF, V_{IH}=5.0V, V_{IL}=0V	5.0	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}		5.0	-0.8	V



Note:

5. C_L includes load and stray capacitance; inputs PRR=1.0MHz, t_W=500ns.

Figure 5. AC Test Circuit

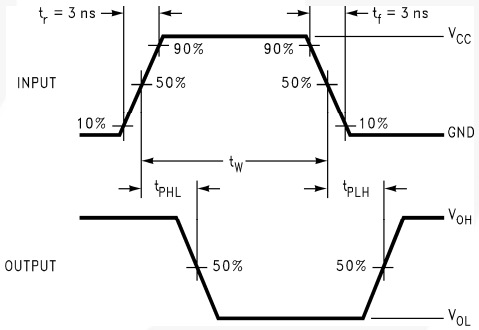
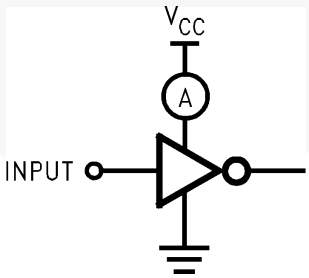


Figure 6. AC Waveforms



Note:

6. Input=AC Waveform; t_r=t_f=1.8ns; PRR=10MHz; Duty Cycle =50%.

Figure 7. I_{CCD} Test Circuit

Physical Dimensions

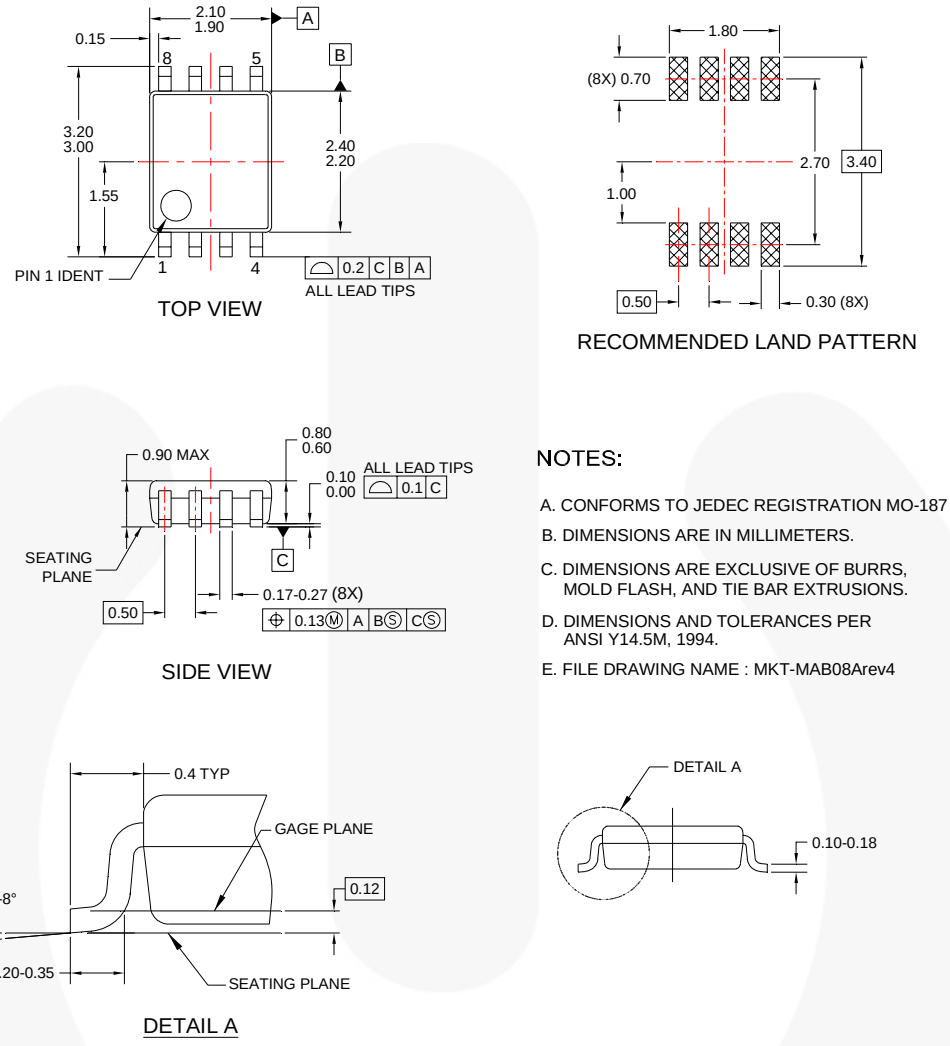


Figure 8. 8-Lead US8, JEDEC MO-187, Variation CA, 3.1mm Wide

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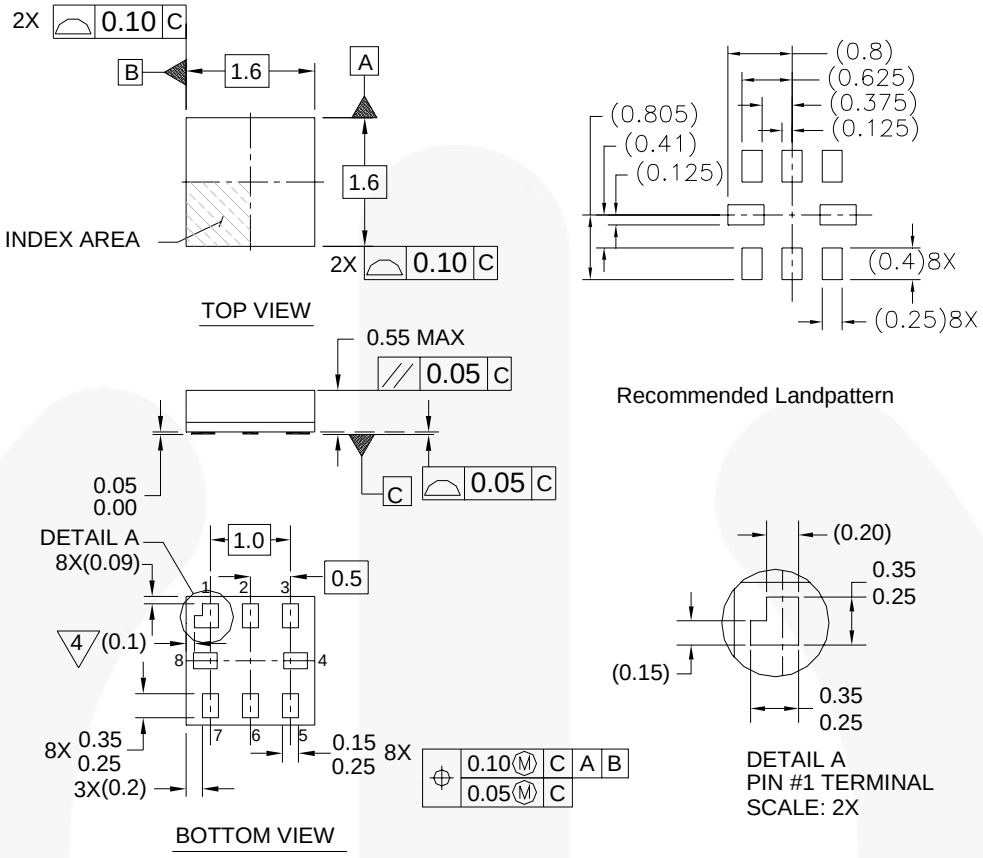
Tape and Reel Specification

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications:
http://www.fairchildsemi.com/packaging/US8_Pack_TNR.pdf

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
K8X	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

Physical Dimensions



Notes:

1. PACKAGE CONFORMS TO JEDEC MO-255 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y.14M-1994
4. PIN 1 FLAG, END OF PACKAGE OFFSET
5. DRAWING FILE NAME: MKT-MAC08AREV4

MAC08AREV4

Figure 9. 8-Lead, MicroPak™, 1.0mm Wide

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Tape and Reel Specification

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications:
http://www.fairchildsemi.com/products/logic/pdf/micropak_tr.pdf

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
L8X	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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Rev. I49

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