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## FDS3672

### N-Channel PowerTrench® MOSFET 100V, 7.5A, 22mΩ

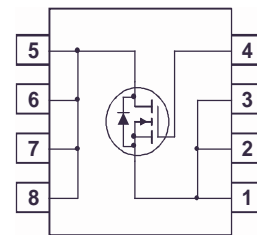
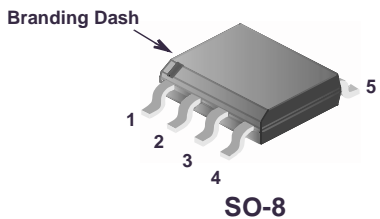
#### Features

- $r_{DS(ON)} = 19m\Omega$  (Typ.),  $V_{GS} = 10V$ ,  $I_D = 7.5A$
- $Q_g(tot) = 28nC$  (Typ.),  $V_{GS} = 10V$
- Low Miller Charge
- Low  $Q_{RR}$  Body Diode
- Optimized efficiency at high frequencies
- UIS Capability (Single Pulse and Repetitive Pulse)

#### Applications

- DC/DC converters and Off-Line UPS
- Distributed Power Architectures and VRMs
- Primary Switch for 24V and 48V Systems
- High Voltage Synchronous Rectifier

Formerly developmental type 82763



#### MOSFET Maximum Ratings $T_A = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain to Source Voltage	100	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current		
	Continuous ( $T_A = 25^\circ C$ , $V_{GS} = 10V$ , $R_{\theta JA} = 50^\circ C/W$ )	7.5	A
	Continuous ( $T_A = 100^\circ C$ , $V_{GS} = 10V$ , $R_{\theta JA} = 50^\circ C/W$ )	4.8	A
	Pulsed	Figure 4	A
$E_{AS}$	Single Pulse Avalanche Energy (Note 1)	416	mJ
$P_D$	Power dissipation	2.5	W
	Derate above $25^\circ C$	20	mW/ $^\circ C$
$T_J, T_{STG}$	Operating and Storage Temperature	-55 to 150	$^\circ C$

#### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient at 10 seconds (Note 3)	50	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient at 1000 seconds (Note 3)	85	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 2)	25	$^\circ C/W$

#### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDS3672	FDS3672	SO-8	330mm	12mm	2500 units

**Electrical Characteristics**  $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$B_{VDSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}$ , $V_{GS} = 0\text{V}$	100	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 80\text{V}$ $V_{GS} = 0\text{V}$ $T_C = 150^\circ\text{C}$	-	-	1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$	-	-	$\pm 100$	nA

**On Characteristics**

$V_{GS(TH)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\mu\text{A}$	2	-	4	V
$r_{DS(ON)}$	Drain to Source On Resistance	$I_D = 7.5\text{A}$ , $V_{GS} = 10\text{V}$	-	0.019	0.023	$\Omega$
		$I_D = 6.8\text{A}$ , $V_{GS} = 6\text{V}$	-	0.023	0.028	
		$I_D = 7.5\text{A}$ , $V_{GS} = 10\text{V}$ , $T_C = 150^\circ\text{C}$	-	0.035	0.043	

**Dynamic Characteristics**

$C_{ISS}$	Input Capacitance	$V_{DS} = 25\text{V}$ , $V_{GS} = 0\text{V}$ , $f = 1\text{MHz}$	-	2015	-	pF
$C_{OSS}$	Output Capacitance		-	285	-	pF
$C_{RSS}$	Reverse Transfer Capacitance		-	70	-	pF
$Q_{g(TOT)}$	Total Gate Charge at 10V	$V_{GS} = 0\text{V}$ to 10V	-	28	37	nC
$Q_{g(TH)}$	Threshold Gate Charge	$V_{GS} = 0\text{V}$ to 2V	-	4	6	nC
$Q_{gs}$	Gate to Source Gate Charge	$V_{DD} = 50\text{V}$ $I_D = 7.5\text{A}$ $I_g = 1.0\text{mA}$	-	10	-	nC
$Q_{gs2}$	Gate Charge Threshold to Plateau		-	6.8	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		-	6	-	nC

**Switching Characteristics** ( $V_{GS} = 10\text{V}$ )

$t_{ON}$	Turn-On Time	$V_{DD} = 50\text{V}$ , $I_D = 4\text{A}$ $V_{GS} = 10\text{V}$ , $R_{GS} = 10\Omega$	-	-	51	ns
$t_{d(ON)}$	Turn-On Delay Time		-	14	-	ns
$t_r$	Rise Time		-	20	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time		-	37	-	ns
$t_f$	Fall Time		-	27	-	ns
$t_{OFF}$	Turn-Off Time		-	-	96	ns

**Drain-Source Diode Characteristics**

$V_{SD}$	Source to Drain Diode Voltage	$I_{SD} = 7.5\text{A}$	-	-	1.25	V
		$I_{SD} = 4\text{A}$	-	-	1.0	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 7.5\text{A}$ , $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	55	ns
$Q_{RR}$	Reverse Recovered Charge	$I_{SD} = 7.5\text{A}$ , $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	90	nC

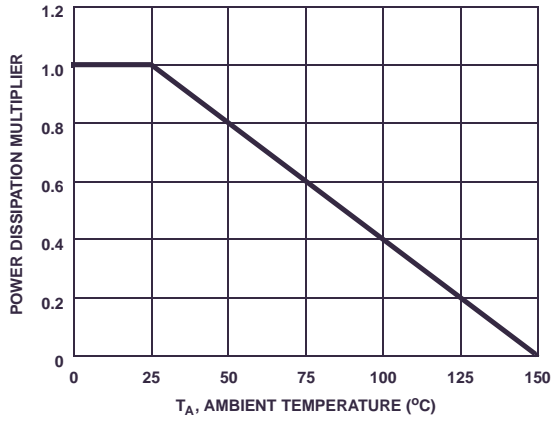
**Notes:**

1: Starting  $T_j = 25^\circ\text{C}$ ,  $L = 13\text{mH}$ ,  $I_{AS} = 8\text{A}$ .

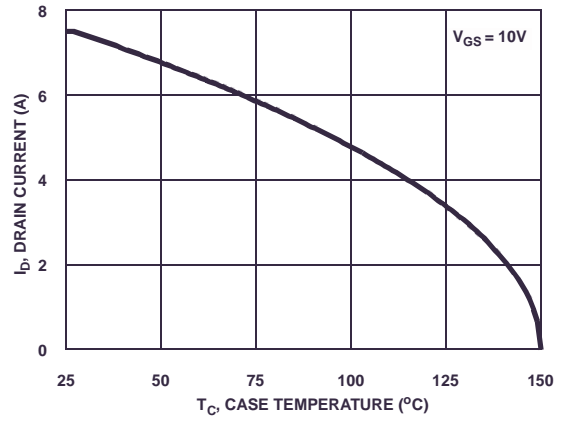
2:  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.

3:  $R_{\theta JA}$  is measured with 1.0 in<sup>2</sup> copper on FR-4 board

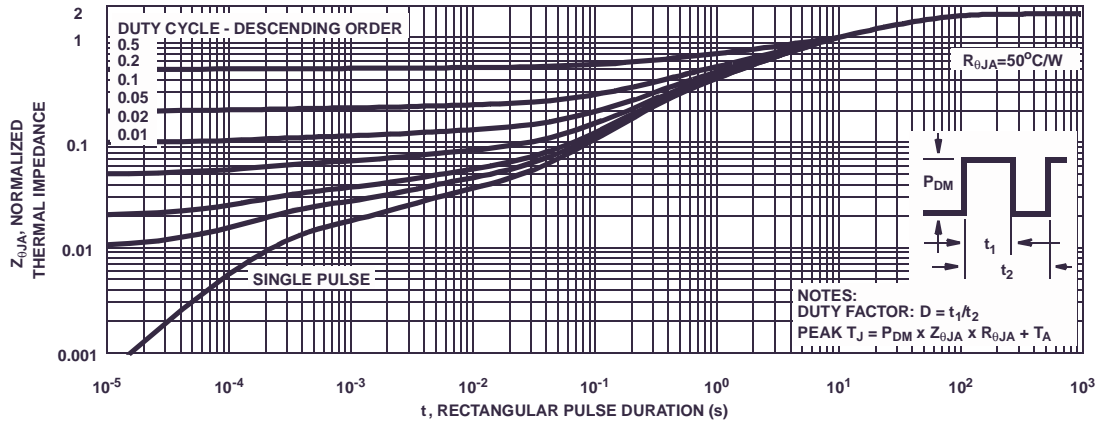
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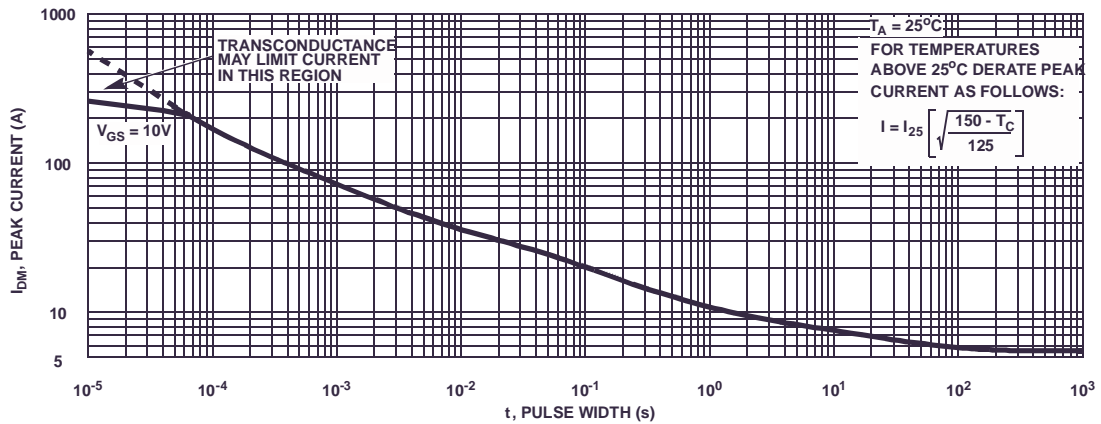
**Figure 1. Normalized Power Dissipation vs Ambient Temperature**



**Figure 2. Maximum Continuous Drain Current vs Case Temperature**

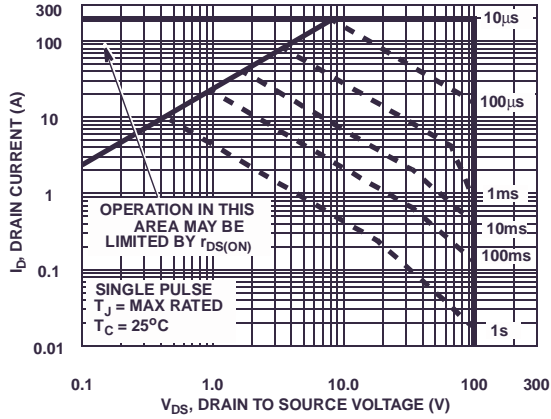


**Figure 3. Normalized Maximum Transient Thermal Impedance**

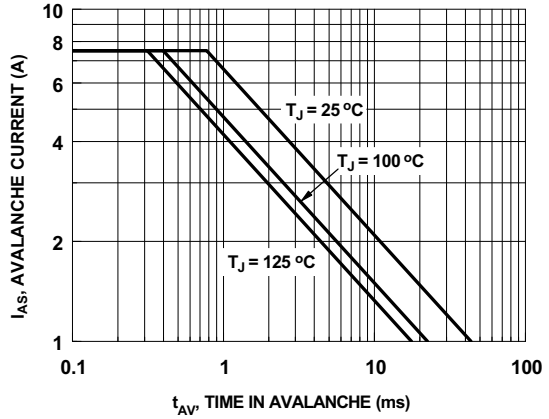


**Figure 4. Peak Current Capability**

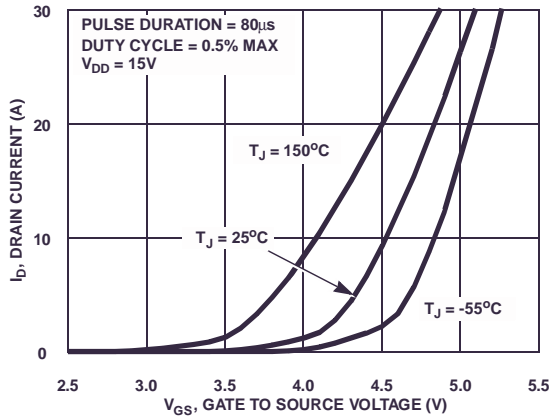
**Typical Characteristics**  $T_A = 25^\circ\text{C}$  unless otherwise noted



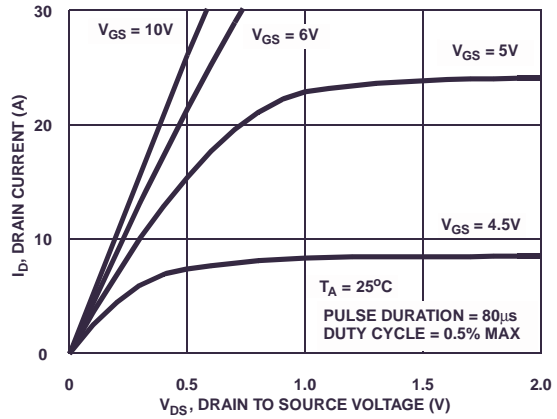
**Figure 5. Forward Bias Safe Operating Area**



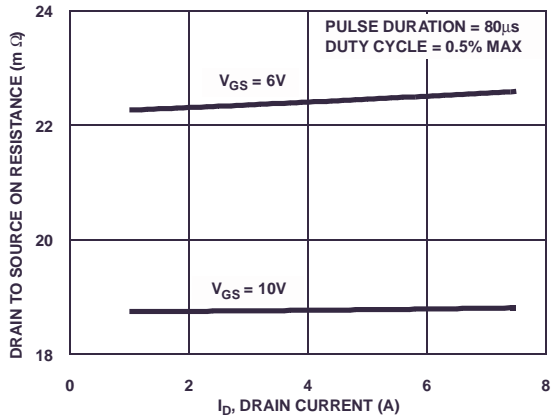
**Figure 6. Unclamped Inductive Switching Capability**



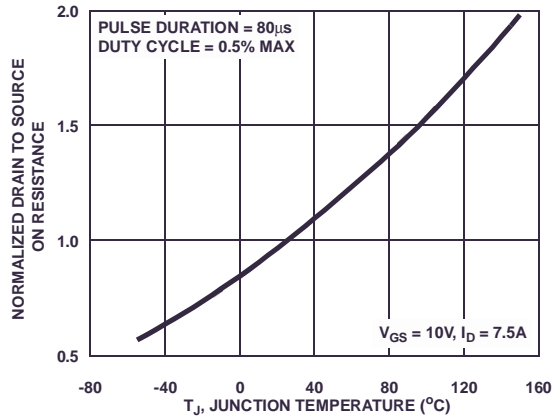
**Figure 7. Transfer Characteristics**



**Figure 8. Saturation Characteristics**

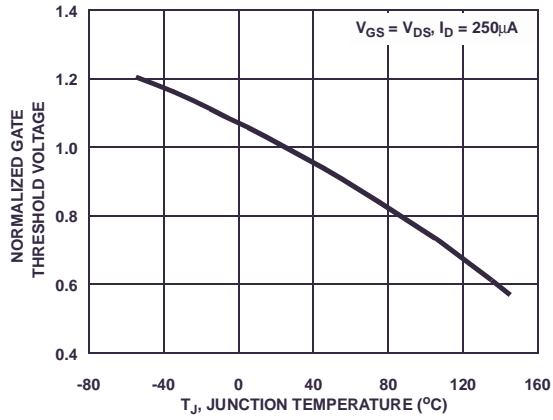


**Figure 9. Drain to Source On Resistance vs Drain Current**

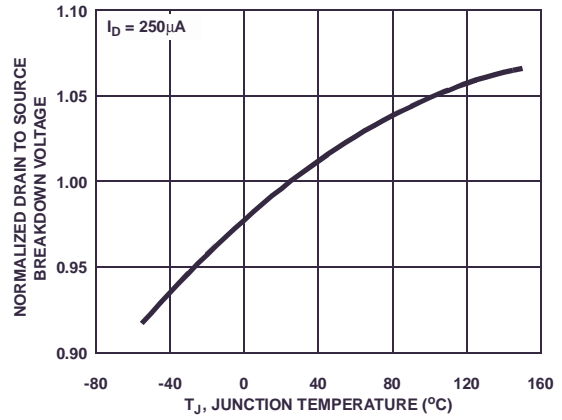


**Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature**

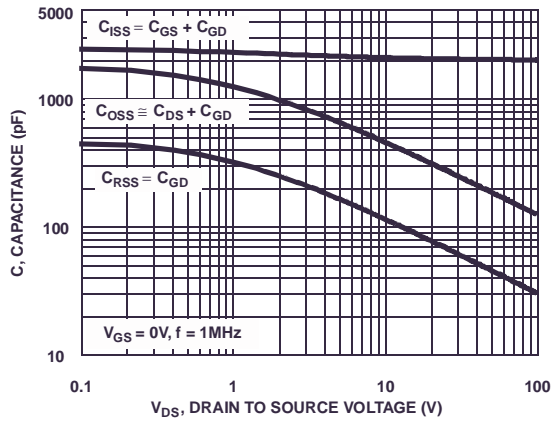
**Typical Characteristics**  $T_A = 25^\circ\text{C}$  unless otherwise noted



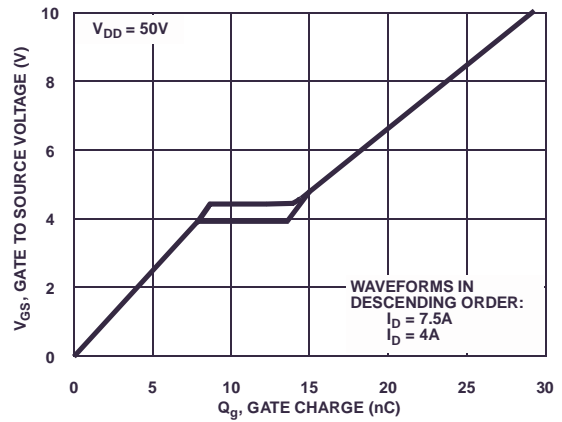
**Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature**



**Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature**



**Figure 13. Capacitance vs Drain to Source Voltage**



**Figure 14. Gate Charge Waveforms for Constant Gate Currents**

Test Circuits and Waveforms

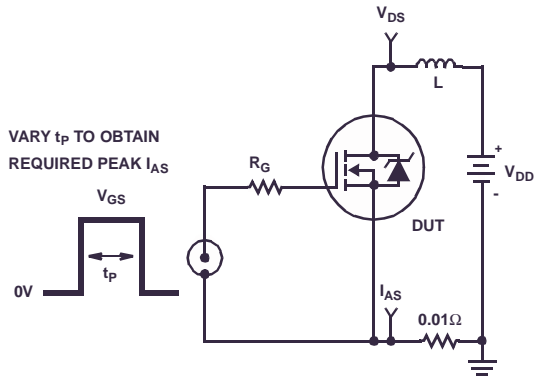


Figure 15. Unclamped Energy Test Circuit

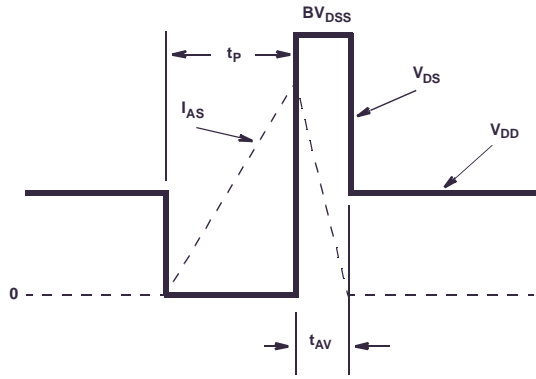


Figure 16. Unclamped Energy Waveforms

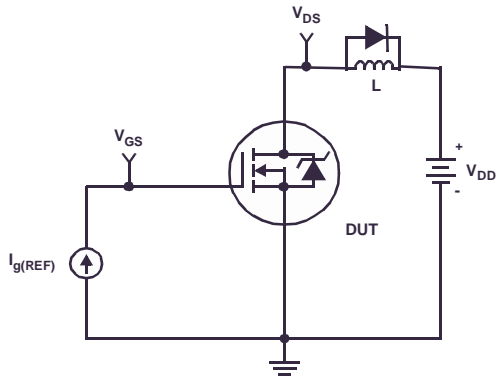


Figure 17. Gate Charge Test Circuit

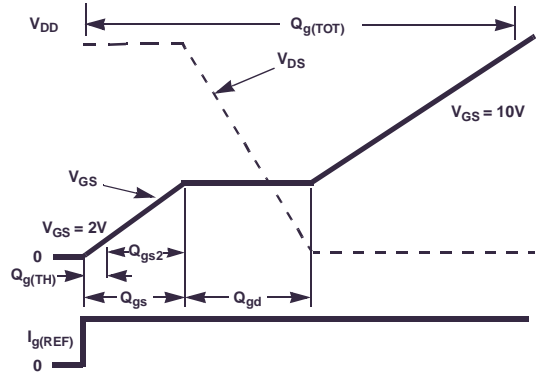


Figure 18. Gate Charge Waveforms

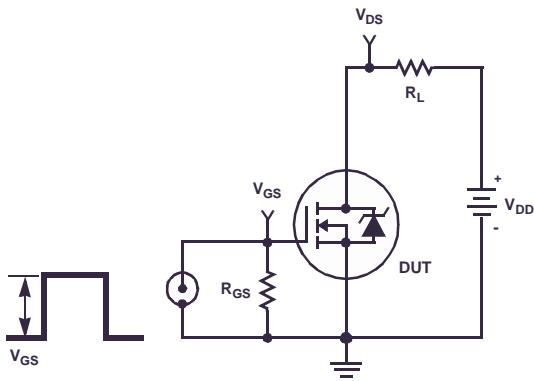


Figure 19. Switching Time Test Circuit

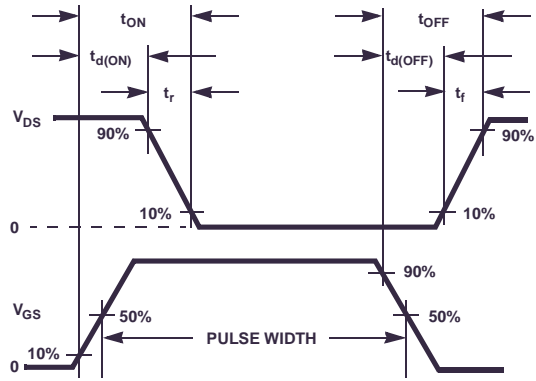







Figure 20. Switching Time Waveforms



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