2:1 HDMI/DVI Switch with Equalization

AD8196

FEATURES

- Two inputs, one output HDMI™/DVI links
- Enables HDMI 1.3-compliant receiver
- Pin-to-pin compatible with the AD8190
  - Four TMDS™ channels per link
    - Supports 250 Mbps to 2.25 Gbps data rates
    - Supports 25 MHz to 225 MHz pixel clocks
    - Equalized inputs for operation with long HDMI cables (20 meters at 2.25 Gbps)
    - Fully buffered unidirectional inputs/outputs
    - Globally switchable, 50 Ω on-chip terminations
    - Pre-emphasized outputs
    - Low added jitter
    - Single-supply operation (3.3 V)
  - Four auxiliary channels per link
    - Bidirectional unbuffered inputs/outputs
    - Flexible supply operation (3.3 V to 5 V)
    - HDCP standard compatible
    - Allows switching of DDC bus and two additional signals
- Output disable feature
  - Reduced power dissipation
  - Output termination removal
- Two AD8196s support HDMI/DVI dual-link
- Standards compliant: HDMI receiver, HDCP, DVI
- Serial (I²C® slave) control interface
- 56-lead, 8 mm x 8 mm, LFCSP, Pb-free package

APPLICATIONS

- Multiple input displays
- Projectors
- A/V receivers
- Set-top boxes
- Advanced television (HDTV) sets

FUNCTIONAL BLOCK DIAGRAM

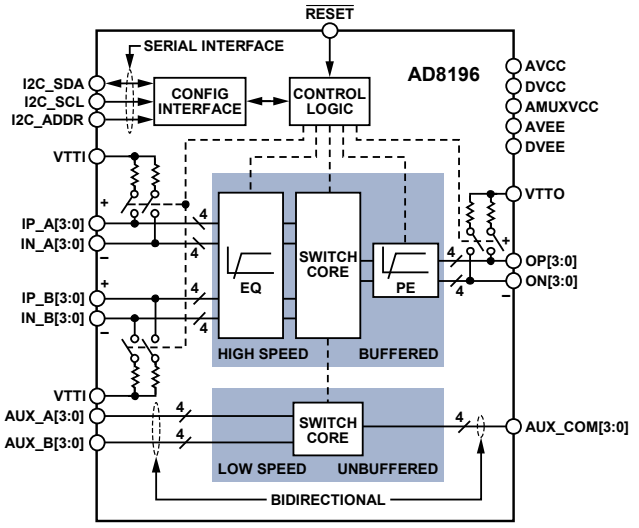

Figure 1.

TYPICAL APPLICATION

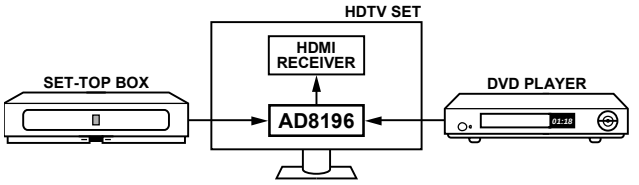

Figure 2. Typical AD8196 Application for HDTV Sets

GENERAL DESCRIPTION

The AD8196 is an HDMI/DVI switch featuring equalized TMDS inputs and pre-emphasized TMDS outputs, ideal for systems with long cable runs. Outputs can be set to a high impedance state to reduce the power dissipation and/or allow the construction of larger arrays using the wire-OR technique.

The AD8196 is provided in a space-saving, 56-lead, LFCSP, surface-mount, Pb-free, plastic package and is specified to operate over the −40°C to +85°C temperature range.

PRODUCT HIGHLIGHTS

1. Supports data rates up to 2.25 Gbps, enabling greater than 1080p deep color (12-bit color) HDMI formats, and greater than UXGA (1600 × 1200) DVI resolutions.
2. Input cable equalizer enables use of long cables at the input (more than 20 meters of 24 AWG cable at 2.25 Gbps).
3. Auxiliary switch allows routing of the DDC bus and two additional single-ended signals for a single chip, HDMI 1.3 receive-compliant solution.

Rev. 0

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- AD8196 Evaluation Board

Documentation

Data Sheet

- AD8196: 2:1 HDMI/DVI Switch with Equalization Data Sheet

Reference Materials

Informational

- Advantiv™ Advanced TV Solutions

Technical Articles

- Analysis of Common Failures of HDMI CT
- Video Portables and Cameras Get HDMI Outputs

Design Resources

- AD8196 Material Declaration
- PCN-PDN Information
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REVISION HISTORY

1/07—Revision 0: Initial Version

SPECIFICATIONS

T_A = 27°C, AVCC = 3.3 V, VTTI = 3.3 V, VTTO = 3.3 V, DVCC = 3.3 V, AMUXVCC = 5 V, AVEE = 0 V, DVEE = 0 V, differential input swing = 1000 mV, TMDS outputs terminated with external 50 Ω resistors to 3.3 V, unless otherwise noted.

Table 1.

Parameter	Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
Maximum Data Rate (DR) per Channel	NRZ	2.25			Gbps
Bit Error Rate (BER)	PRBS $2^{23} - 1$			10^{-9}	
Added Deterministic Jitter	DR ≤ 2.25 Gbps, PRBS $2^7 - 1$, EQ = 12 dB		25		ps (p-p)
Added Random Jitter			1		ps (rms)
Differential Intrapair Skew	At output		1		ps
Differential Interpair Skew[1]	At output		40		ps
EQUALIZATION PERFORMANCE					
Receiver (Highest Setting)[2]	Boost frequency = 825 MHz		12		dB
Transmitter (Highest Setting)[3]	Boost frequency = 825 MHz		6		dB
INPUT CHARACTERISTICS					
Input Voltage Swing	Differential	150		1200	mV
Input Common-Mode Voltage (V_{ICM})		AVCC − 800		AVCC	mV
OUTPUT CHARACTERISTICS					
High Voltage Level	Single-ended high speed channel	AVCC − 10		AVCC + 10	mV
Low Voltage Level	Single-ended high speed channel	AVCC − 600		AVCC − 400	mV
Rise/Fall Time (20% to 80%)		75	135	200	ps
INPUT TERMINATION					
Resistance	Single-ended		50		Ω
AUXILIARY CHANNELS					
On Resistance, R_{AUX}			100		Ω
On Capacitance, C_{AUX}	DC bias = 2.5 V, ac voltage = 3.5 V, f = 100 kHz		8		pF
Input/Output Voltage Range		DVEE		AMUXVCC	V
POWER SUPPLY					
AVCC	Operating range	3	3.3	3.6	V
QUIESCENT CURRENT					
AVCC	Outputs disabled	30	40	45	mA
	Outputs enabled, no pre-emphasis	53	60	66	mA
	Outputs enabled, maximum pre-emphasis	98	108	120	mA
VTTI	Input termination on[4]	5	40	54	mA
VTTO	Output termination on, no pre-emphasis	36	40	44	mA
	Output termination on, maximum pre-emphasis	73	80	88	mA
DVCC		4	7	10	mA
AMUXVCC			0.01	0.1	mA
POWER DISSIPATION					
	Outputs disabled	115	271	364	mW
	Outputs enabled, no pre-emphasis	411	574	664	mW
	Outputs enabled, maximum pre-emphasis	754	936	1057	mW
TIMING CHARACTERISTICS					
Switching/Update Delay	High speed switching register: HS_CH			200	ms
	All other configuration registers			1.5	µs
$\overline{\text{RESET}}$ Pulse Width		50			ns

Parameter	Conditions/Comments	Min	Typ	Max	Unit
SERIAL CONTROL INTERFACE[5]					
Input High Voltage, V_{IH}		2			V
Input Low Voltage, V_{IL}				0.8	V
Output High Voltage, V_{OH}		2.4			V
Output Low Voltage, V_{OL}				0.4	V

[1] Differential interpair skew is measured between the TMDS pairs of a single link.
[2] AD8196 output meets the transmitter eye diagram as defined in the DVI Standard Revision 1.0 and the HDMI Standard Revision 1.3.
[3] Cable output meets the receiver eye diagram mask as defined in the DVI Standard Revision 1.0 and the HDMI Standard Revision 1.3.
[4] Typical value assumes only the selected HDMI/DVI link is active with nominal signal swings and that the unselected HDMI/DVI link is deactivated. Minimum and maximum limits are measured at the respective extremes of input termination resistance and input voltage swing.
[5] The AD8196 is an I^2C slave and its serial control interface is based on the 3.3 V I^2C bus specification.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
AVCC to AVEE	3.7 V
DVCC to DVEE	3.7 V
DVEE to AVEE	±0.3 V
VTTI	AVCC + 0.6 V
VTTO	AVCC + 0.6 V
AMUXVCC	5.5 V
Internal Power Dissipation	4.62 W
High Speed Input Voltage	AVCC − 1.4 V < V_{IN} < AVCC + 0.6 V
High Speed Differential Input Voltage	2.0 V
Low Speed Input Voltage	DVEE − 0.3 V < V_{IN} < AMUXVCC + 0.6 V
I^2C Logic Input Voltage	DVEE − 0.3 V < V_{IN} < DVCC + 0.6 V
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions: a device soldered in a 4-layer JEDEC circuit board for surface-mount packages. θ_{JC} is specified for the exposed pad soldered to the circuit board with no airflow.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
56-Lead LFCSP	27	2.1	°C/W

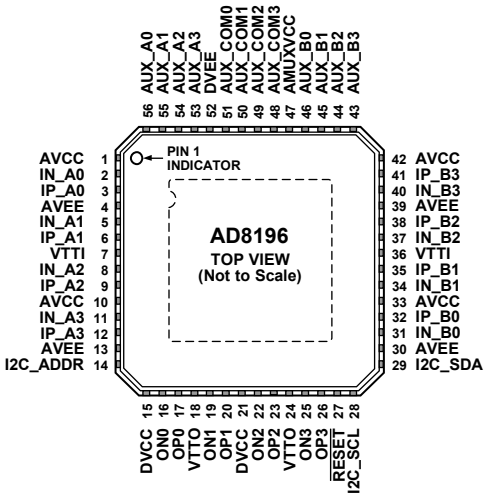
MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8196 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure. To ensure proper operation, it is necessary to observe the maximum power derating as determined by the coefficients in Table 3.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE AD8196 LFCSP HAS AN EXPOSED PADDLE (ePAD) ON THE UNDERSIDE OF THE PACKAGE WHICH AIDS IN HEAT DISSIPATION. THE ePAD MUST BE ELECTRICALLY CONNECTED TO THE AVEE SUPPLY PLANE IN ORDER TO MEET THERMAL SPECIFICATIONS.

06470-003

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1, 10, 33, 42	AVCC	Power	Positive Analog Supply. 3.3 V nominal.
2	IN_A0	HS I	High Speed Input Complement.
3	IP_A0	HS I	High Speed Input.
4, 13, 30, 39, ePAD	AVEE	Power	Negative Analog Supply. 0 V nominal.
5	IN_A1	HS I	High Speed Input Complement.
6	IP_A1	HS I	High Speed Input.
7, 36	VTTI	Power	Input Termination Supply. Nominally connected to AVCC.
8	IN_A2	HS I	High Speed Input Complement.
9	IP_A2	HS I	High Speed Input.
11	IN_A3	HS I	High Speed Input Complement.
12	IP_A3	HS I	High Speed Input.
14	I2C_ADDR	Control	I^2C Address LSB.
15, 21	DVCC	Power	Positive Digital Power Supply. 3.3 V nominal.
16	ON0	HS O	High Speed Output Complement.
17	OP0	HS O	High Speed Output.
18, 24	VTTO	Power	Output Termination Supply. Nominally connected to AVCC.
19	ON1	HS O	High Speed Output Complement.
20	OP1	HS O	High Speed Output.
22	ON2	HS O	High Speed Output Complement.
23	OP2	HS O	High Speed Output.
25	ON3	HS O	High Speed Output Complement.
26	OP3	HS O	High Speed Output.
27	$\overline{\text{RESET}}$	Control	Configuration Registers Reset. This pin is normally pulled up to DVCC.
28	I2C_SCL	Control	I^2C Clock.
29	I2C_SDA	Control	I^2C Data.
31	IN_B0	HS I	High Speed Input Complement.
32	IP_B0	HS I	High Speed Input.

Pin No.	Mnemonic	Type[1]	Description
34	IN_B1	HS I	High Speed Input Complement.
35	IP_B1	HS I	High Speed Input.
37	IN_B2	HS I	High Speed Input Complement.
38	IP_B2	HS I	High Speed Input.
40	IN_B3	HS I	High Speed Input Complement.
41	IP_B3	HS I	High Speed Input.
43	AUX_B3	LS I/O	Low Speed Input/Output.
44	AUX_B2	LS I/O	Low Speed Input/Output.
45	AUX_B1	LS I/O	Low Speed Input/Output.
46	AUX_B0	LS I/O	Low Speed Input/Output.
47	AMUXVCC	Power	Positive Auxiliary Switch Supply. 5 V typical.
48	AUX_COM3	LS I/O	Low Speed Common Input/Output.
49	AUX_COM2	LS I/O	Low Speed Common Input/Output.
50	AUX_COM1	LS I/O	Low Speed Common Input/Output.
51	AUX_COM0	LS I/O	Low Speed Common Input/Output.
52	DVEE	Power	Negative Digital and Auxiliary Switch Power Supply. 0 V nominal.
53	AUX_A3	LS I/O	Low Speed Input/Output.
54	AUX_A2	LS I/O	Low Speed Input/Output.
55	AUX_A1	LS I/O	Low Speed Input/Output.
56	AUX_A0	LS I/O	Low Speed Input/Output.

[1] HS = high speed, LS = low speed, I = input, O = output.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 27°C, AVCC = 3.3 V, VTTI = 3.3 V, VTTO = 3.3 V, DVCC = 3.3 V, AMUXVCC = 5 V, AVEE = 0 V, DVEE = 0 V, differential input swing = 1000 mV, TMDS outputs terminated with external 50 Ω resistors to 3.3 V, pattern = PRBS $2^7 - 1$, data rate = 2.25 Gbps, unless otherwise noted.

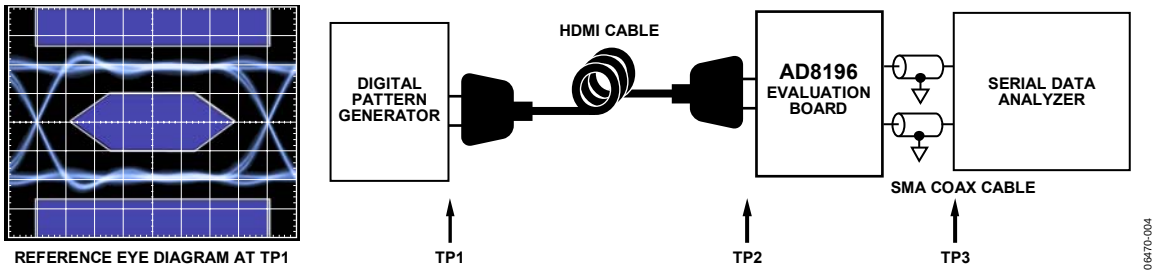


Figure 4. Test Circuit Diagram for RX Eye Diagrams

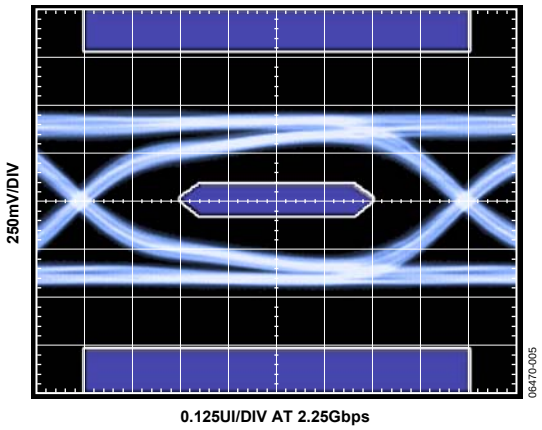


Figure 5. RX Eye Diagram at TP2 (Cable = 2 m, 30 AWG)

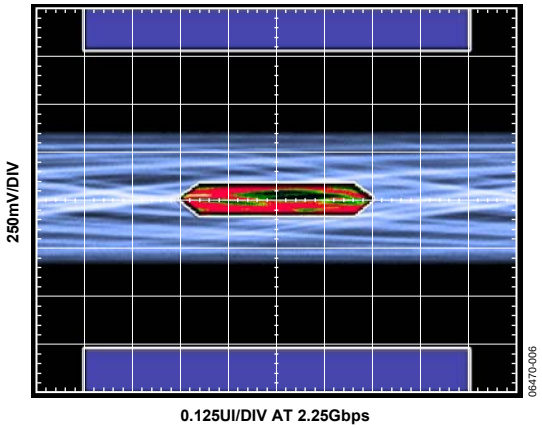


Figure 6. RX Eye Diagram at TP2 (Cable = 20 m, 24 AWG)

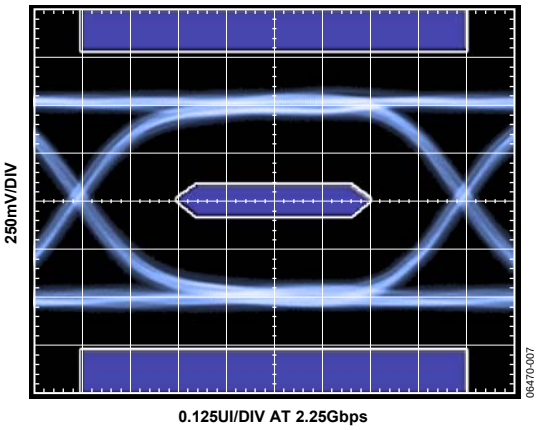


Figure 7. RX Eye Diagram at TP3, EQ = 6 dB (Cable = 2 m, 30 AWG)

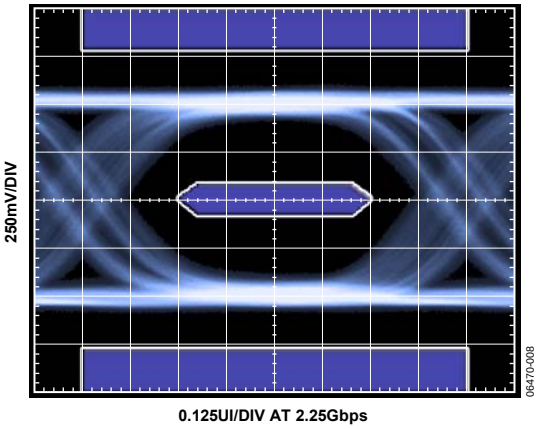


Figure 8. RX Eye Diagram at TP3, EQ = 12 dB (Cable = 20 m, 24 AWG)

T_A = 27°C, AVCC = 3.3 V, VTTI = 3.3 V, VTTO = 3.3 V, DVCC = 3.3 V, AMUXVCC = 5 V, AVEE = 0 V, DVEE = 0 V, differential input swing = 1000 mV, TMDS outputs terminated with external 50 Ω resistors to 3.3 V, pattern = PRBS $2^7 - 1$, data rate = 2.25 Gbps, unless otherwise noted.

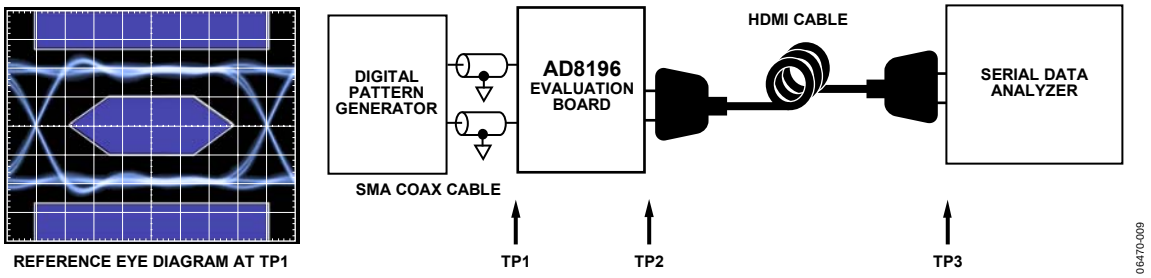


Figure 9. Test Circuit Diagram for TX Eye Diagram

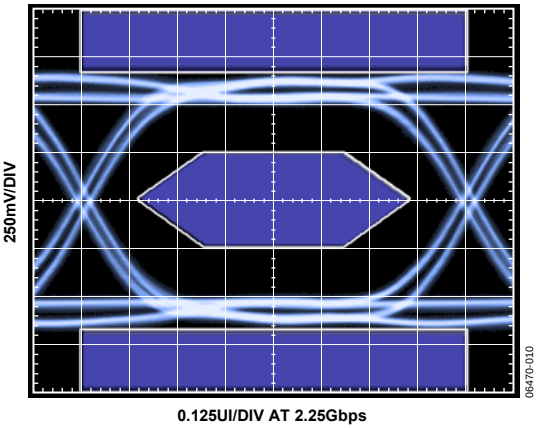


Figure 10. TX Eye Diagram at TP2, PE = 2 dB

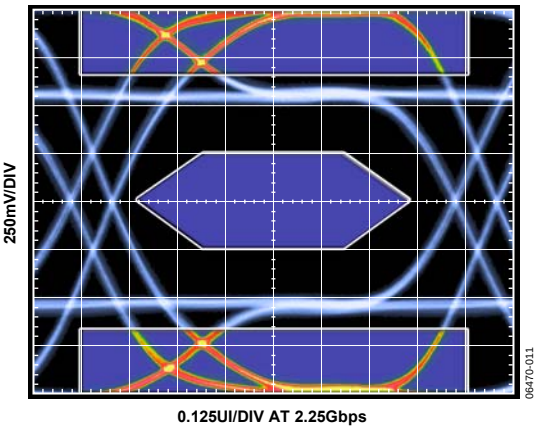


Figure 11. TX Eye Diagram at TP2, PE = 6 dB

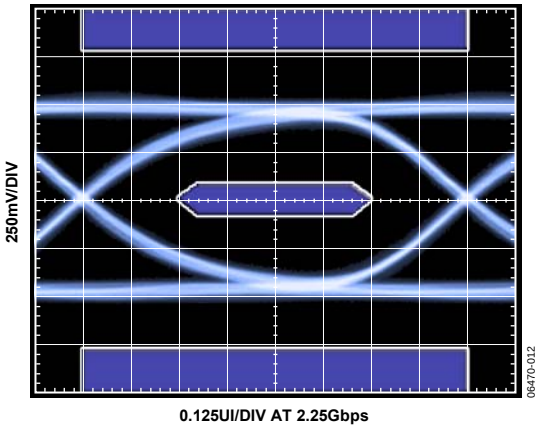


Figure 12. TX Eye Diagram at TP3, PE = 2 dB (Cable = 2 m, 30 AWG)

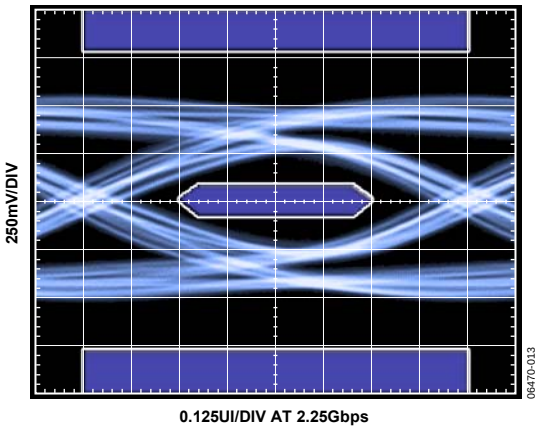


Figure 13. TX Eye Diagram at TP3, PE = 6 dB (Cable = 10 m, 28 AWG)

T_A = 27°C, AVCC = 3.3 V, VTTI = 3.3 V, VTTO = 3.3 V, DVCC = 3.3 V, AMUXVCC = 5 V, AVEE = 0 V, DVEE = 0 V, differential input swing = 1000 mV, TMDS outputs terminated with external 50 Ω resistors to 3.3 V, pattern = PRBS $2^7 - 1$, data rate = 2.25 Gbps, unless otherwise noted.

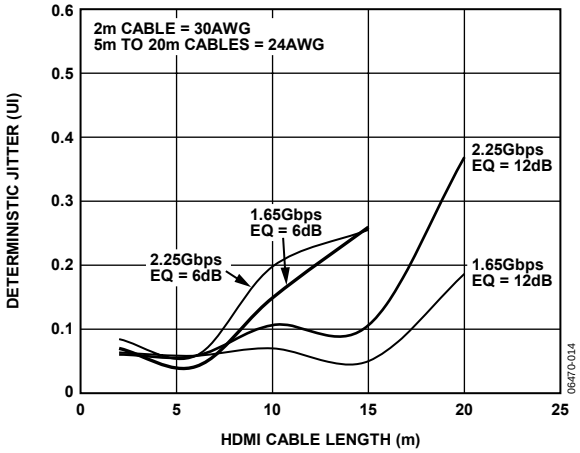


Figure 14. Jitter vs. Input Cable Length (See Figure 4 for Test Setup)

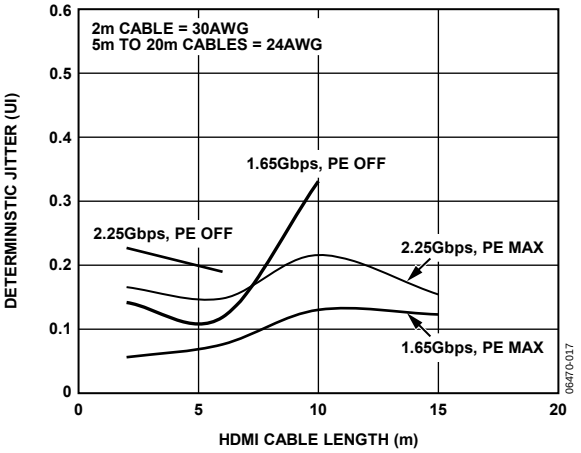


Figure 17. Jitter vs. Output Cable Length (See Figure 9 for Test Setup)

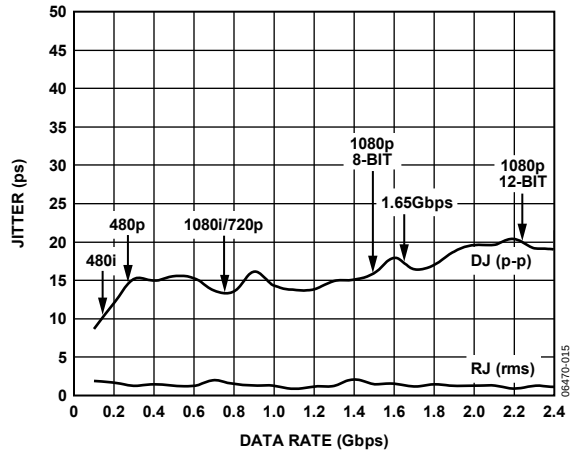


Figure 15. Jitter vs. Data Rate

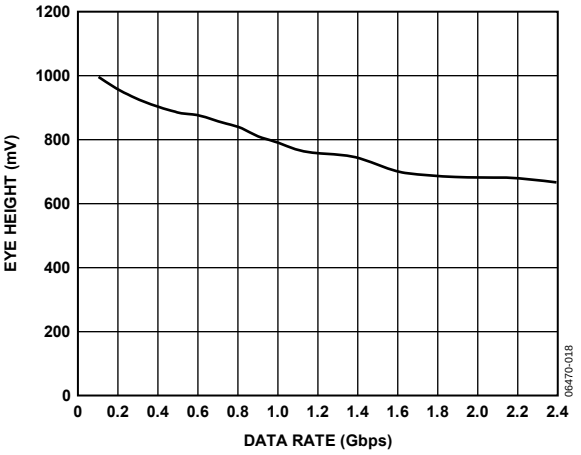


Figure 18. Eye Height vs. Data Rate

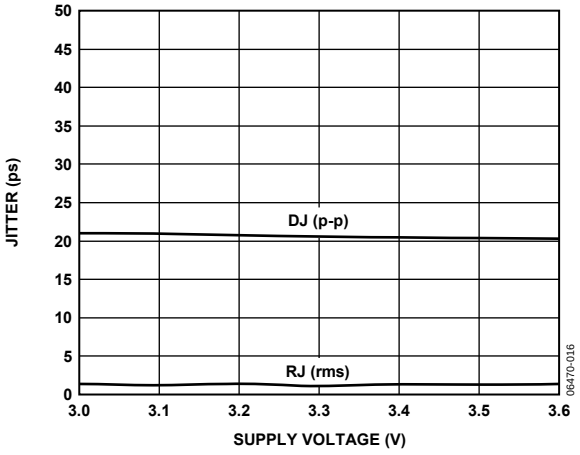


Figure 16. Jitter vs. Supply Voltage

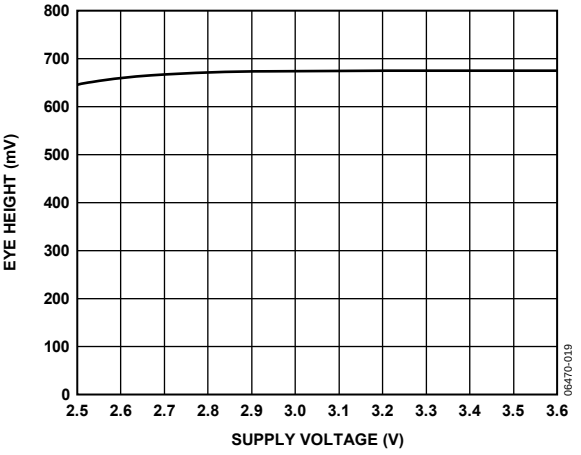


Figure 19. Eye Height vs. Supply Voltage

T_A = 27°C, AVCC = 3.3 V, VTTI = 3.3 V, VTTO = 3.3 V, DVCC = 3.3 V, AMUXVCC = 5 V, AVEE = 0 V, DVEE = 0 V, differential input swing = 1000 mV, TMDS outputs terminated with external 50 Ω resistors to 3.3 V, pattern = PRBS $2^7 - 1$, data rate = 2.25 Gbps, unless otherwise noted.

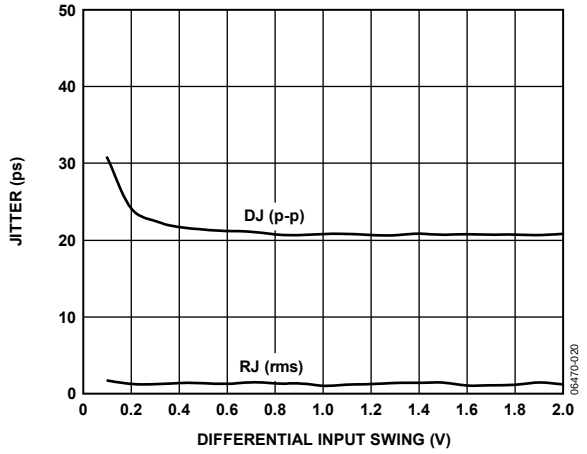


Figure 20. Jitter vs. Differential Input Swing

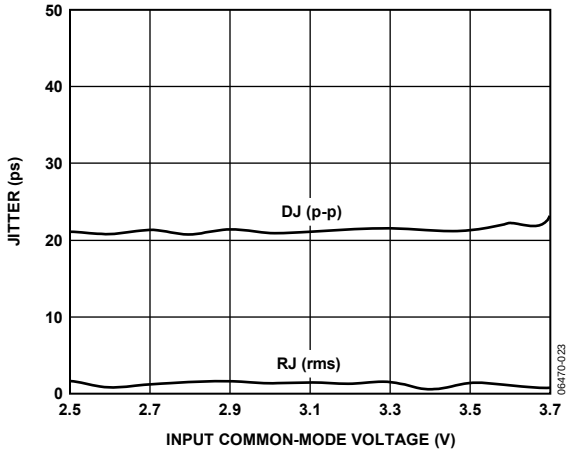


Figure 23. Jitter vs. Input Common-Mode Voltage

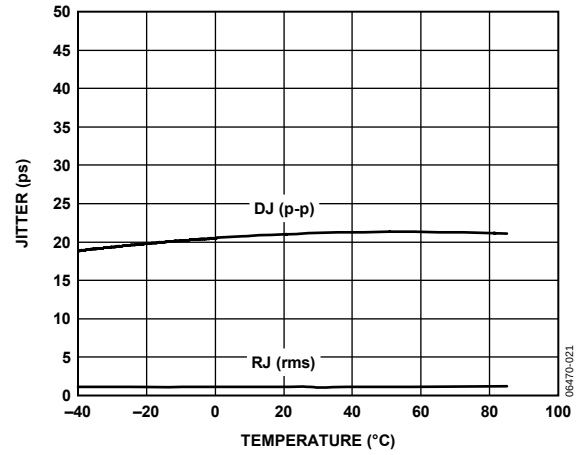


Figure 21. Jitter vs. Temperature

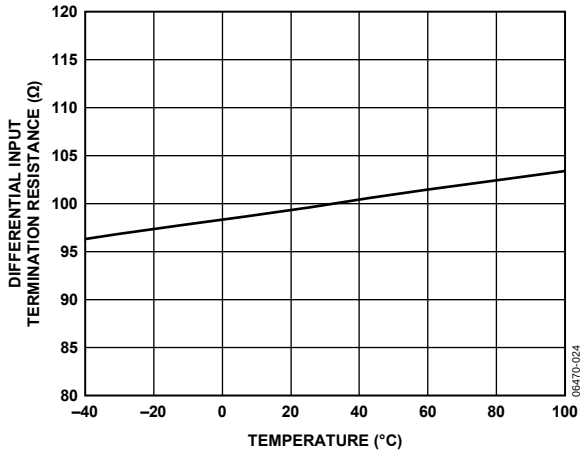


Figure 24. Differential Input Termination Resistance vs. Temperature

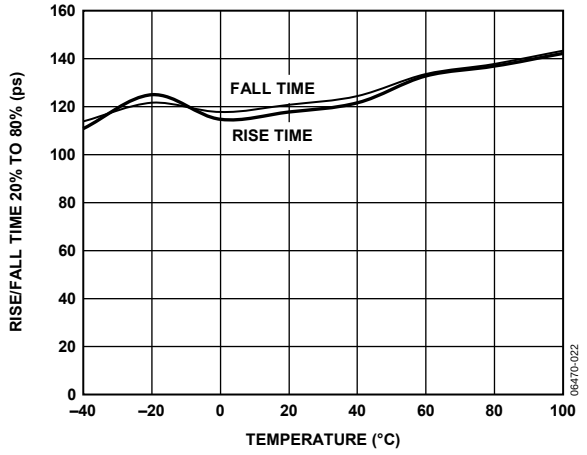


Figure 22. Rise and Fall Time vs. Temperature

THEORY OF OPERATION

INTRODUCTION

The AD8196 is a pin-to-pin HDMI 1.3 receive-compliant replacement for the AD8190. The primary function of the AD8196 is to switch one of two (DVI or HDMI) single link sources to one output. Each HDMI/DVI link consists of four differential, high speed channels and four auxiliary single-ended, low speed control signals. The high speed channels include a data-word clock and three transition minimized differential signaling (TMDS) data channels running at 10× the data-word clock frequency for data rates up to 2.25 Gbps. The four low speed control signals are 5 V tolerant bidirectional lines that can carry configuration signals, HDCP encryption, and other information, depending upon the specific application.

All four high speed TMDS channels in a given link are identical; that is, the pixel clock can be run on any of the four TMDS channels. Transmit and receive channel compensation is provided for the high speed channels where the user can (manually) select among a number of fixed settings.

The AD8196 has I²C serial programming with two user programmable I²C slave addresses. The I²C slave address of the AD8196 is 0b100100X. The least significant bit, represented by X in the address, is set by tying the I2C_ADDR pin to either 3.3 V (for the value, X = 1) or to 0 V (for X = 0).

INPUT CHANNELS

Each high speed input differential pair terminates to the 3.3 V VTTI power supply through a pair of single-ended 50 Ω on-chip resistors, as shown in Figure 25. The input terminations can be optionally disconnected for approximately 100 ms following a source switch. The user can program which of the eight high speed input channels employs this feature by selectively programming the associated RX_PT bits in the input termination pulse register. Additionally, all the input terminations can be disconnected by programming the RX_TO bit in the receiver settings register. By default, the input termination is enabled.

The input equalizer can be manually configured to provide two different levels of high frequency boost: 6 dB or 12 dB. The user can individually control the equalization level of the eight high speed input channels by selectively programming the associated RX_EQ bits in the receive equalizer register. No specific cable length is suggested for a particular equalization setting because cable performance varies widely between manufacturers; however, in general, the equalization of the AD8196 can be set to 12 dB without degrading the signal integrity, even for short input cables. At the 12 dB setting, the AD8196 can equalize more than 20 meters of 24 AWG cable at data rates of 2.25 Gbps.

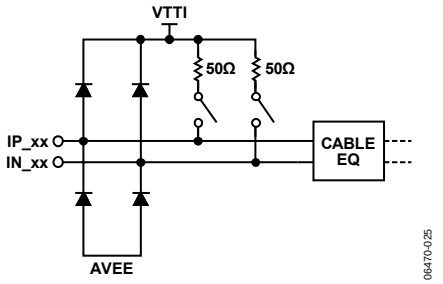


Figure 25. High Speed Input Simplified Schematic

OUTPUT CHANNELS

Each high speed output differential pair is terminated to the 3.3 V VTTO power supply through two single-ended 50 Ω on-chip resistors (see Figure 26). This output termination is user-selectable; all the output terminations can be turned on or off by programming the TX_PTO bit of the transmitter settings register.

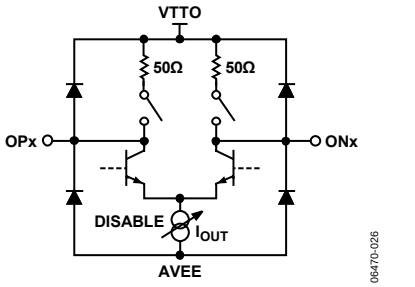


Figure 26. High Speed Output Simplified Schematic

The output termination resistors of the AD8196 back-terminate the output TMDS transmission lines. These back-terminations, as recommended in the HDMI 1.3 specification, act to absorb reflections from impedance discontinuities on the output traces, improving the signal integrity of the output traces and adding flexibility to how the output traces can be routed. For example, interlayer vias can be used to route the AD8196 TMDS outputs on multiple layers of the PCB without severely degrading the quality of the output signal.

The AD8196 output has a disable feature that places the outputs in a tristate mode. This mode is enabled by programming the HS_EN bit of the high speed device modes register. Larger wire-OR'ed arrays can be constructed using the AD8196 in this mode.

The AD8196 requires output termination resistors when the high speed outputs are enabled. Termination can be internal and/or external. The internal terminations of the AD8196 are enabled by programming the TX_PTO bit of the transmitter settings register (the default upon reset). External terminations can be provided either by on-board resistors or by the input termination resistors of an HDMI/DVI receiver. If both the internal terminations are enabled and external terminations are present, set the output current level to 20 mA by programming the TX_OCL bit of the transmitter settings register (the default

upon reset). If only external terminations are provided (if the internal terminations are disabled), set the output current level to 10 mA by programming the TX_OCL bit of the transmitter settings register. The high speed outputs must be disabled if there are no output termination resistors present in the system.

The output pre-emphasis can be manually configured to provide one of four different levels of high frequency boost. The specific boost level is selected by programming the TX_PE bits of the transmitter settings register. No specific cable length is suggested for a particular pre-emphasis setting because cable performance varies widely between manufacturers.

SWITCHING MODE

The AD8196 behaves like a 2:1 HDMI/DVI link multiplexer by routing groups of four TMDS input channels to the four channel output. In this mode, the user selects the group of high speed source signals (A or B) that is routed to the output by programming the HS_CH bit of the high speeds modes register as shown in Table 7. The group of low speed auxiliary source signals (AUX_A or AUX_B) that is routed to the common output is separately set by programming the AUX_CH bit of the auxiliary device register as shown in Table 9.

AUXILIARY LINES SWITCHING

The auxiliary (low speed) lines have no amplification. They are routed using a passive switch that is bandwidth compatible with standard speed I^2C. The schematic equivalent for this passive connection is shown in Figure 27.

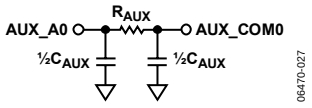


Figure 27. Auxiliary Channel Simplified Schematic Showing AUX_A0 to AUX_COM0 Routing

When turning off the AD8196, care needs to be taken with the AMUXVCC supply to ensure that the auxiliary multiplexer pins are in a high impedance state. A scenario that illustrates this requirement is one where the auxiliary multiplexer is used to switch the display data channel (DDC) bus. In some applications, additional devices can be connected to the DDC bus (such as an EEPROM with EDID information) upstream of the AD8196. Extended display identification data (EDID) is a VESA standard-defined data format for conveying display configuration information to sources to optimize display use. EDID devices may need to be available via the DDC bus, regardless of the state of the AD8196 and any downstream circuit. For this configuration, the auxiliary inputs of the powered down AD8196 need to be in a high impedance state to avoid pulling down on the DDC lines and preventing these other devices from using the bus.

When the AD8196 is powered from a simple resistor network, as shown in Figure 28, it uses the 5 V supply that is required from any HDMI/DVI source to guarantee high impedance of the auxiliary multiplexer pins. The AMUXVCC supply does not draw any static current; therefore, it is recommended that the resistor network tap the 5 V supplies as close to the connectors as possible to avoid any additional voltage drop.

This precaution does not need to be taken if the DDC peripheral circuitry is connected to the bus downstream of the AD8196.

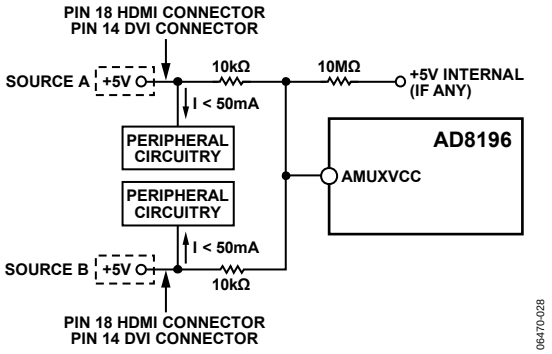


Figure 28. Suggested AMUXVCC Power Scheme

SERIAL CONTROL INTERFACE

RESET

On initial power-up, or at any point in operation, the AD8196 register set can be restored to the default values by pulling the $\overline{\text{RESET}}$ pin to low according to the specification in Table 1. During normal operation, however, the $\overline{\text{RESET}}$ pin must be pulled up to 3.3 V. Pulling the $\overline{\text{RESET}}$ pin to low sets the HS_CH register to 0 (Input A) and incurs the associated switching delay before the input can be switched to Input B, regardless of the previous state of the AD8196.

WRITE PROCEDURE

To write data to the AD8196 register set, an I²C master (such as a microcontroller) needs to send the appropriate control signals to the AD8196 slave device. The signals are controlled by the I²C master, unless otherwise specified. For a diagram of the procedure, see Figure 29. The steps for a write procedure are as follows:

1. Send a start condition (while holding the I2C_SCL line high, pull the I2C_SDA line low).
2. Send the AD8196 part address (seven bits). The upper six bits of the AD8196 part address are the static value [100100] and the LSB is set by Input Pin I2C_ADDR. This transfer should be MSB first.
3. Send the write indicator bit (0).
4. Wait for the AD8196 to acknowledge the request.
5. Send the register address (eight bits) to which data is to be written. This transfer should be MSB first.
6. Wait for the AD8196 to acknowledge the request.
7. Send the data (eight bits) to be written to the register whose address was set in Step 5. This transfer should be MSB first.
8. Wait for the AD8196 to acknowledge the request.
9. Do one of the following:
    a. Send a stop condition (while holding the I2C_SCL line high, pull the I2C_SDA line high) and release control of the bus to end the transaction (shown in Figure 29).
    b. Send a repeated start condition (while holding the I2C_SCL line high, pull the I2C_SDA line low) and continue with Step 2 in this procedure to perform another write.
    c. Send a repeated start condition (while holding the I2C_SCL line high, pull the I2C_SDA line low) and continue with Step 2 of the read procedure (in the Read Procedure section) to perform a read from another address.
    d. Send a repeated start condition (while holding the I2C_SCL line high, pull the I2C_SDA line low) and continue with Step 8 of the read procedure (in the Read Procedure section) to perform a read from the same address set in Step 5.

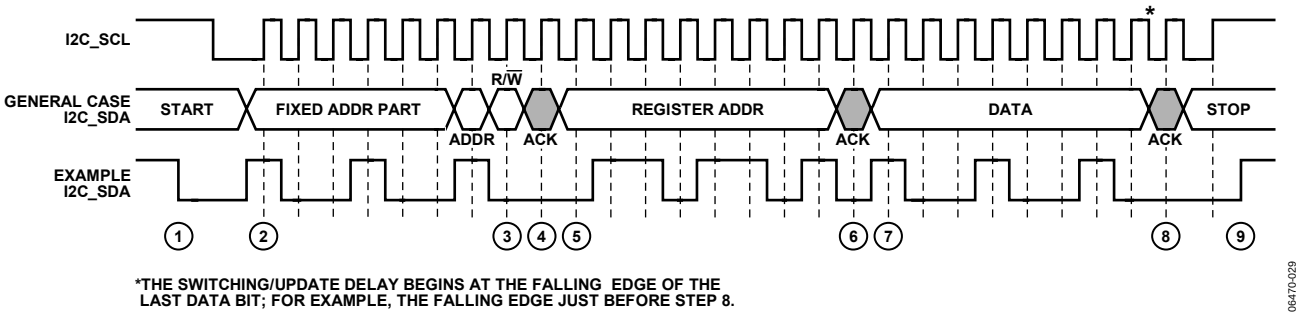


Figure 29. I²C Write Procedure

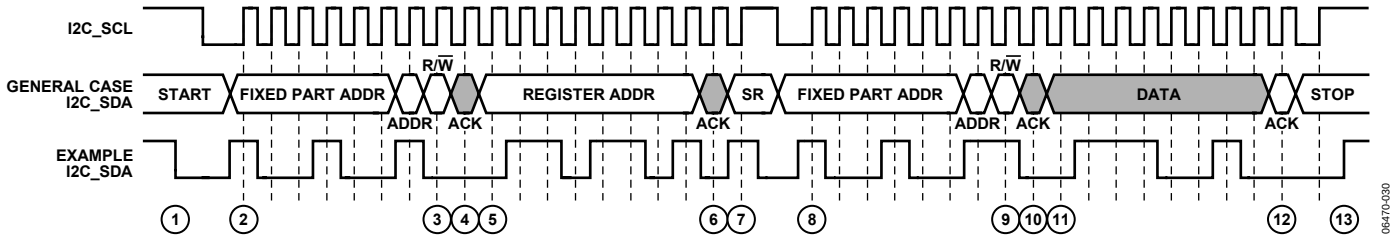


Figure 30. I²C Read Procedure

READ PROCEDURE

To read data from the AD8196 register set, an I²C master (such as a microcontroller) needs to send the appropriate control signals to the AD8196 slave device. The signals are controlled by the I²C master, unless otherwise specified. For a diagram of the procedure, see Figure 30. The steps for a read procedure are as follows:

1. Send a start condition (while holding the I2C_SCL line high, pull the I2C_SDA line low).
2. Send the AD8196 part address (seven bits). The upper six bits of the AD8196 part address are the static value [100100] and the LSB is set by Input Pin I2C_ADDR. This transfer should be MSB first.
3. Send the write indicator bit (0).
4. Wait for the AD8196 to acknowledge the request.
5. Send the register address (eight bits) from which data is to be read. This transfer should be MSB first.
6. Wait for the AD8196 to acknowledge the request.
7. Send a repeated start condition (Sr) by holding the I2C_SCL line high and pulling the I2C_SDA line low.
8. Resend the AD8196 part address (seven bits) from Step 2. The upper six bits of the AD8196 part address compose the static value [100100]. The LSB is set by Input Pin I2C_ADDR. This transfer should be MSB first.
9. Send the read indicator bit (1).
10. Wait for the AD8196 to acknowledge the request.
11. The AD8196 serially transfers the data (eight bits) held in the register indicated by the address set in Step 5. This data is sent MSB first.
12. Acknowledge the data from the AD8196.
13. Do one of the following:
    a. Send a stop condition (while holding the I2C_SCL line high, pull the SDA line high) and release control of the bus to end the transaction (shown in Figure 30).
    b. Send a repeated start condition (while holding the I2C_SCL line high, pull the I2C_SDA line low) and continue with Step 2 of the write procedure (see the previous Write Procedure section) to perform a write.
    c. Send a repeated start condition (while holding the I2C_SCL line high, pull the I2C_SDA line low) and continue with Step 2 of this procedure to perform a read from another address.
    d. Send a repeated start condition (while holding the I2C_SCL line high, pull the I2C_SDA line low) and continue with Step 8 of this procedure to perform a read from the same address.

SWITCHING/UPDATE DELAY

There is a delay between when a user writes to the configuration registers of the AD8196 and when that state change takes physical effect. This update delay begins at the falling edge of I2C_SCL for the last data bit transferred, as shown in Figure 29. This update delay is register specific and the times are specified in Table 1.

During a delay window, new values can be written to the configuration registers but the AD8196 does not physically update until the end of that register's delay window. Writing new values during the delay window does not reset the window; new values supersede the previously written values. At the end of the delay window, the AD8196 physically assumes the state indicated by the last set of values written to the configuration registers. If the configuration registers are written after the delay window ends, the AD8196 immediately updates and a new delay window begins.

CONFIGURATION REGISTERS

The serial interface configuration registers can be read and written using the I²C serial interface, Pin I2C_SDA, and Pin I2C_SCL. The LSB of the AD8196 I²C part address is set by tying Pin I2C_ADDR to 3.3 V (I2C_ADDR = 1) or 0 V (I2C_ADDR = 0).

Table 5. Register Map

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Addr.	Default
High Speed Device Modes		High speed switch enable						High speed source select	0x00	0x40
		HS_EN						HS_CH		
Auxiliary Device Modes		Auxiliary switch enable						Auxiliary switch source select	0x01	0x40
		AUX_EN						AUX_CH		
Receiver Settings								High speed input termination select	0x10	0x01
								RX_TO		
Input Termination Pulse	Input termination pulse-on-source-switch select (disconnect termination for a short period of time)								0x11	0x00
	RX_PT[7]	RX_PT[6]	RX_PT[5]	RX_PT[4]	RX_PT[3]	RX_PT[2]	RX_PT[1]	RX_PT[0]		
Receive Equalizer	Input equalization level select								0x13	0x00
	RX_EQ[7]	RX_EQ[6]	RX_EQ[5]	RX_EQ[4]	RX_EQ[3]	RX_EQ[2]	RX_EQ[1]	RX_EQ[0]		
Transmitter Settings					High speed output pre-emphasis level select		High speed output termination select	High speed output current level select	0x20	0x03
					TX_PE[1]	TX_PE[0]	TX_PTO	TX_OCL		

HIGH SPEED DEVICE MODES REGISTER

HS_EN: High Speed (TMDS) Switch Enable Bit

Table 6. HS_EN Description

HS_EN	Description
0	High speed channels off, low power/standby mode
1	High speed channels on

HS_CH: High Speed (TMDS) Source Select Bit

Table 7. HS_CH Mapping

HS_CH	O[3:0]	Description
0	A[3:0]	High speed Source A switched to output
1	B[3:0]	High speed Source B switched to output

AUXILIARY DEVICE MODES REGISTER

AUX_EN: Auxiliary (Low Speed) Switch Enable Bit

Table 8. AUX_EN Description

AUX_EN	Description
0	Auxiliary switch off, no low speed input/output to low speed common input/output connection
1	Auxiliary switch on

AUX_CH: Auxiliary (Low Speed) Switch Source Select Bit

Table 9. AUX_CH Mapping

AUX_CH	AUX_COM[3:0]	Description
0	AUX_A[3:0]	Auxiliary Source A switched to output
1	AUX_B[3:0]	Auxiliary Source B switched to output

RECEIVER SETTINGS REGISTER

RX_TO: High Speed (TMDS) Input Termination On/Off Select Bit

Table 10. RX_TO Description

RX_TO	Description
0	Input termination off
1	Input termination on (can be pulsed on and off when source is switched, according to settings in the input termination pulse register)

INPUT TERMINATION PULSE REGISTER

RX_PT[X]: High Speed (TMDS) Input Termination X Pulse-On-Source Switch Select Bit

Table 11. RX_PT[X] Description

RX_PT[X]	Description
0	Input termination for TMDS Channel X always connected when source is switched
1	Input termination for TMDS Channel X disconnected for approximately 100 ms when source is switched

Table 12. RX_PT[X] Mapping

RX_PT[X]	Corresponding Input TMDS Channel
Bit 0	A0
Bit 1	A1
Bit 2	A2
Bit 3	A3
Bit 4	B3
Bit 5	B2
Bit 6	B1
Bit 7	B0

RECEIVE EQUALIZER REGISTER

RX_EQ[X]: High Speed (TMDS) Input X Equalization Level Select Bit

Table 13. RX_EQ[X] Description

RX_EQ[X]	Description
0	Low equalization (6 dB)
1	High equalization (12 dB)

Table 14. RX_EQ[X] Mapping

RX_EQ[X]	Corresponding Input TMDS Channel
Bit 0	A0
Bit 1	A1
Bit 2	A2
Bit 3	A3
Bit 4	B3
Bit 5	B2
Bit 6	B1
Bit 7	B0

TRANSMITTER SETTINGS REGISTER

TX_PE[1:0]: High Speed (TMDS) Output Pre-Emphasis Level Select Bus (All TMDS Channels)

Table 15. TX_PE[1:0] Description

TX_PE[1:0]	Description
00	No pre-emphasis (0 dB)
01	Low pre-emphasis (2 dB)
10	Medium pre-emphasis (4 dB)
11	High pre-emphasis (6 dB)

TX_PTO: High Speed (TMDS) Output Termination On/Off Select Bit (All Channels)

Table 16. TX_PTO Description

TX_PTO	Description
0	Output termination off
1	Output termination on

TX_OCL: High Speed (TMDS) Output Current Level Select Bit (All Channels)

Table 17. TX_OCL Description

TX_OCL	Description
0	Output current set to 10 mA
1	Output current set to 20 mA

APPLICATION NOTES

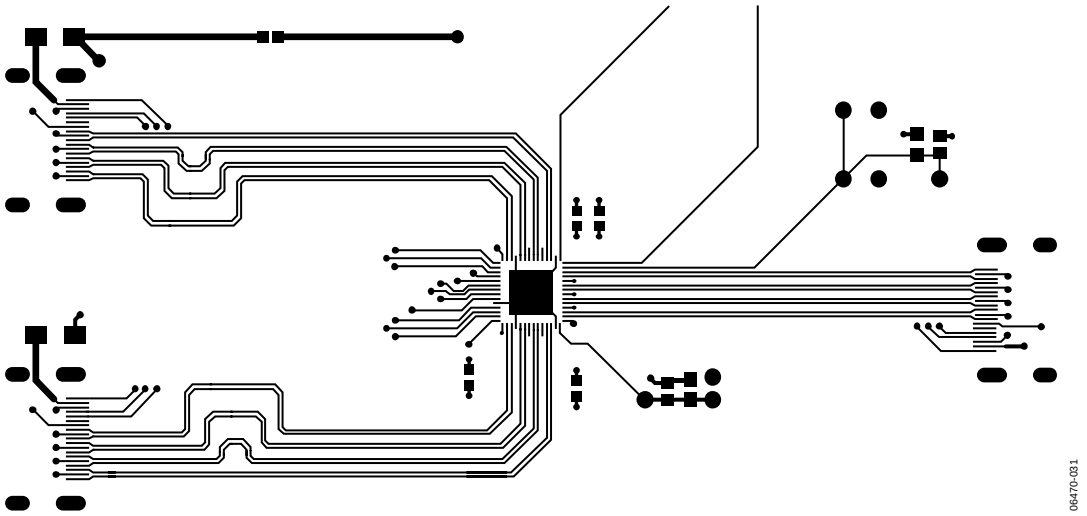


Figure 31. Evaluation Board Layout of the TMDS Traces

The AD8196 is an HDMI/DVI switch featuring equalized TMDS inputs and pre-emphasized TMDS outputs. It is intended for use as a 2:1 switch in systems with long cable runs on both the input and/or the output, and is fully HDMI 1.3 receive-compliant.

PINOUT

The AD8196 is designed to have an HDMI/DVI receiver pinout at its input and a transmitter pinout at its output. This makes the AD8196 ideal for use in AVR-type applications where a designer routes both the inputs and the outputs directly to HDMI/DVI connectors as shown in Figure 31. When the AD8196 is used in receiver-type applications, it is necessary to change the order of the output pins on the PCB to align with the on-board receiver.

One advantage of the AD8196 in an AVR-type application is that all of the high speed signals can be routed on one side (the topside) of the board, as shown in Figure 31. In addition to 12 dB of input equalization, the AD8196 provides up to 6 dB of output pre-emphasis that boosts the output TMDS signals and allows the AD8196 to precompensate when driving long PCB traces or output cables. The net effect of the input equalization and output pre-emphasis of the AD8196 is that the AD8196 can compensate for the signal degradation of both input and output cables; it acts to reopen a closed input data eye and transmit a full swing HDMI signal to an end receiver. More information on the specific performance metrics of the AD8196 can be found in the Typical Performance Characteristics section.

The AD8196 also provides a distinct advantage in receive-type applications because it is a fully buffered HDMI/DVI switch. Although inverting the output pin order of the AD8196 on the PCB requires a designer to place vias in the high speed signal path, the AD8196 fully buffers and electrically decouples the outputs from the inputs. Therefore, the effects of the vias placed on the output signal lines are not seen at the input of the AD8196. The programmable output terminations also improve signal quality at the output of the AD8196. The PCB designer, therefore, has significantly improved flexibility in the placement and routing of the output signal path with the AD8196 over other solutions.

CABLE LENGTHS AND EQUALIZATION

The AD8196 offers two levels of programmable equalization for the high speed inputs: 6 dB and 12 dB. The equalizer of the AD8196 supports video data rates of up to 2.25 Gbps, and as shown in Figure 14, it can equalize more than 20 meters of 24 AWG HDMI cable at 2.25 Gbps, which corresponds to the video format, 1080p with deep color.

The length of cable that can be used in a typical HDMI/DVI application depends on a large number of factors including

- Cable quality: the quality of the cable in terms of conductor wire gauge and shielding. Thicker conductors have lower signal degradation per unit length.
- Data rate: the data rate being sent over the cable. The signal degradation of HDMI cables increases with data rate.
- Edge rates: the edge rates of the source input. Slower input edges result in more significant data eye closure at the end of a cable.
- Receiver sensitivity: the sensitivity of the terminating receiver.

As such, specific cable types and lengths are not recommended for use with a particular equalizer setting. In nearly all applications, the AD8196 equalization level can be set to high, or 12 dB, for all input cable configurations at all data rates, without degrading the signal integrity.

THE AD8196 AS A SINGLE-CHANNEL BUFFER

The AD8196 can be used as a single-channel TMDS buffer without the need for any external I²C control. In its default configuration, the AD8196 connects both the high speed and low speed channels of Input A to their respective outputs, sets the input equalization level to 6 dB, the output pre-emphasis level to 0 dB, enables both the output and input terminations, and provides a fully functioning HDMI link with TMDS buffering.

The AD8196 enters this default state whenever the $\overline{\text{RESET}}$ pin is pulled to low in accordance with the specification in Table 1.

PCB LAYOUT GUIDELINES

The AD8196 is used to switch two distinctly different types of signals, both of which are required for HDMI and DVI video. These signal groups require different treatment when laying out a PC board.

The first group of signals carries the audiovisual (AV) data. HDMI/DVI video signals are differential, unidirectional, and high speed (up to 2.25 Gbps). The channels that carry the video data over the PCB must be controlled impedance, terminated at the receiver, and capable of operating at the maximum specified system data rate. It is especially important to note that the differential traces that carry the TMDS signals should be designed with a controlled differential impedance of 100 Ω. The AD8196 provides single-ended 50 Ω terminations on-chip for both its inputs and outputs, and both the input and output terminations can be enabled or disabled through the serial interface. Transmitter termination is not required by the HDMI 1.3 standard but its inclusion improves the overall system signal integrity.

The audiovisual (AV) data carried on these high speed channels is encoded by a technique called transition minimized differential signaling (TMDS) and in the case of HDMI, is also encrypted according to the high bandwidth digital copy protection (HDCP) standard.

The second group of signals consists of low speed auxiliary control signals used for communication between a source and a sink. Depending upon the application, these signals can include the DDC bus (this is an I²C bus used to send EDID information and HDCP encryption keys between the source and the sink), the consumer electronics control (CEC) line, and the hot plug detect (HPD) line. These auxiliary signals are bidirectional, low speed, and transferred over a single-ended transmission line that does not need to have controlled impedance. The primary concern with laying out the auxiliary lines is ensuring that they conform to the I²C bus standard and do not have excessive capacitive loading.

TMDS Signals

In the HDMI/DVI standard, four differential pairs carry the TMDS signals. In DVI, three of these pairs are dedicated to carrying RGB video and sync data. For HDMI, audio data interleaves with the video data; the DVI standard does not incorporate audio information. The fourth high speed differential pair is used for the AV data-word clock, and runs at one-tenth the speed of the TMDS data channels.

The four high speed channels of the AD8196 are identical. No concession was made to lower the bandwidth of the fourth channel for the pixel clock, so any channel can be used for any TMDS signal. The user chooses which signal is routed over which channel. Additionally, the TMDS channels are symmetrical; therefore, the p and n of a given differential pair are interchangeable, provided the inversion is consistent across all inputs and outputs of the AD8196. However, the routing between inputs and outputs through the AD8196 is fixed. For example, Output Channel 0 always switches between Input A0 and Input B0, and so forth.

The AD8196 buffers the TMDS signals and the input traces can be considered electrically independent of the output traces. In most applications, the quality of the signal on the input TMDS traces are more sensitive to the PCB layout. Regardless of the data being carried on a specific TMDS channel, or whether the TMDS line is at the input or the output of the AD8196, all four high speed signals should be routed on a PCB in accordance with the same RF layout guidelines.

Layout for the TMDS Signals

The TMDS differential pairs can either be microstrip traces, routed on the outer layer of a board, or stripline traces, routed on an internal layer of the board. If microstrip traces are used, there should be a continuous reference plane on the PCB layer directly below the traces. If stripline traces are used, they must be sandwiched between two continuous reference planes in the PCB stack-up. Additionally, the p and n of each differential pair must have a controlled differential impedance of 100 Ω. The characteristic impedance of a differential pair is a function of several variables including the trace width, the distance separating the two traces, the spacing between the traces and the reference plane, and the dielectric constant of the PC board binder material. Interlayer vias introduce impedance discontinuities that can cause reflections and jitter on the signal path, therefore, it is preferable to route the TMDS lines exclusively on one layer of the board, particularly for the input traces. Additionally, to prevent unwanted signal coupling and interference, route the TMDS signals away from other signals and noise sources on the PCB.

Both traces of a given differential pair must be equal in length to minimize intrapair skew. Maintaining the physical symmetry of a differential pair is integral to ensuring its signal integrity; excessive intrapair skew can introduce jitter through duty cycle distortion (DCD). The p and n of a given differential pair should always be routed together to establish the required 100 Ω differential impedance. Enough space should be left between the differential pairs of a given group so that the n of one pair does not couple to the p of another pair. For example, one technique is to make the interpair distance 4 to 10 times wider than the intrapair spacing.

Any one group of four TMDS channels (Input A, Input B, or the output) should have closely matched trace lengths to minimize interpair skew. Severe interpair skew can cause the data on the four different channels of a group to arrive out of alignment with one another. A good practice is to match the trace lengths for a given group of four channels to within 0.05 inches on FR4 material.

Minimizing intra- and interpair skew becomes increasingly important as data rates increase. Any introduced skew constitutes a correspondingly larger fraction of a bit period at higher data rates.

Though the AD8196 features input equalization and output preemphasis, the length of the TMDS traces should be minimized to reduce overall system signal degradation. Commonly used PC board material such as FR4 is lossy at high frequencies, so long traces on the circuit board increase signal attenuation, resulting in decreased signal swing and increased jitter through intersymbol interference (ISI).

Controlling the Characteristic Impedance of a TMDS Differential Pair

The characteristic impedance of a differential pair depends on a number of variables including the trace width, the distance between the two traces, the height of the dielectric material between the trace and the reference plane below it, and the dielectric constant of the PCB binder material. To a lesser extent, the characteristic impedance also depends upon the trace thickness and the presence of solder mask. There are many combinations that can produce the correct characteristic impedance. Generally, working with the PC board fabricator is required to obtain a set of parameters to produce the desired results.

One consideration is how to guarantee a differential pair with a differential impedance of 100 Ω over the entire length of the trace. One technique to accomplish this is to change the width of the traces in a differential pair based on how closely one trace is coupled to the other. When the two traces of a differential pair are close and strongly coupled, they should have a width that produces a 100 Ω differential impedance. When the traces split apart to go into a connector, for example, and are no longer so strongly coupled, the width of the traces should be increased to yield a differential impedance of 100 Ω in the new configuration.

Ground Current Return

In some applications, it can be necessary to invert the output pin order of the AD8196. This requires a designer to route the TMDS traces on multiple layers of the PCB. When routing differential pairs on multiple layers, it is necessary to also reroute the corresponding reference plane to provide one continuous ground current return path for the differential signals. Standard plated through-hole vias are acceptable for both the TMDS traces and the reference plane. An example of this is illustrated in Figure 32.

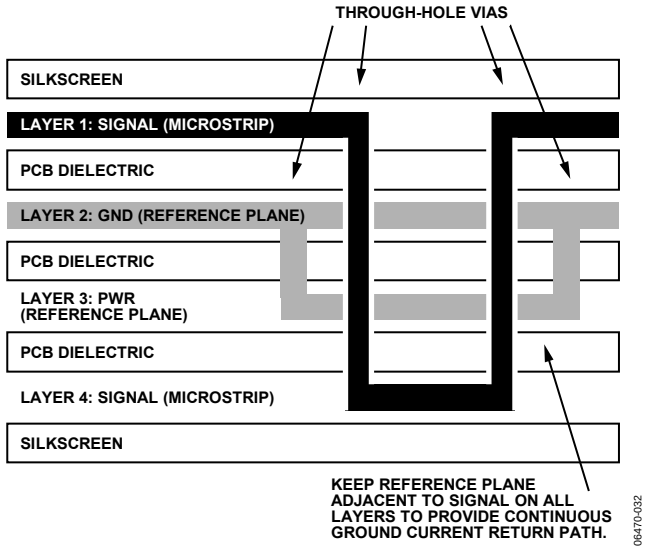


Figure 32. Example Routing of Reference Plane

TMDS Terminations

The AD8196 provides internal 50 Ω single-ended terminations for all of its high speed inputs and outputs. It is not necessary to include external termination resistors for the TMDS differential pairs on the PCB.

The output termination resistors of the AD8196 back-terminate the output TMDS transmission lines. These back-terminations act to absorb reflections from impedance discontinuities on the output traces, improving the signal integrity of the output traces and adding flexibility to how the output traces can be routed. For example, interlayer vias can be used to route the AD8196 TMDS outputs on multiple layers of the PCB without severely degrading the quality of the output signal.

Auxiliary Control Signals

There are four single-ended control signals associated with each source or sink in an HDMI/DVI application. These are hot plug detect (HPD), consumer electronics control (CEC), and two display data channel (DDC) lines. The two signals on the DDC bus are SDA and SCL (serial data and serial clock, respectively). These four signals can be switched through the auxiliary bus of the AD8196 and do not need to be routed with the same strict considerations as the high speed TMDS signals.

In general, it is sufficient to route each auxiliary signal as a single-ended trace. These signals are not sensitive to impedance discontinuities, do not require a reference plane, and can be routed on multiple layers of the PCB. However, it is best to follow strict layout practices whenever possible to prevent the PCB design from affecting the overall application. The specific routing of the HPD, CEC, and DDC lines depends upon the application in which the AD8196 is being used.

For example, the maximum speed of signals present on the auxiliary lines are 100 kHz I^2C data on the DDC lines, therefore, any layout that enables 100 kHz I^2C to be passed over the DDC bus should suffice. The HDMI 1.3 specification, however, places a strict 50 pF limit on the amount of capacitance that can be measured on either SDA or SCL at the HDMI input connector. This 50 pF limit includes the HDMI connector, the PCB, and whatever capacitance is seen at the input of the AD8196, or an equivalent receiver. There is a similar limit of 100 pF of input capacitance for the CEC line.

The parasitic capacitance of traces on a PCB increases with trace length. To help ensure that a design satisfies the HDMI specification, the length of the CEC and DDC lines on the PCB should be made as short as possible. Additionally, if there is a reference plane in the layer adjacent to the auxiliary traces in the PCB stackup, relieving or clearing out this reference plane immediately under the auxiliary traces significantly decreases the amount of parasitic trace capacitance. An example of the board stackup is shown in Figure 33.

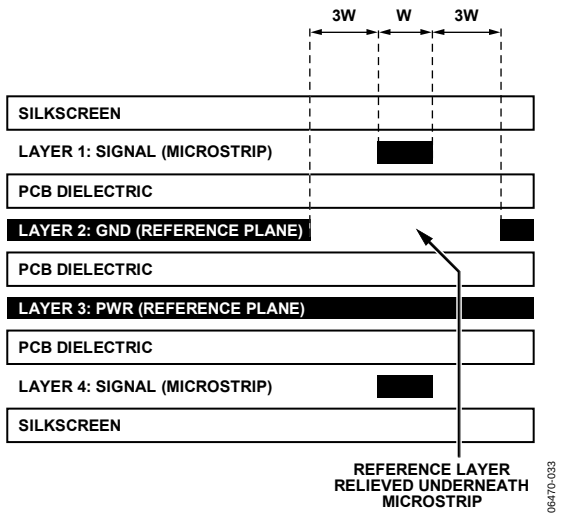


Figure 33. Example Board Stackup

HPD is a dc signal presented by a sink to a source to indicate that the source EDID is available for reading. The placement of this signal is not critical, but it should be routed as directly as possible.

When the AD8196 is powered up, one set of the auxiliary inputs is passively routed to the outputs. In this state, the AD8196 looks like a 100 Ω resistor between the selected auxiliary inputs and the corresponding outputs as illustrated in Figure 27. The AD8196 does not buffer the auxiliary signals, therefore, the input traces, output traces, and the connection through the AD8196 all must be considered when designing a PCB to meet HDMI/DVI specifications. The unselected auxiliary inputs of the AD8196 are placed into a high impedance mode when the device is powered up. To ensure that all of the auxiliary inputs of the AD8196 are in a high impedance mode when the device is powered off, it is necessary to power the AMUXVCC supply as illustrated in Figure 28.

In contrast to the auxiliary signals, the AD8196 buffers the TMDS signals, allowing a PCB designer to layout the TMDS inputs independently of the outputs.

Power Supplies

The AD8196 has five separate power supplies referenced to two separate grounds. The supply/ground pairs are

- AVCC/AVEE
- VTTI/AVEE
- VTTO/AVEE
- DVCC/DVEE
- AMUXVCC/DVEE

The AVCC/AVEE (3.3 V) and DVCC/DVEE (3.3 V) supplies power the core of the AD8196. The VTTI/AVEE supply (3.3 V) powers the input termination (see Figure 25). Similarly, the VTTO/AVEE supply (3.3 V) powers the output termination (see Figure 26). The AMUXVCC/DVEE supply (3.3 V to 5 V) powers the auxiliary multiplexer core and determines the

maximum allowed voltage on the auxiliary lines. For example, if the DDC bus is using 5 V I²C, then AMUXVCC should be connected to +5 V relative to DVEE.

In a typical application, all pins labeled AVEE or DVEE should be connected directly to ground. All pins labeled AVCC, DVCC, VTTI, or VTTO should be connected to 3.3 V, and Pin AMUXVCC tied to 5 V. The supplies can also be powered individually, but care must be taken to ensure that each stage of the AD8196 is powered correctly.

Power Supply Bypassing

The AD8196 requires minimal supply bypassing. When powering the supplies individually, place a 0.01 µF capacitor between each 3.3 V supply pin (AVCC, DVCC, VTTI, and VTTO) and ground to filter out supply noise. Generally, bypass capacitors should be placed near the power pins and should connect directly to the relevant supplies (without long intervening traces). For example, to improve the parasitic inductance of the power supply decoupling capacitors, minimize the trace length between capacitor landing pads and the vias as shown in Figure 34.

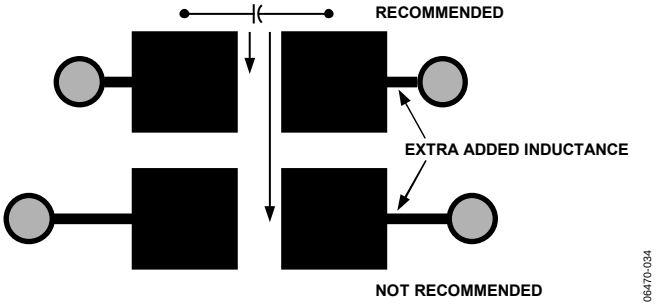


Figure 34. Recommended Pad Outline for Bypass Capacitors

In applications where the AD8196 is powered by a single 3.3 V supply, it is recommended to use two reference supply planes and bypass the 3.3 V reference plane to the ground reference plane with one 220 pF, one 1000 pF, two 0.01 µF, and one 4.7 µF capacitors. The capacitors should via down directly to the supply planes and be placed within a few centimeters of the AD8196. The AMUXVCC supply does not require additional bypassing. This scheme is illustrated in Figure 35.

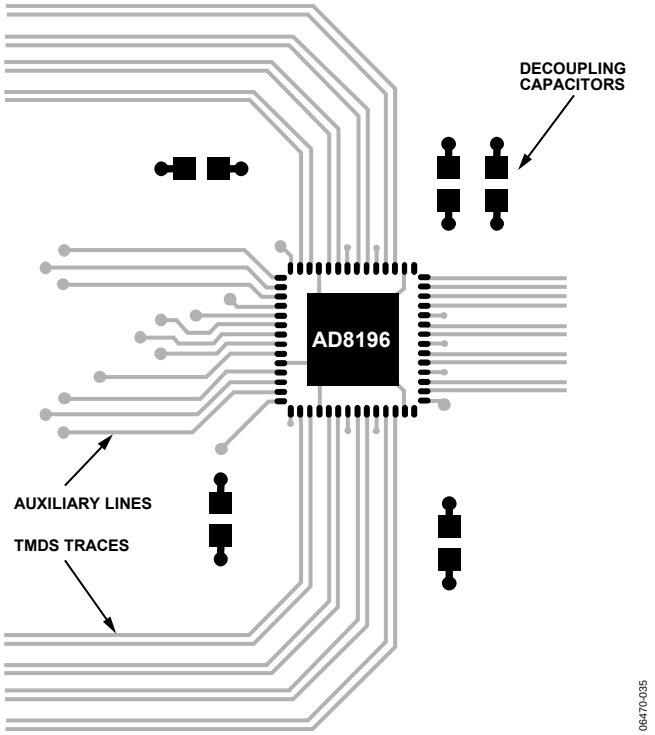
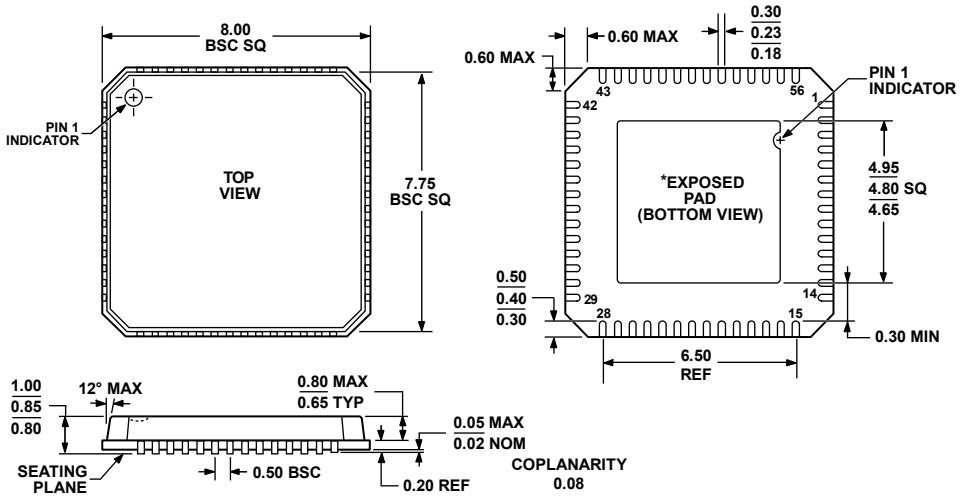


Figure 35. Example Placement of Power Supply Decoupling Capacitors Around the AD8196

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VLLD-2

*NOTE:
THE AD8196 HAS A CONDUCTIVE HEAT SLUG TO HELP DISSIPATE HEAT AND ENSURE RELIABLE OPERATION OF THE DEVICE OVER THE FULL HDMI/DVI TEMPERATURE RANGE. THE SLUG IS EXPOSED ON THE BOTTOM OF THE PACKAGE AND ELECTRICALLY CONNECTED TO AVEE. IT IS RECOMMENDED THAT NO PCB SIGNAL TRACES OR VIAS BE LOCATED UNDER THE PACKAGE THAT COULD COME IN CONTACT WITH THE CONDUCTIVE SLUG. ATTACHING THE SLUG TO AN AVEE PLANE REDUCES THE JUNCTION TEMPERATURE OF THE DEVICE WHICH MAY BE BENEFICIAL IN HIGH TEMPERATURE ENVIRONMENTS.

011907-A

Figure 36. 56-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
8 mm × 8 mm Body, Very Thin Quad
(CP-56-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Ordering Quantity
AD8196ACPZ[1]	−40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-56-3	
AD8196ACPZ-R7[1]	−40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP_VQ], Reel	CP-56-3	750
AD8196ACPZ-RL[1]	−40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP_VQ], Reel	CP-56-3	2500
AD8196-EVAL		Evaluation Board		

[1] Z = Pb-free part.

NOTES

Purchase of licensed I²C components of Analog Devices or one of its sublicensed Associated Companies conveys a license for the purchaser under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

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