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# FDG6316P

## P-Channel 1.8V Specified PowerTrench® MOSFET

### General Description

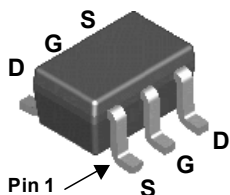
This P-Channel 1.8V specified MOSFET uses Fairchild's advanced low voltage PowerTrench process. It has been optimized for battery power management applications.

### Applications

- Battery management
- Load switch

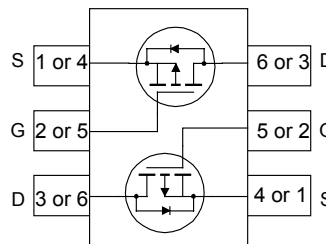
### Features

- -0.7 A, -12 V.  $R_{DS(ON)} = 270 \text{ m}\Omega @ V_{GS} = -4.5 \text{ V}$   
 $R_{DS(ON)} = 360 \text{ m}\Omega @ V_{GS} = -2.5 \text{ V}$   
 $R_{DS(ON)} = 650 \text{ m}\Omega @ V_{GS} = -1.8 \text{ V}$
- Low gate charge
- High performance trench technology for extremely low  $R_{DS(ON)}$
- Compact industry standard SC70-6 surface mount package



**SC70-6**

The pinouts are symmetrical; pin 1 and pin 4 are interchangeable.



### Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain-Source Voltage	-12	V
$V_{GSS}$	Gate-Source Voltage	$\pm 8$	V
$I_D$	Drain Current - Continuous (Note 1)	-0.7	A
	- Pulsed	-1.8	
$P_D$	Power Dissipation for Single Operation (Note 1)	0.3	W
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	415	$^\circ\text{C}/\text{W}$
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### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
.16	FDG6316P	7"	8mm	3000 units

**Electrical Characteristics**T<sub>A</sub> = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
BV <sub>DSS</sub>	Drain–Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = –250 μA	–12			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = –250 μA, Referenced to 25°C		–3.7		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = –10 V, V <sub>GS</sub> = 0 V			–1	μA
I <sub>GSSF</sub>	Gate–Body Leakage, Forward	V <sub>GS</sub> = –8 V, V <sub>DS</sub> = 0 V			–100	nA
I <sub>GSSR</sub>	Gate–Body Leakage, Reverse	V <sub>GS</sub> = 8 V, V <sub>DS</sub> = 0 V			100	nA

**On Characteristics** (Note 2)

V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = –250 μA	–0.4	–0.6	–1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I <sub>D</sub> = –250 μA, Referenced to 25°C		2		mV/°C
R <sub>DS(on)</sub>	Static Drain–Source On–Resistance	V <sub>GS</sub> = –4.5 V, I <sub>D</sub> = –0.7 A V <sub>GS</sub> = –2.5 V, I <sub>D</sub> = –0.5 A V <sub>GS</sub> = –1.8 V, I <sub>D</sub> = –0.4 A V <sub>GS</sub> = –4.5 V, I <sub>D</sub> = –0.7 A, T <sub>J</sub> = 125°C		221 297 427 250	270 360 650 348	mΩ
I <sub>D(on)</sub>	On–State Drain Current	V <sub>GS</sub> = –4.5 V, V <sub>DS</sub> = –5 V	–1.8			A
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = –5 V, I <sub>D</sub> = –0.7 A		2.5		S

**Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = –6 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz		146		pF
C <sub>oss</sub>	Output Capacitance			60		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			48		pF

**Switching Characteristics** (Note 2)

t <sub>d(on)</sub>	Turn–On Delay Time	V <sub>DD</sub> = –6 V, I <sub>D</sub> = 1 A, V <sub>GS</sub> = –4.5 V, R <sub>GEN</sub> = 6 Ω		5	10	ns
t <sub>r</sub>	Turn–On Rise Time			13	23	ns
t <sub>d(off)</sub>	Turn–Off Delay Time			8	16	ns
t <sub>f</sub>	Turn–Off Fall Time			2	4	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = –6 V, I <sub>D</sub> = –0.7 A, V <sub>GS</sub> = –4.5 V		1.7	2.4	nC
Q <sub>gs</sub>	Gate–Source Charge			0.3		nC
Q <sub>gd</sub>	Gate–Drain Charge			0.4		nC

**Drain–Source Diode Characteristics and Maximum Ratings**

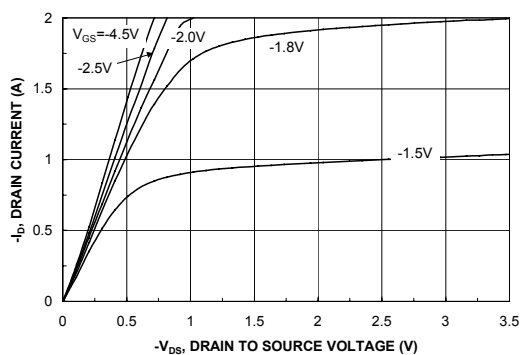
I <sub>S</sub>	Maximum Continuous Drain–Source Diode Forward Current				–0.25	A
V <sub>SD</sub>	Drain–Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = –0.25 A (Note 2)		–0.7	–1.2	V

**Notes:**

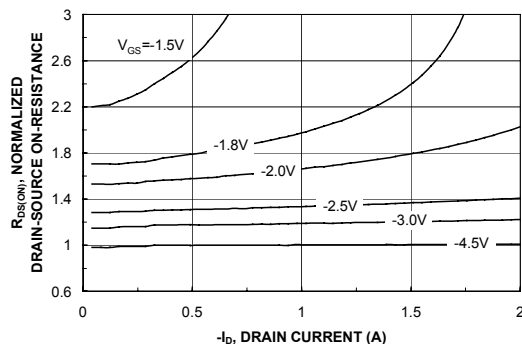
1. R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>θJC</sub> is guaranteed by design while R<sub>θJA</sub> is determined by the user's board design. R<sub>θJA</sub> = 415°C/W when mounted on a minimum pad of FR-4 PCB on still air environment

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%

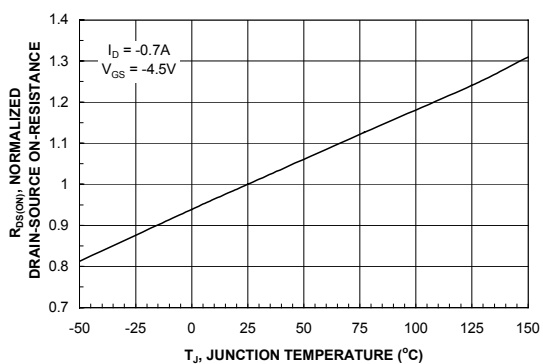
## Typical Characteristics



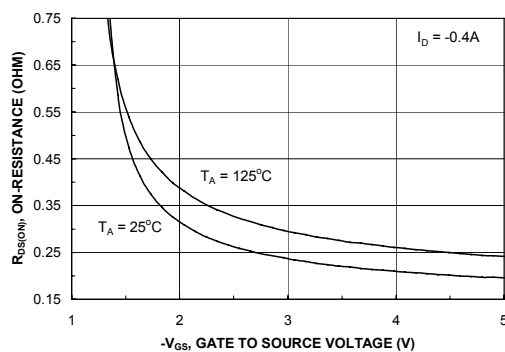
**Figure 1. On-Region Characteristics.**



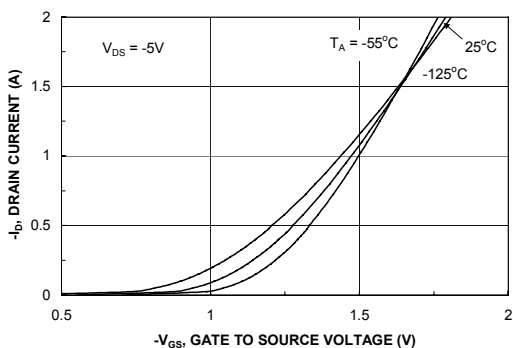
**Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.**



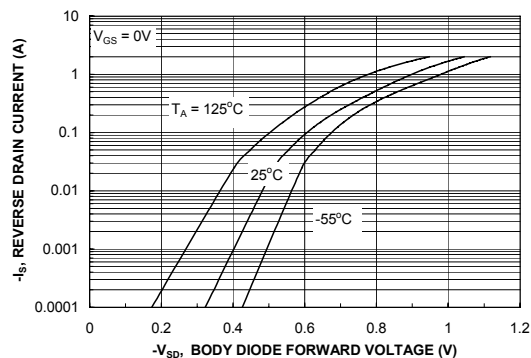
**Figure 3. On-Resistance Variation with Temperature.**



**Figure 4. On-Resistance Variation with Gate-to-Source Voltage.**

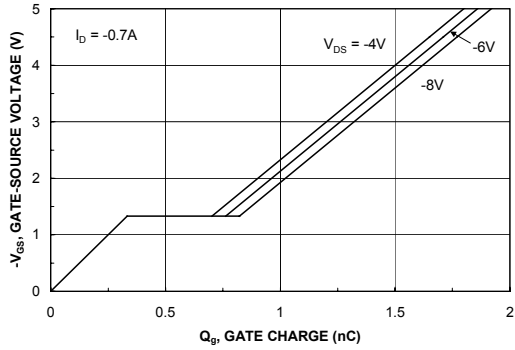


**Figure 5. Transfer Characteristics.**

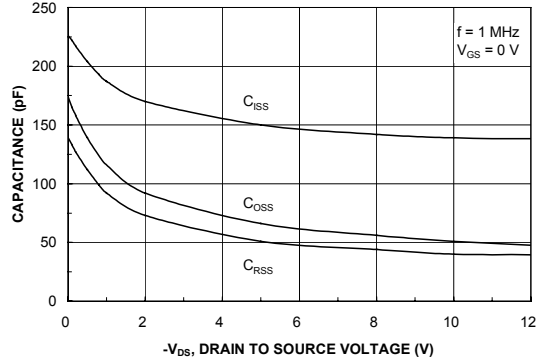


**Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.**

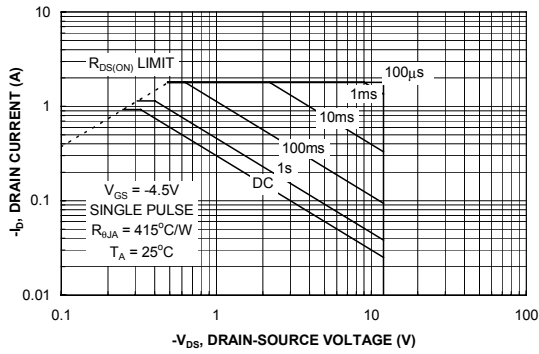
**Typical Characteristics**



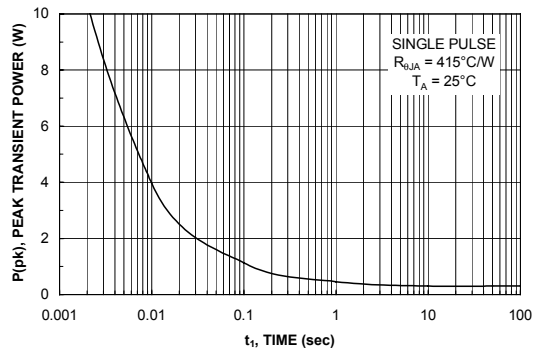
**Figure 7. Gate Charge Characteristics.**



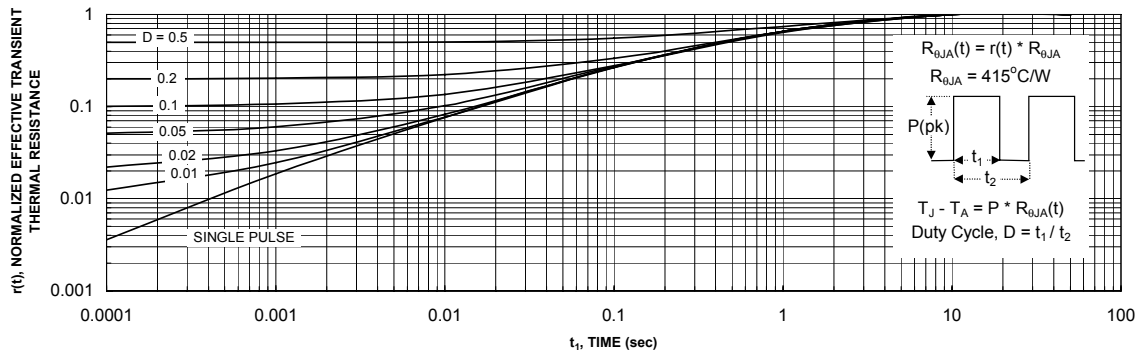
**Figure 8. Capacitance Characteristics.**



**Figure 9. Maximum Safe Operating Area.**



**Figure 10. Single Pulse Maximum Power Dissipation.**



**Figure 11. Transient Thermal Response Curve.**

Thermal characterization performed using the conditions described in Note 1.  
Transient thermal response will change depending on the circuit board design.

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