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FDD8444

N-Channel PowerTrench[®] MOSFET

40V, 50A, 5.2mΩ

Features

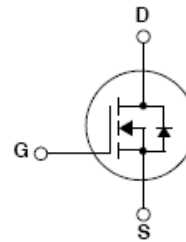
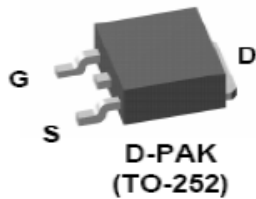
- Typ $r_{DS(on)}$ = 4mΩ at $V_{GS} = 10V$, $I_D = 50A$
- Typ $Q_{g(10)}$ = 89nC at $V_{GS} = 10V$
- Low Miller Charge
- Low Q_{rr} Body Diode
- UIS Capability (Single Pulse/ Repetitive Pulse)
- Qualified to AEC Q101
- RoHS Compliant

Applications

- Automotive Engine Control
- Powertrain Management
- Solenoid and Motor Drivers
- Electronic Transmission
- Distributed Power Architecture and VRMs
- Primary Switch for 12V Systems



FDD8444 N-Channel PowerTrench[®] MOSFET



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	40	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current Continuous ($V_{GS} = 10\text{V}$) (Note 1)	145	A
	Continuous ($V_{GS} = 10\text{V}$, with $R_{\theta JA} = 52^\circ\text{C/W}$)	20	
	Pulsed	Figure 4	
E_{AS}	Single Pulse Avalanche Energy (Note 2)	535	mJ
P_D	Power Dissipation	153	W
	Derate above 25°C	1.02	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature	-55 to +175	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.98	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient TO-252, 1in ² copper pad area	52	$^\circ\text{C/W}$

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD8444	FDD8444	TO-252AA	13"	16mm	2500 units

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

B_{VDSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	40	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 32\text{V}$ $V_{GS} = 0\text{V}$	-	-	1	μA
		$T_J = 150^\circ\text{C}$	-	-	250	
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	2	2.5	4	V
$r_{DS(on)}$	Drain to Source On Resistance	$I_D = 50\text{A}, V_{GS} = 10\text{V}$	-	4	5.2	m Ω
		$I_D = 50\text{A}, V_{GS} = 10\text{V},$ $T_J = 175^\circ\text{C}$	-	7.2	9.4	

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V},$ $f = 1\text{MHz}$	-	6195	-	pF	
C_{oss}	Output Capacitance		-	585	-	pF	
C_{rfs}	Reverse Transfer Capacitance		-	332	-	pF	
R_G	Gate Resistance	$f = 1\text{MHz}$	-	1.9	-	Ω	
$Q_{g(TOT)}$	Total Gate Charge at 10V	$V_{GS} = 0$ to 10V	$V_{DD} = 20\text{V}$ $I_D = 50\text{A}$ $I_g = 1.0\text{mA}$	-	89	116	nC
$Q_{g(5)}$	Total Gate Charge at 5V	$V_{GS} = 0$ to 5V		43	56	nC	
$Q_{g(TH)}$	Threshold Gate Charge	$V_{GS} = 0$ to 2V		-	11	14.3	nC
Q_{gs}	Gate to Source Gate Charge			-	23	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau			-	11	-	nC
Q_{gd}	Gate to Drain "Miller" Charge			-	20	-	nC

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Switching Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
t_{on}	Turn-On Time	$V_{DD} = 20\text{V}, I_D = 50\text{A}$ $V_{GS} = 10\text{V}, R_{GS} = 2\Omega$	-	-	135	ns
$t_{d(on)}$	Turn-On Delay Time		-	12	-	ns
t_r	Turn-On Rise Time		-	78	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	48	-	ns
t_f	Turn-Off Fall Time		-	15	-	ns
t_{off}	Turn-Off Time		-	-	95	ns

Drain-Source Diode Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{SD}	Source to Drain Diode Voltage	$I_{SD} = 50\text{A}$	-	0.9	1.25	V
		$I_{SD} = 25\text{A}$	-	0.8	1.0	
t_{rr}	Reverse Recovery Time	$I_F = 50\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$	-	39	51	ns
Q_{rr}	Reverse Recovery Charge		-	45	59	nC

Notes:

- 1: Package current limitation is 50A.
- 2: Starting $T_J = 25^\circ\text{C}$, $L = 0.67\text{mH}$, $I_{AS} = 40\text{A}$

This product has been designed to meet the extreme test conditions and environment demanded by the automotive industry. For a copy of the requirements, see AEC Q101 at: <http://www.aecouncil.com/>
 All Fairchild Semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

Typical Characteristics

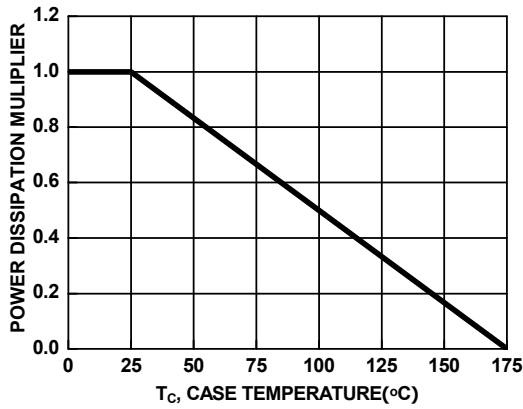


Figure 1. Normalized Power Dissipation vs Case Temperature

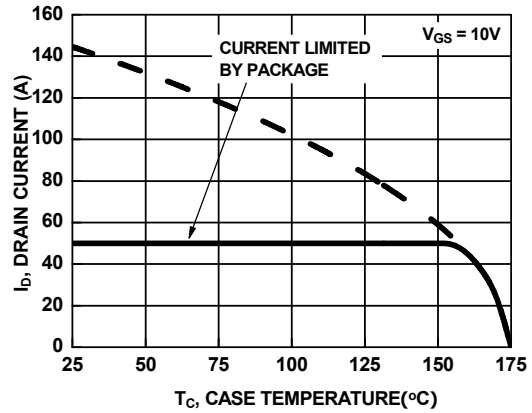


Figure 2. Maximum Continuous Drain Current vs Case Temperature

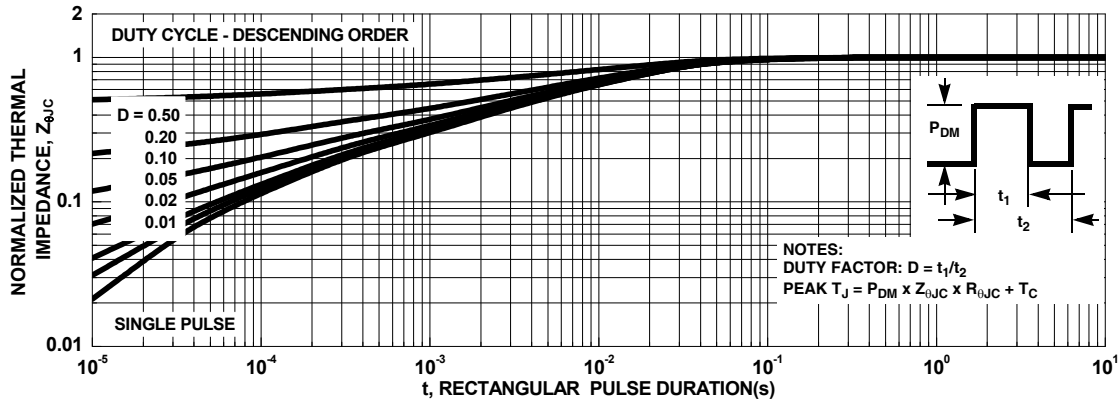


Figure 3. Normalized Maximum Transient Thermal Impedance

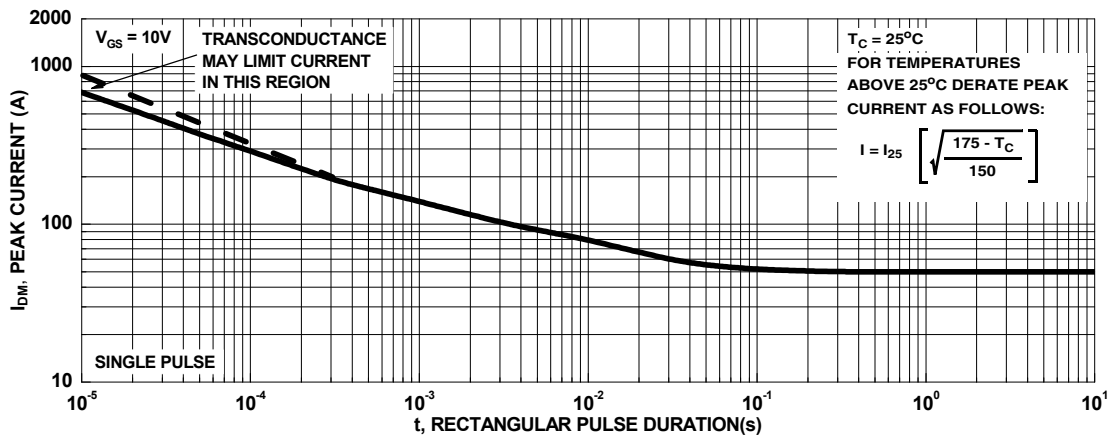


Figure 4. Peak Current Capability

Typical Characteristics

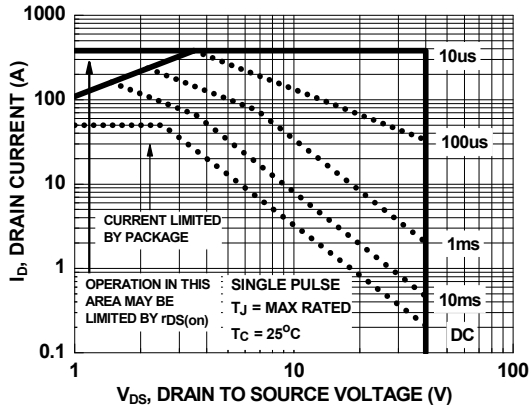
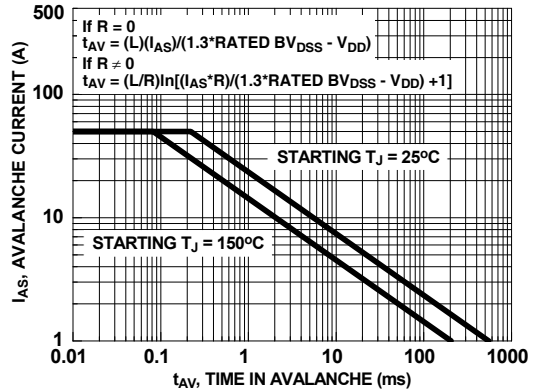


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515
 Figure 6. Unclamped Inductive Switching Capability

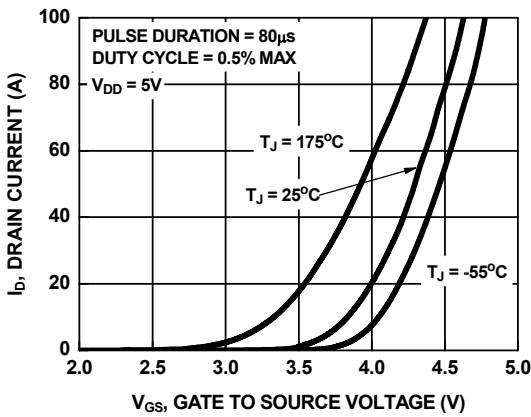


Figure 7. Transfer Characteristics

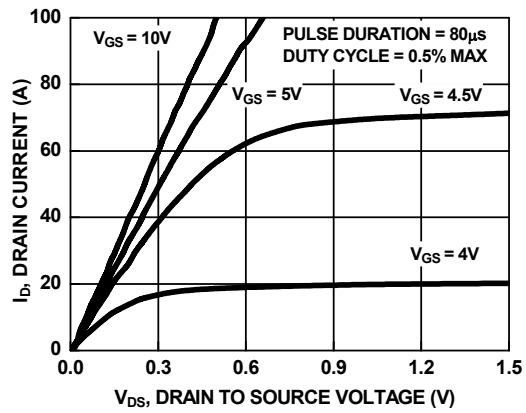


Figure 8. Saturation Characteristics

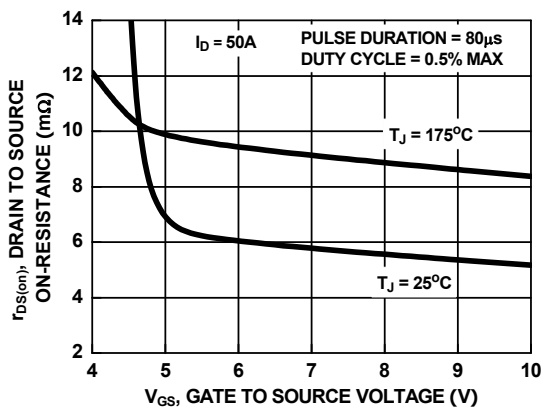


Figure 9. Drain to Source On-Resistance Variation vs Gate to Source Voltage

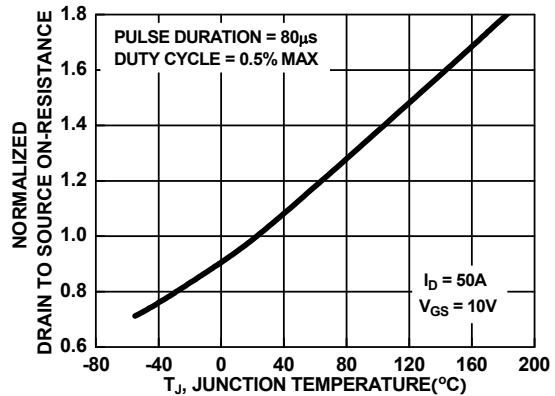


Figure 10. Normalized Drain to Source On-Resistance vs Junction Temperature

Typical Characteristics

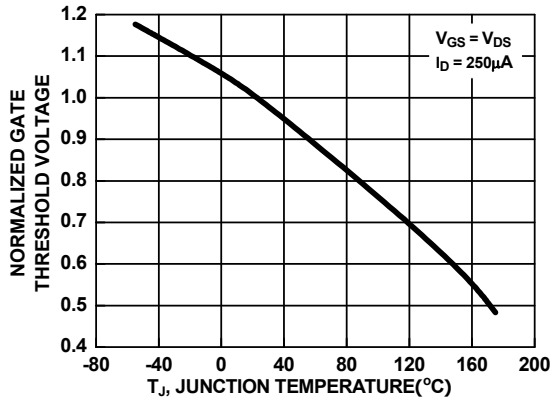


Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

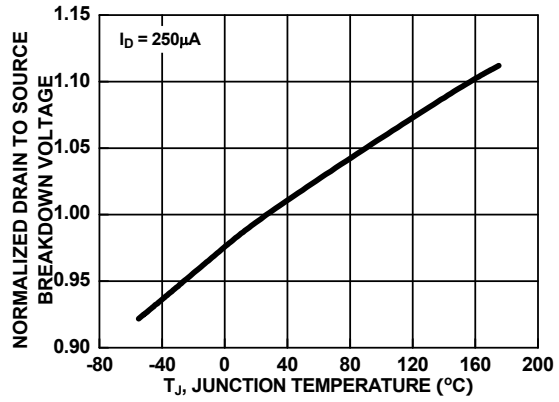


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

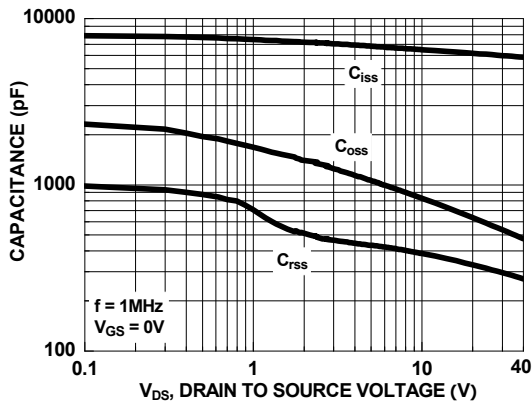


Figure 13. Capacitance vs Drain to Source Voltage

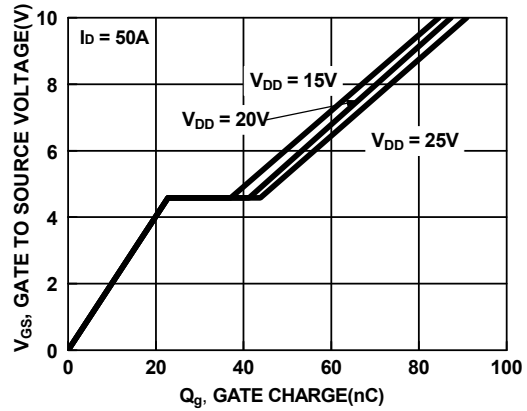
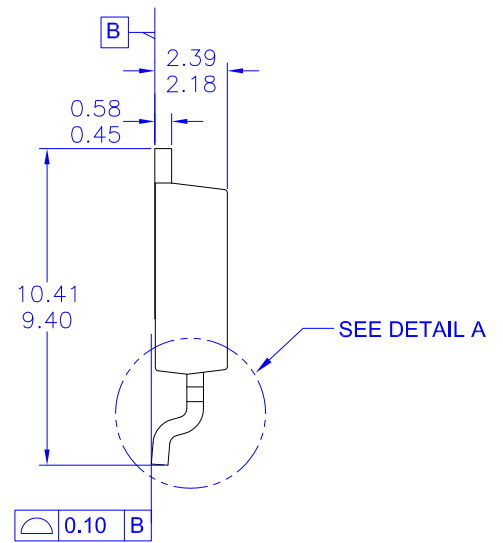
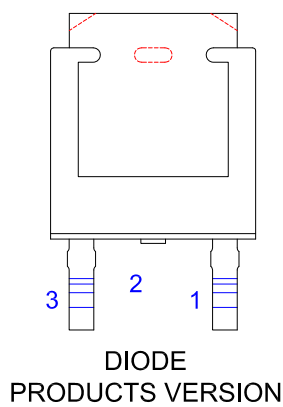
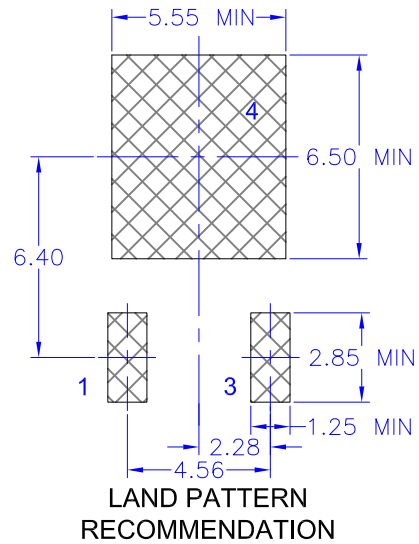
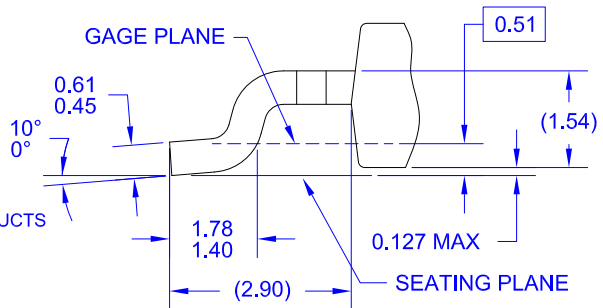


Figure 14. Gate Charge vs Gate to Source Voltage



NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
- E) TRIMMED METAL CENTER LEAD IS PRESENT ON FOR NON-DIODE PRODUCTS
- F) DIMENSIONS ARE EXCLUSIVE OF BURS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.
- H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV11



DETAIL A
(ROTATED -90°)
SCALE: 12X



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