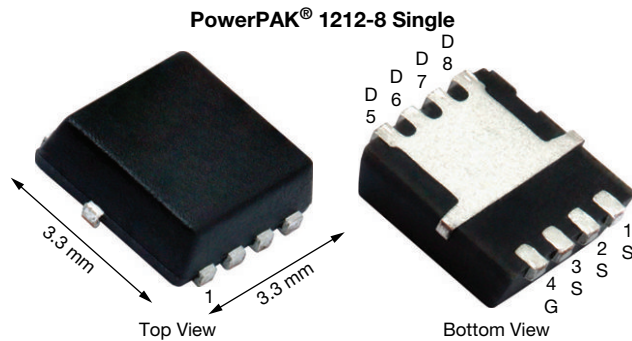


## N-Channel 30 V (D-S) MOSFET



### FEATURES

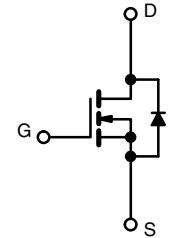
- TrenchFET® Gen IV power MOSFET
- Tuned for reducing transient spikes
- 100 % R<sub>g</sub> and UIS tested
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### APPLICATIONS

- Synchronous buck converter
- High power density DC/DC
- Motor drive control
- Battery management
- Load switch



N-Channel MOSFET

PRODUCT SUMMARY	
V <sub>DS</sub> (V)	30
R <sub>DS(on)</sub> max. (Ω) at V <sub>GS</sub> = 10 V	0.0088
R <sub>DS(on)</sub> max. (Ω) at V <sub>GS</sub> = 4.5 V	0.0120
Q <sub>g</sub> typ. (nC)	9.9
I <sub>D</sub> (A)	16 <sup>a, g</sup>
Configuration	Single

ORDERING INFORMATION	
Package	PowerPAK 1212-Single
Lead (Pb)-free and halogen-free	SiSA96DN-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	V <sub>DS</sub>	30	V	
Gate-source voltage	V <sub>GS</sub>	+20 / -16	V	
Continuous drain current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	16 <sup>a</sup>	A
		T <sub>C</sub> = 70 °C	12 <sup>a</sup>	
		T <sub>A</sub> = 25 °C	14.8 <sup>b, c</sup>	
		T <sub>A</sub> = 70 °C	12 <sup>b, c</sup>	
Pulsed drain current (t = 100 μs)	I <sub>DM</sub>	65	A	
Continuous source-drain diode current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	16 <sup>a</sup>	A
		T <sub>A</sub> = 25 °C	3.2 <sup>b, c</sup>	
Single pulse avalanche current	I <sub>AS</sub>	15	A	
Single pulse avalanche energy	E <sub>AS</sub>	11.25	mJ	
Maximum power dissipation	P <sub>D</sub>	T <sub>C</sub> = 25 °C	26.5	W
		T <sub>C</sub> = 70 °C	17	
		T <sub>A</sub> = 25 °C	3.5 <sup>c</sup>	
		T <sub>A</sub> = 70 °C	2.3 <sup>b, c</sup>	
Operating junction and storage temperature range	T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C	
Soldering recommendations (peak temperature) <sup>c</sup>		260	°C	

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient <sup>b</sup>	R <sub>thJA</sub>	28	35	°C/W
Maximum junction-to-case (drain)	R <sub>thJC</sub>	3.8	4.7	

### Notes

- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 70 °C/W.
- T<sub>C</sub> = 25 °C.



SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	30	-	-	V
Drain-source breakdown voltage (transient) <sup>c</sup>	$V_{DS(t)}$	$V_{GS} = 0\text{ V}, I_{D(aval)} = 15\text{ A}, t_{\text{transient}} = 50\text{ ns}$	36	-	-	V
$V_{DS}$ temperature coefficient	$\Delta V_{DS}/T_J$	$I_D = 10\text{ mA}$	-	13	-	mV/ $^\circ\text{C}$
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250\text{ }\mu\text{A}$	-	-4.7	-	mV/ $^\circ\text{C}$
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1	-	2.2	V
Gate-source leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = +20 / -16\text{ V}$	-	-	100	nA
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 70\text{ }^\circ\text{C}$	-	-	15	$\mu\text{A}$
On-state drain current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 10\text{ V}, V_{GS} = 10\text{ V}$	30	-	-	A
Drain-source on-state resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	-	0.0073	0.0088	$\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$	-	0.0092	0.0120	$\Omega$
Forward transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}, I_D = 10\text{ A}$	-	70	-	S
<b>Dynamic <sup>b</sup></b>						
Input capacitance	$C_{iss}$	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	1385	-	pF
Output capacitance	$C_{oss}$		-	478	-	
Reverse transfer capacitance	$C_{rss}$		-	37	-	
Total gate charge	$Q_g$	$V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	-	20.5	31	nC
		$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$	-	9.9	15	
Gate-source charge	$Q_{gs}$	$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$	-	4.2	-	nC
Gate-drain charge	$Q_{gd}$		-	2.5	-	
Gate resistance	$R_g$	$f = 1\text{ MHz}$	0.2	0.73	1.4	$\Omega$
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 15\text{ V}, R_L = 1.5\text{ }\Omega, I_D \cong 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$	-	8	16	ns
Rise time	$t_r$		-	25	50	
Turn-off delay time	$t_{d(off)}$		-	13	26	
Fall time	$t_f$		-	9	18	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 15\text{ V}, R_L = 1.5\text{ }\Omega, I_D \cong 10\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$	-	12	24	ns
Rise time	$t_r$		-	47	94	
Turn-off delay time	$t_{d(off)}$		-	15	30	
Fall time	$t_f$		-	25	50	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous source-drain diode current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$	-	-	16	A
Pulse diode forward current	$I_{SM}$		-	-	50	
Body diode voltage	$V_{SD}$	$I_S = 5\text{ A}, V_{GS} = 0\text{ V}$	-	0.77	1.1	V
Body diode reverse recovery time	$t_{rr}$	$I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$	-	50	100	ns
Body diode reverse recovery charge	$Q_{rr}$		-	75	150	nC
Reverse recovery fall time	$t_a$		-	43	-	ns
Reverse recovery rise time	$t_b$		-	7	-	

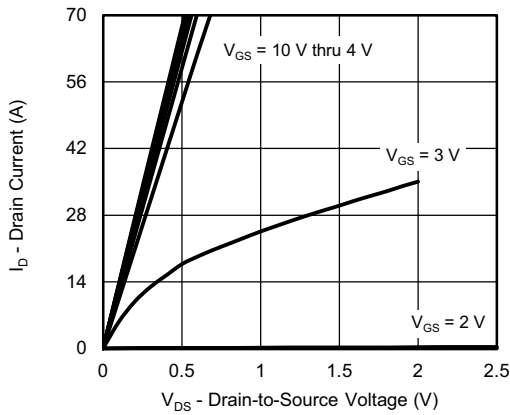
**Notes**

- Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- Guaranteed by design, not subject to production testing.
- $T_{CASE} = 25\text{ }^\circ\text{C}$ . Expected voltage stress during 100% UIS test. Production datalog is not available.

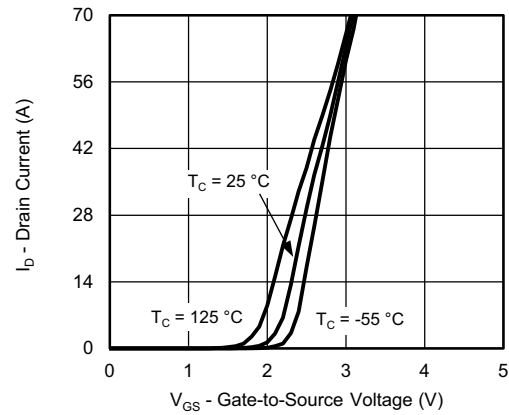
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



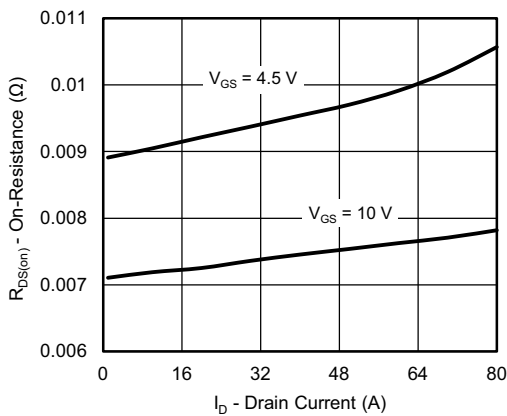
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



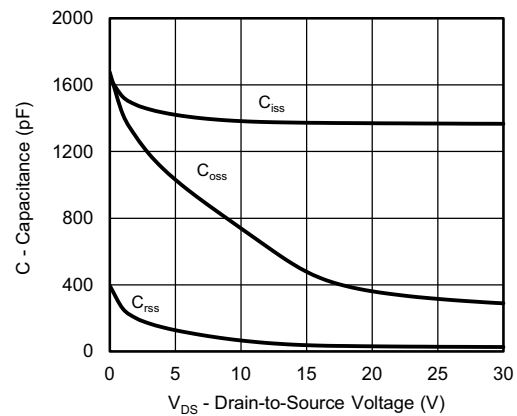
Output Characteristics



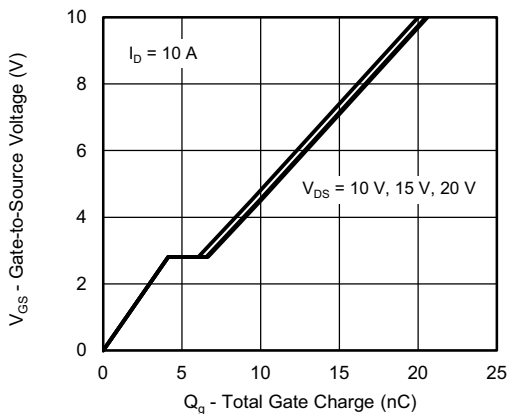
Transfer Characteristics



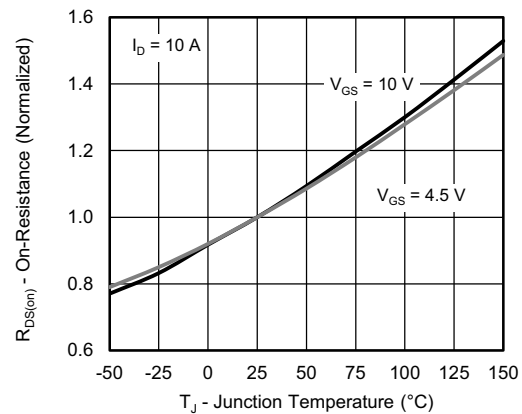
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



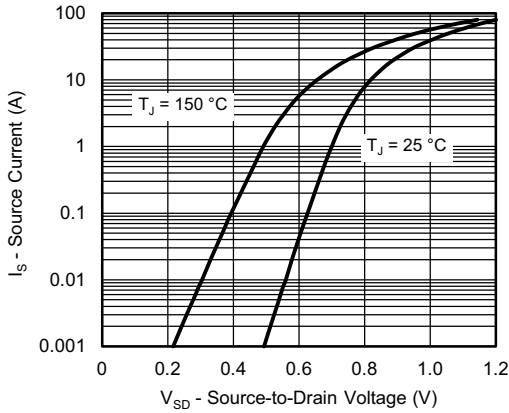
Gate Charge



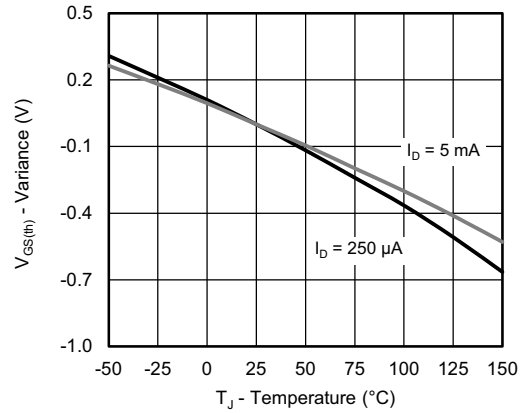
On-Resistance vs. Junction Temperature



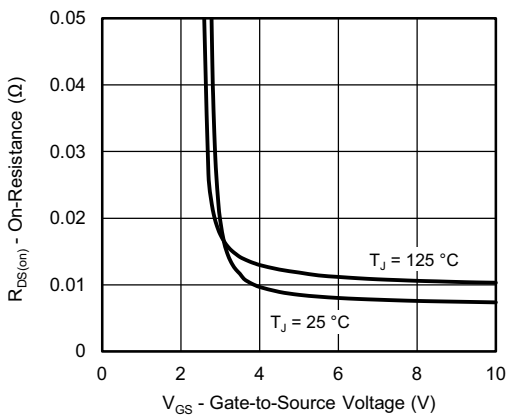
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



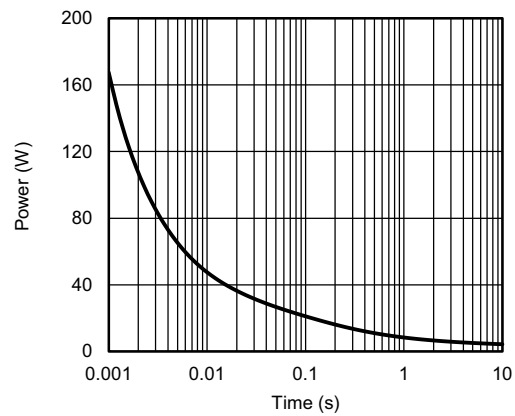
Source-Drain Diode Forward Voltage



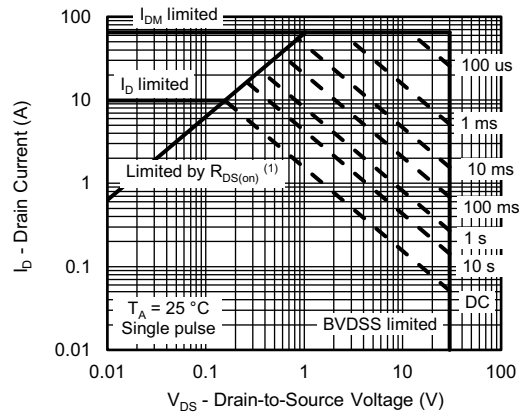
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



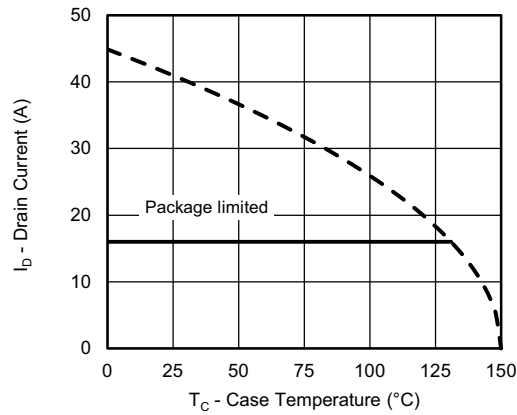
Single Pulse Power, Junction-to-Ambient



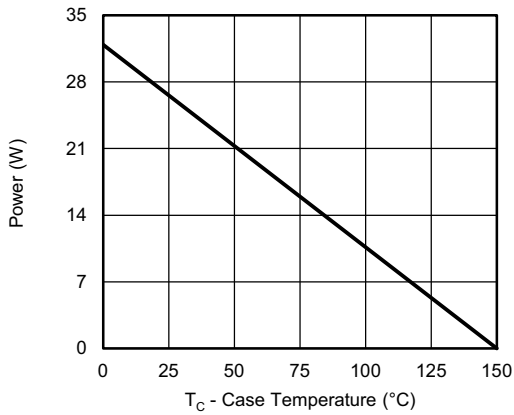
Safe Operating Area, Junction-to-Ambient



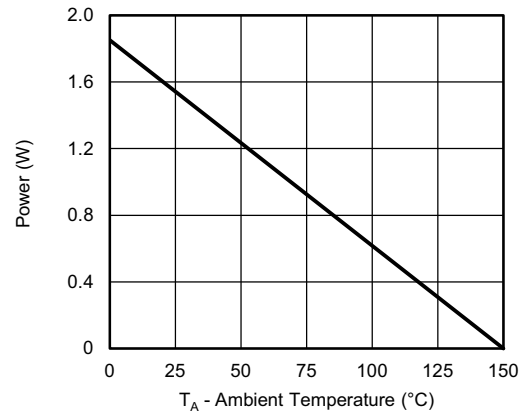
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Current Derating <sup>a</sup>**



**Power, Junction-to-Case**



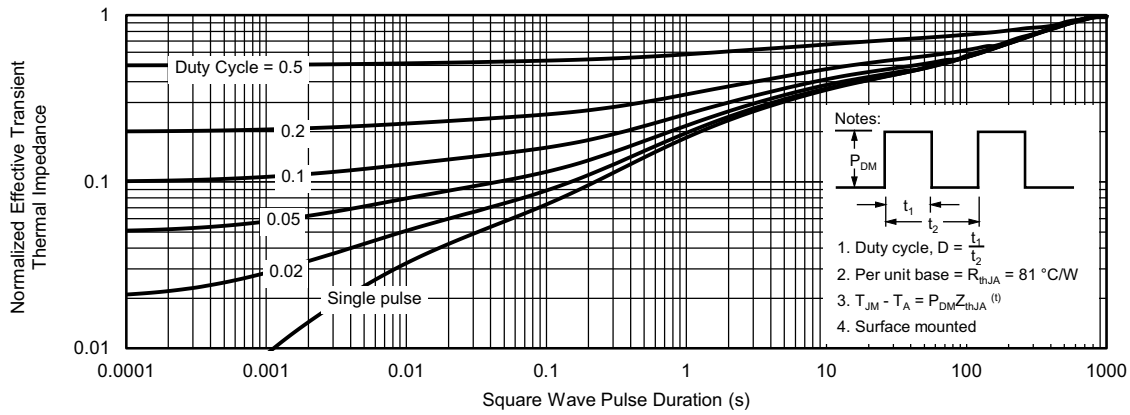
**Power, Junction-to-Ambient**

**Note**

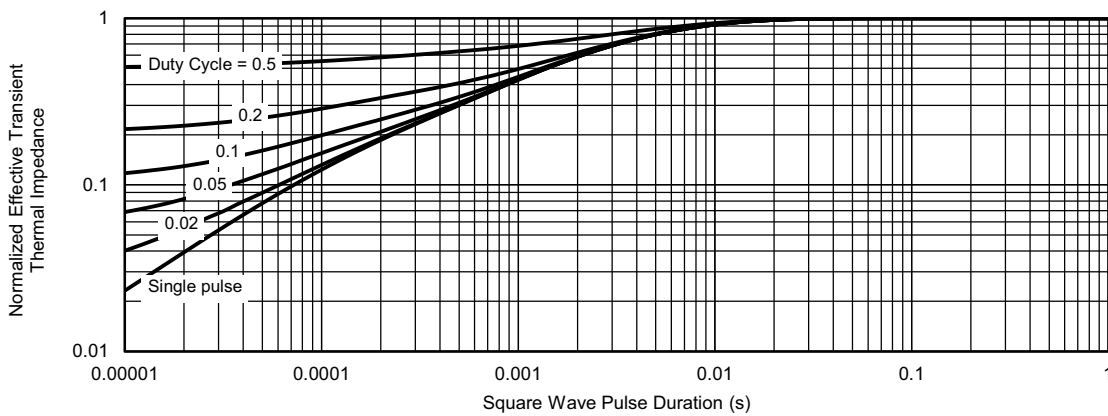
- a. The power dissipation  $P_D$  is based on  $T_J$  max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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