

## Single/Dual Digital Potentiometer with SPI™ Interface

### Features

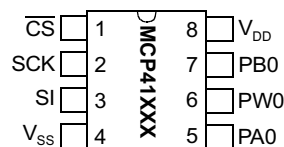
- 256 taps for each potentiometer
- Potentiometer values for 10 kΩ, 50 kΩ and 100 kΩ
- Single and dual versions
- SPI serial interface (mode 0,0 and 1,1)
- +/- 1 LSB max INL & DNL
- Low power CMOS technology
- 1 μA maximum supply current in static operation
- Multiple devices can be daisy-chained together (MCP42XXX only)
- Shutdown feature open circuits of all resistors for maximum power savings
- Hardware shutdown pin available on MCP42XXX only
- Single supply operation (2.7V - 5.5V)
- Industrial temperature range: -40°C to +85°C

### Description

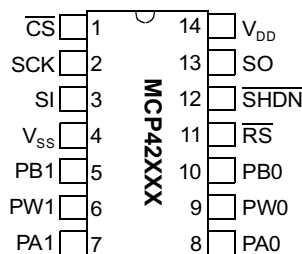
The MCP41XXX and MCP42XXX devices are 256 position digital potentiometers available in 10 kΩ, 50 kΩ, and 100 kΩ resistance versions. The MCP41XXX is a single channel device and is offered in an 8-pin PDIP or SOIC package. The MCP42XXX contains two independent channels in a 14-pin PDIP, SOIC, or TSSOP package. The wiper position of the MCP41XXX/42XXX varies linearly and is controlled via an industry-standard SPI interface. The devices consume <1 μA during static operation. A software shutdown feature is provided that disconnects the "A" terminal from the resistor stack and simultaneously connects the wiper to the "B" terminal. In addition, the dual MCP42XXX has a SHDN pin that performs the same function in hardware. During the shutdown mode, the contents of the wiper register can be changed and the potentiometer returns from shutdown to the new value. The wiper is reset to the mid-scale position, 80h, upon power-up. The RS (reset) pin implements a hardware reset and also returns the wiper to mid-scale. The MCP42XXX SPI interface includes both the SI and SO pins, allowing daisy-chaining of multiple devices. Channel-to-channel resistance matching on the MCP42XXX varies by less than 1%. These devices operate from a single 2.7 - 5.5V supply and are specified over the extended industrial temperature range of -40°C to +85°C.

### Package Types

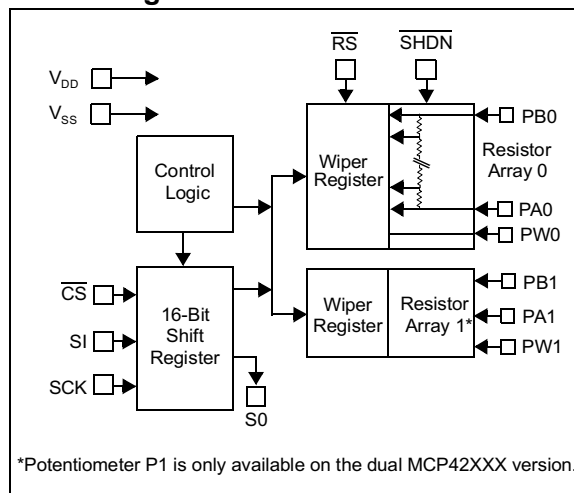
#### PDIP/SOIC



#### PDIP/SOIC/TSSOP



### Block Diagram



# MCP41XXX/42XXX

## 1.0 ELECTRICAL CHARACTERISTICS

### DC CHARACTERISTICS: 10 K $\Omega$ VERSION

All parameters apply across the specified operating ranges unless noted.		Industrial (I): $V_{DD} = +2.7V$ to $5.5V$ , $T_A = -40^{\circ}C$ to $+85^{\circ}C$ (Note 8) Typical specifications represent values for $V_{DD} = 5V$ , $V_{SS} = 0V$ , $V_B = 0V$ , $T_A = +25^{\circ}C$				
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONS
<b>Rheostat Mode</b>						
Nominal Resistance	R	8	10	12	k $\Omega$	$T_A = +25^{\circ}C$ (Note 1)
Rheostat Differential Non Linearity	R-DNL	-1	$\pm 1/4$	+1	LSB	Note 2
Rheostat Integral Non Linearity	R-INL	-1	$\pm 1/4$	+1	LSB	Note 2
Rheostat Tempco	$\Delta R_{AB}/\Delta T$	—	800	—	ppm/ $^{\circ}C$	
Wiper Resistance	$R_W$	—	52	100	$\Omega$	$V_{DD} = 5.5V$ , $I_W = 1mA$ , code 00h
	$R_W$	—	73	125	$\Omega$	$V_{DD} = 2.7V$ , $I_W = 1mA$ , code 00h
Wiper Current	$I_W$	-1	—	+1	mA	
Nominal Resistance Match	$\Delta R/R$	—	0.2	1	%	MCP42010 only, P0 to P1; $T_A = 25^{\circ}C$
<b>Potentiometer Divider</b>						
Resolution	N	8	—	—	Bits	
Monotonicity	N	8	—	—	Bits	
Differential Non Linearity	DNL	-1	$\pm 1/4$	+1	LSB	Note 3
Integral Non Linearity	INL	-1	$\pm 1/4$	+1	LSB	Note 3
Voltage Divider Tempco (Variation between both halves of the voltage divider)	$\Delta V_W/\Delta T$	—	1	—	ppm/ $^{\circ}C$	Code 80h
Full Scale Error	$V_{WFSE}$	-2	-0.7	0	LSB	Code FFh, $V_{DD} = 5V$ (Note 9)
	$V_{WFSE}$	-2	-0.7	0	LSB	Code FFh, $V_{DD} = 3V$ (Note 9)
Zero Scale Error	$V_{WZSE}$	0	+0.7	+2	LSB	Code 00h, $V_{DD} = 5V$ (Note 9)
	$V_{WZSE}$	0	+0.7	+2	LSB	Code 00h, $V_{DD} = 3V$ (Note 9)
<b>Resistor Terminals</b>						
Voltage Range	$V_{A,B,W}$	0	—	$V_{DD}$		Note 4
Capacitance ( $C_A$ or $C_B$ )		—	15	—	pF	$f = 1MHz$ , Code = 80h, see Figure 2-30 for test circuit
Capacitance ( $C_W$ )		—	5.6	—	pF	$f = 1MHz$ , Code = 80h, see Figure 2-30 for test circuit
<b>Dynamic Characteristics (Note 6)</b>						
Bandwidth -3dB	BW	—	1	—	MHz	$V_B = 0V$ , Measured at Code 80h, Output Load = 30 pF
Settling Time	$t_S$	—	2	—	$\mu s$	$V_A = V_{DD}$ , $V_B = 0V$ , $\pm 1\%$ Error Band, Transition from Code 00h to Code 80h, Output Load = 30 pF
Resistor Noise Voltage	$e_{NWB}$	—	9	—	nV/ $\sqrt{Hz}$	$V_A = \text{Open}$ , Code 80h, $f = 1kHz$
Crosstalk	$C_T$	—	-95	—	dB	$V_A = V_{DD}$ , $V_B = 0V$ (Note 5)
<b>Digital Inputs/Outputs (CS, SCK, SI, SO) Note 10</b>						
Schmitt Trigger High Level Input Voltage (All digital input pins)	$V_{IH}$	$0.7V_{DD}$	—	—	V	
Schmitt Trigger Low Level Input Voltage (All digital input pins)	$V_{IL}$	—	—	$0.3V_{DD}$	V	
Hysteresis of Schmitt Trigger Inputs	$V_{HYS}$	—	$0.05V_{DD}$	—		
Low Level Output Voltage	$V_{OL}$	—	—	0.40	V	$I_{OL} = 2.1mA$ , $V_{DD} = 5V$
High Level Output Voltage	$V_{OH}$	$V_{DD} - 0.5$	—	—	V	$I_{OH} = -400\mu A$ , $V_{DD} = 5V$
Input Leakage Current	$I_{LI}$	-1	—	1	$\mu A$	$CS = V_{DD}$ , $V_{IN} = V_{SS}$ or $V_{DD}$ , includes $V_A$ while $SHDN = 0$
Pin Capacitance (All inputs/outputs)	$C_{IN}, C_{OUT}$	—	10	—	pF	$V_{DD} = 5.0V$ , $T_A = +25^{\circ}C$ , $f_c = 1MHz$
<b>Power Requirements</b>						
Operating Voltage Range	$V_{DD}$	2.7	—	5.5	V	
Supply Current, Active	$I_{DDA}$	—	340	500	$\mu A$	$V_{DD} = 5.5V$ , $CS = V_{SS}$ , $f_{SCK} = 10MHz$ , $SO = \text{Open}$ , Code FFh (Note 7)
Supply Current, Static	$I_{DDS}$	—	0.01	1	$\mu A$	$CS, SHDN, RS = V_{DD} = 5.5V$ , $SO = \text{Open}$ (Note 7)
Power Supply Sensitivity	PSS	—	0.0015	0.0035	%/%	$V_{DD} = 4.5V - 5.5V$ , $V_A = 4.5V$ , Code 80h
	PSS	—	0.0015	0.0035	%/%	$V_{DD} = 2.7V - 3.3V$ , $V_A = 2.7V$ , Code 80h

- Note**
- $V_{AB} = V_{DD}$ , no connection on wiper.
  - Rheostat position non linearity R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from the ideal between successive tap positions.  $I_W = 50\mu A$  for  $V_{DD} = 3V$  and  $I_W = 400\mu A$  for  $V_{DD} = 5V$  for 10 k $\Omega$  version. See Figure 2-26 for test circuit.
  - INL and DNL are measured at  $V_W$  with the device configured in the voltage divider or potentiometer mode.  $V_A = V_{DD}$  and  $V_B = 0V$ . DNL specification limits of  $\pm 1$  LSB max are specified monotonic operating conditions. See Figure 2-25 for test circuit.
  - Resistor terminals A, B and W have no restrictions on polarity with respect to each other. Full scale and zero scale error were measured using Figure 2-25.
  - Measured at  $V_W$  pin where the voltage on the adjacent  $V_W$  pin is swinging full scale.
  - All dynamic characteristics use  $V_{DD} = 5V$ .
  - Supply current is independent of current through the potentiometers.
  - TSSOP devices are only specified at  $25^{\circ}C$  and  $85^{\circ}C$ .
  - See Figure 2-25 for test circuit.
  - See Figure 2-12 for RS and SHDN pin operation.

**DC CHARACTERISTICS: 50 KΩ VERSION**

All parameters apply across the specified operating ranges unless noted.		Industrial (I): $V_{DD} = +2.7V$ to $5.5V$ , $T_A = -40^{\circ}C$ to $+85^{\circ}C$ (Note 8) Typical specifications represent values for $V_{DD} = 5V$ , $V_{SS} = 0V$ , $V_B = 0V$ , $T_A = +25^{\circ}C$				
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONS
<b>Rheostat Mode</b>						
Nominal Resistance	R	35	50	65	kΩ	$T_A = +25^{\circ}C$ (Note 1)
Rheostat Differential Non Linearity	R-DNL	-1	$\pm 1/4$	+1	LSB	Note 2
Rheostat Integral Non Linearity	R-INL	-1	$\pm 1/4$	+1	LSB	Note 2
Rheostat Tempco	$\Delta R_{AB}/\Delta T$	—	800	—	ppm/ $^{\circ}C$	
Wiper Resistance	$R_W$	—	125	175	Ω	$V_{DD} = 5.5V$ , $I_W = 1mA$ , code 00h
	$R_W$	—	175	250	Ω	$V_{DD} = 2.7V$ , $I_W = 1mA$ , code 00h
Wiper Current	$I_W$	-1	—	+1	mA	
Nominal Resistance Match	$\Delta R/R$	—	0.2	1	%	MCP42050 only, P0 to P1; $T_A = 25^{\circ}C$
<b>Potentiometer Divider</b>						
Resolution	N	8	—	—	Bits	
Monotonicity	N	8	—	—	Bits	
Differential Non Linearity	DNL	-1	$\pm 1/4$	+1	LSB	$V_{DD} = 5V$ (Note 3)
Integral Non Linearity	INL	-1	$\pm 1/4$	+1	LSB	Note 3
Voltage Divider Tempco (Variation between both halves of the voltage divider)	$\Delta V_W/\Delta T$	—	1	—	ppm/ $^{\circ}C$	Code 80h
Full Scale Error	$V_{WFSE}$	-1	-0.25	0	LSB	Code FFh, $V_{DD} = 5V$ (Note 9)
	$V_{WFSE}$	-1	-0.35	0	LSB	Code FFh, $V_{DD} = 3V$ (Note 9)
Zero Scale Error	$V_{WZSE}$	0	+0.25	+1	LSB	Code 00h, $V_{DD} = 5V$ (Note 9)
	$V_{WZSE}$	0	+0.35	+1	LSB	Code 00h, $V_{DD} = 3V$ (Note 9)
<b>Resistor Terminals</b>						
Voltage Range	$V_{A,B,W}$	0	—	$V_{DD}$		Note 4
Capacitance (CA or CB)		—	11	—	pF	$f = 1MHz$ , Code = 80h, see Figure 2-30 for test circuit
Capacitance (CW)		—	5.6	—	pF	$f = 1MHz$ , Code = 80h, see Figure 2-30 for test circuit
<b>Dynamic Characteristics (Note 6)</b>						
Bandwidth -3dB	BW	—	280	—	kHz	$V_B = 0V$ , Measured at Code 80h, Output Load = 30 pF
Settling Time	$t_s$	—	8	—	μs	$V_A = V_{DD}$ , $V_B = 0V$ , $\pm 1\%$ Error Band, Transition from Code 00h to Code 80h, Output Load = 30 pF
Resistor Noise Voltage	$e_{NWB}$	—	20	—	nV/ $\sqrt{Hz}$	$V_A = \text{Open}$ , Code 80h, $f = 1kHz$
Crosstalk	$C_T$	—	-95	—	dB	$V_A = V_{DD}$ , $V_B = 0V$ (Note 5)
<b>Digital Inputs/Outputs (CS, SCK, SI, SO) Note 10</b>						
Schmitt Trigger High Level Input Voltage (All digital input pins)	$V_{IH}$	$0.7V_{DD}$	—	—	V	
Schmitt Trigger Low Level Input Voltage (All digital input pins)	$V_{IL}$	—	—	$0.3V_{DD}$	V	
Hysteresis of Schmitt Trigger Inputs	$V_{HYS}$	—	$0.05V_{DD}$	—		
Low Level Output Voltage	$V_{OL}$	—	—	0.40	V	$I_{OL} = 2.1mA$ , $V_{DD} = 5V$
High Level Output Voltage	$V_{OH}$	$V_{DD} - 0.5$	—	—	V	$I_{OH} = -400\mu A$ , $V_{DD} = 5V$
Input Leakage Current	$I_{LI}$	-1	—	1	μA	$\overline{CS} = V_{DD}$ , $V_{IN} = V_{SS}$ or $V_{DD}$ , includes $V_A$ while SHDN = 0
Pin Capacitance (All inputs/outputs)	$C_{IN}, C_{OUT}$	—	10	—	pF	$V_{DD} = 5.0V$ , $T_A = +25^{\circ}C$ , $f_c = 1MHz$
<b>Power Requirements</b>						
Operating Voltage Range	$V_{DD}$	2.7	—	5.5	V	
Supply Current, Active	$I_{DDA}$	—	340	500	μA	$V_{DD} = 5.5V$ , $\overline{CS} = V_{SS}$ , $f_{SCK} = 10MHz$ , SO = Open, Code FFh (Note 7)
Supply Current, Static	$I_{DDs}$	—	0.01	1	μA	CS, SHDN, RS = $V_{DD} = 5.5V$ , SO = Open (Note 7)
Power Supply Sensitivity	PSS	—	0.0015	0.0035	%%	$V_{DD} = 4.5V - 5.5V$ , $V_A = 4.5V$ , Code 80h
	PSS	—	0.0015	0.0035	%%	$V_{DD} = 2.7V - 3.3V$ , $V_A = 2.7V$ , Code 80h

Note 1:  $V_{AB} = V_{DD}$ , no connection on wiper.

Note 2: Rheostat position non linearity R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from the ideal between successive tap positions.  $I_W = V_{DD}/R$  for +3V or +5V for the 50 kΩ version. See Figure 2-26 for test circuit.

Note 3: INL and DNL are measured at  $V_W$  with the device configured in the voltage divider or potentiometer mode.  $V_A = V_{DD}$  and  $V_B = 0V$ . DNL specification limits of  $\pm 1$  LSB max are specified monotonic operating conditions. See Figure 2-25 for test circuit.

Note 4: Resistor terminals A,B and W have no restrictions on polarity with respect to each other. Full scale and zero scale error were measured using Figure 2-25.

Note 5: Measured at  $V_W$  pin where the voltage on the adjacent  $V_W$  pin is swinging full scale.

Note 6: All dynamic characteristics use  $V_{DD} = 5V$ .

Note 7: Supply current is independent of current through the potentiometers.

Note 8: TSSOP devices are only specified at  $25^{\circ}C$  and  $85^{\circ}C$ .

Note 9: See Figure 2-25 for test circuit.

Note 10: See Figure 2-12 for RS and SHDN pin operation.

# MCP41XXX/42XXX

## DC CHARACTERISTICS OF 100 KW VERSION

All parameters apply across the specified operating ranges unless noted.		Industrial (I): $V_{DD} = +2.7V$ to $5.5V$ , $T_A = -40^{\circ}C$ to $+85^{\circ}C$ ( <b>Note 8</b> ) Typical specifications represent values for $V_{DD} = 5V$ , $V_{SS} = 0V$ , $V_B = 0V$ , $T_A = +25^{\circ}C$				
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONS
<b>Rheostat Mode</b>						
Nominal Resistance	R	70	100	130	k $\Omega$	$T_A = +25^{\circ}C$ ( <b>Note 1</b> )
Rheostat Differential Non Linearity	R-DNL	-1	$\pm 1/4$	+1	LSB	<b>Note 2</b>
Rheostat Integral Non Linearity	R-INL	-1	$\pm 1/4$	+1	LSB	<b>Note 2</b>
Rheostat Tempco	$\Delta R_{AB}/\Delta T$	—	800	—	ppm/ $^{\circ}C$	
Wiper Resistance	$R_W$	—	125	175	$\Omega$	$V_{DD} = 5.5V$ , $I_W = 1mA$ , code 00h
	$R_W$	—	175	250	$\Omega$	$V_{DD} = 2.7V$ , $I_W = 1mA$ , code 00h
Wiper Current	$I_W$	-1	—	+1	mA	
Nominal Resistance Match	$\Delta R/R$	—	0.2	1	%	MCP42100 only, P0 to P1; $T_A = 25^{\circ}C$
<b>Potentiometer Divider</b>						
Resolution	N	8	—	—	Bits	
Monotonicity	N	8	—	—	Bits	
Differential Non Linearity	DNL	-1	$\pm 1/4$	+1	LSB	$V_{DD} = 5V$ ( <b>Note 3</b> )
Integral Non Linearity	INL	-1	$\pm 1/4$	+1	LSB	<b>Note 3</b>
Voltage Divider Tempco (Variation between both halves of the voltage divider)	$\Delta V_W/\Delta T$	—	1	—	ppm/ $^{\circ}C$	Code 80h
Full Scale Error	$V_{WFSE}$	-1	-0.25	0	LSB	Code FFh, $V_{DD} = 5V$ ( <b>Note 9</b> )
	$V_{WFSE}$	-1	-0.35	0	LSB	Code FFh, $V_{DD} = 3V$ ( <b>Note 9</b> )
Zero Scale Error	$V_{WZSE}$	0	+0.25	+1	LSB	Code 00h, $V_{DD} = 5V$ ( <b>Note 9</b> )
	$V_{WZSE}$	0	+0.35	+1	LSB	Code 00h, $V_{DD} = 3V$ ( <b>Note 9</b> )
<b>Resistor Terminals</b>						
Voltage Range	$V_{A,B,W}$	0	—	$V_{DD}$		<b>Note 4</b>
Capacitance ( $C_A$ or $C_B$ )		—	11	—	pF	$f = 1MHz$ , Code = 80h, see Figure 2-30 for test circuit
Capacitance ( $C_W$ )		—	5.6	—	pF	$f = 1MHz$ , Code = 80h, see Figure 2-30 for test circuit
<b>Dynamic Characteristics (Note 6)</b>						
Bandwidth -3dB	BW	—	145	—	kHz	$V_B = 0V$ , Measured at Code 80h, Output Load = 30 pF
Settling Time	$t_S$	—	18	—	$\mu S$	$V_A = V_{DD}$ , $V_B = 0V$ , $\pm 1\%$ Error Band, Transition from Code 00h to Code 80h, Output Load = 30 pF
Resistor Noise Voltage	$e_{NWB}$	—	29	—	nV/ $\sqrt{Hz}$	$V_A = \text{Open}$ , Code 80h, $f = 1kHz$
Crosstalk	$C_T$	—	-95	—	dB	$V_A = V_{DD}$ , $V_B = 0V$ ( <b>Note 5</b> )
<b>Digital Inputs/Outputs (CS, SCK, SI, SO) Note 10</b>						
Schmitt Trigger High Level Input Voltage (All digital input pins)	$V_{IH}$	$0.7V_{DD}$	—	—	V	
Schmitt Trigger Low Level Input Voltage (All digital input pins)	$V_{IL}$	—	—	$0.3V_{DD}$	V	
Hysteresis of Schmitt Trigger Inputs	$V_{HYS}$	—	$0.05V_{DD}$	—		
Low Level Output Voltage	$V_{OL}$	—	—	0.40	V	$I_{OL} = 2.1mA$ , $V_{DD} = 5V$
High Level Output Voltage	$V_{OH}$	$V_{DD} - 0.5$	—	—	V	$I_{OH} = -400\mu A$ , $V_{DD} = 5V$
Input Leakage Current	$I_{LI}$	-1	—	1	$\mu A$	$CS = V_{DD}$ , $V_{IN} = V_{SS}$ or $V_{DD}$ , includes $V_A$ while $SHDN = 0$
Pin Capacitance (All inputs/outputs)	$C_{IN}$ , $C_{OUT}$	—	10	—	pF	$V_{DD} = 5.0V$ , $T_A = +25^{\circ}C$ , $f_c = 1MHz$
<b>Power Requirements</b>						
Operating Voltage Range	$V_{DD}$	2.7	—	5.5	V	
Supply Current, Active	$I_{DDA}$	—	340	500	$\mu A$	$V_{DD} = 5.5V$ , $CS = V_{SS}$ , $f_{SCK} = 10MHz$ , $SO = \text{Open}$ , Code FFh ( <b>Note 7</b> )
Supply Current, Static	$I_{DDS}$	—	0.01	1	$\mu A$	$CS$ , $SHDN$ , $RS = V_{DD} = 5.5V$ , $SO = \text{Open}$ ( <b>Note 7</b> )
Power Supply Sensitivity	PSS	—	0.0015	0.0035	%/%	$V_{DD} = 4.5V - 5.5V$ , $V_A = 4.5V$ Code 80h
	PSS	—	0.0015	0.0035	%/%	$V_{DD} = 2.7V - 3.3V$ , $V_A = 2.7V$ Code 80h

- Note**
- $V_{AB} = V_{DD}$ , no connection on wiper.
  - Rheostat position non linearity R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from the ideal between successive tap positions.  $I_W = V_{DD}/R$  for +3V or +5V for the 100 k $\Omega$  version. See Figure 2-26 for test circuit.
  - INL and DNL are measured at  $V_W$  with the device configured in the voltage divider or potentiometer mode.  $V_A = V_{DD}$  and  $V_B = 0V$ . DNL specification limits of  $\pm 1$  LSB max are specified monotonic operating conditions. See Figure 2-25 for test circuit.
  - Resistor terminals A,B and W have no restrictions on polarity with respect to each other. Full scale and zero scale error were measured using Figure 2-25.
  - Measured at  $V_W$  pin where the voltage on the adjacent  $V_W$  pin is swinging full scale.
  - All dynamic characteristics use  $V_{DD} = 5V$ .
  - Supply current is independent of current through the potentiometers.
  - TSSOP devices are only specified at  $25^{\circ}C$  and  $85^{\circ}C$
  - See Figure 2-25 for test circuit.
  - See Figure 2-12 for  $RS$  and  $SHDN$  pin operation.

## ELECTRICAL CHARACTERISTICS (CONTINUED)

### Maximum Ratings\*

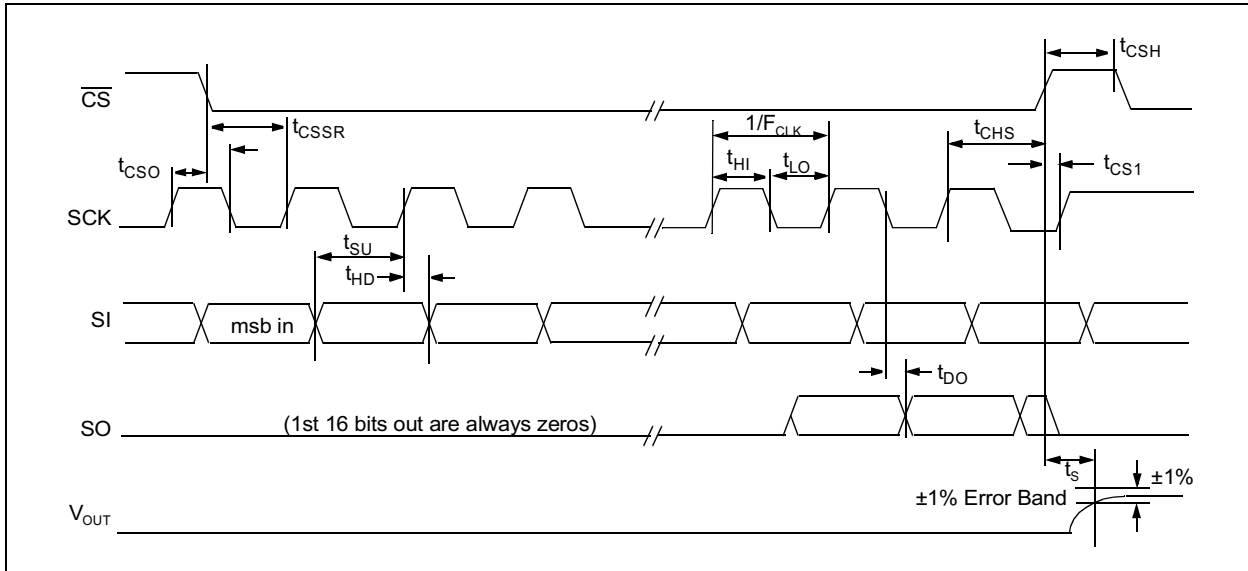
$V_{DD}$ .....	7.0V
All inputs and outputs w.r.t. $V_{SS}$ .....	-0.6V to $V_{DD} + 1.0V$
Storage temperature .....	-60°C to +150°C
Ambient temp. with power applied .....	-60°C to +125°C
ESD protection on all pins .....	$\geq 2$ kV

\***Notice:** Stresses above those listed under “maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

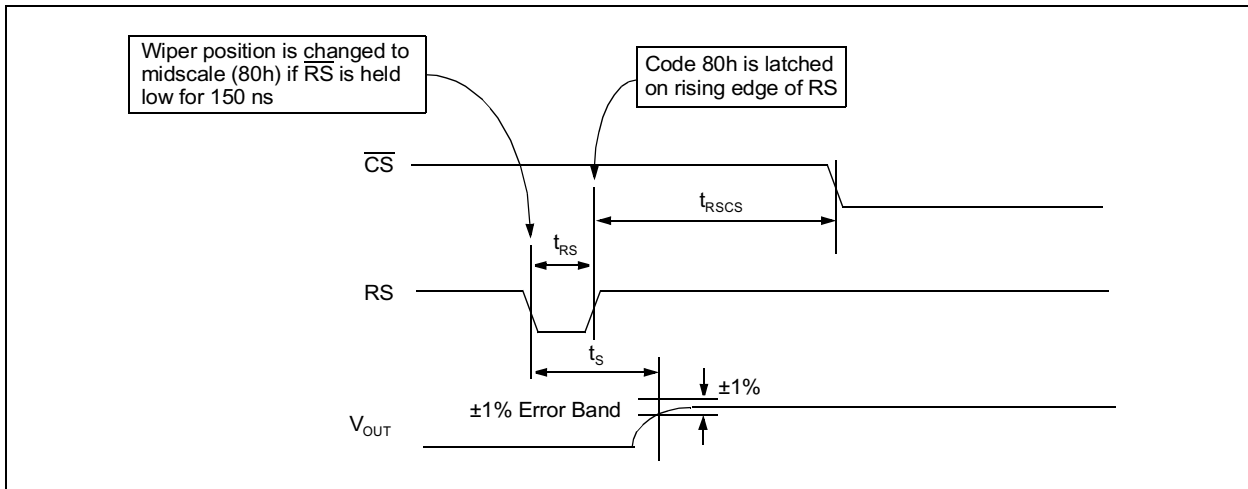
## AC TIMING CHARACTERISTICS

All parameters apply across the specified operating ranges unless otherwise noted.		Industrial (I): $V_{DD} = +2.7V$ to $5.5V$ $T_A = -40^\circ C$ to $+85^\circ C$				
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Clock Frequency	$F_{CLK}$	—	—	10	MHz	$V_{DD} = 5V$ (Note 1)
Clock High Time	$t_{HI}$	40	—	—	ns	
Clock Low Time	$t_{LO}$	40	—	—	ns	
$\overline{CS}$ Fall to First Rising CLK Edge	$t_{CSSR}$	40	—	—	ns	
Data Input Setup Time	$t_{SU}$	40	—	—	ns	
Data Input Hold Time	$t_{HD}$	10	—	—	ns	
SCK Fall to SO Valid Propagation Delay	$t_{DO}$	—	—	80	ns	$C_L = 30$ pF (Note 2)
SCK Rise to $\overline{CS}$ Rise Hold Time	$t_{CHS}$	30	—	—	ns	
SCK Rise to $\overline{CS}$ Fall Delay	$t_{CS0}$	10	—	—	ns	
$\overline{CS}$ Rise to CLK Rise Hold	$t_{CS1}$	100	—	—	ns	
$\overline{CS}$ High Time	$t_{CSH}$	40	—	—	ns	
Reset Pulse Width	$t_{RS}$	150	—	—	ns	Note 2
$\overline{RS}$ Rising to $\overline{CS}$ Falling Delay Time	$t_{RSCS}$	150	—	—	ns	Note 2
$\overline{CS}$ rising to $\overline{RS}$ or $\overline{SHDN}$ falling delay time	$t_{SE}$	40	—	—	ns	Note 3
$\overline{CS}$ low time	$t_{CSL}$	100	—	—	ns	Note 3
Shutdown Pulse Width	$t_{SH}$	150	—	—	ns	Note 3
<b>Note 1:</b> When using the device in the daisy chain configuration, max. clock frequency is determined by a combination of propagation delay time ( $t_{DO}$ ) and data input setup time ( $t_{SU}$ ). Max. clock frequency is therefore ~ 5.8 MHz based on SCK rise and fall times of 5 ns, $t_{HI} = 40$ ns, $t_{DO} = 80$ ns and $t_{SU} = 40$ ns. <b>Note 2:</b> Applies only to the MCP42XXX devices. <b>Note 3:</b> Applies only when using hardware pins to exit software shutdown mode, MCP42XXX only.						

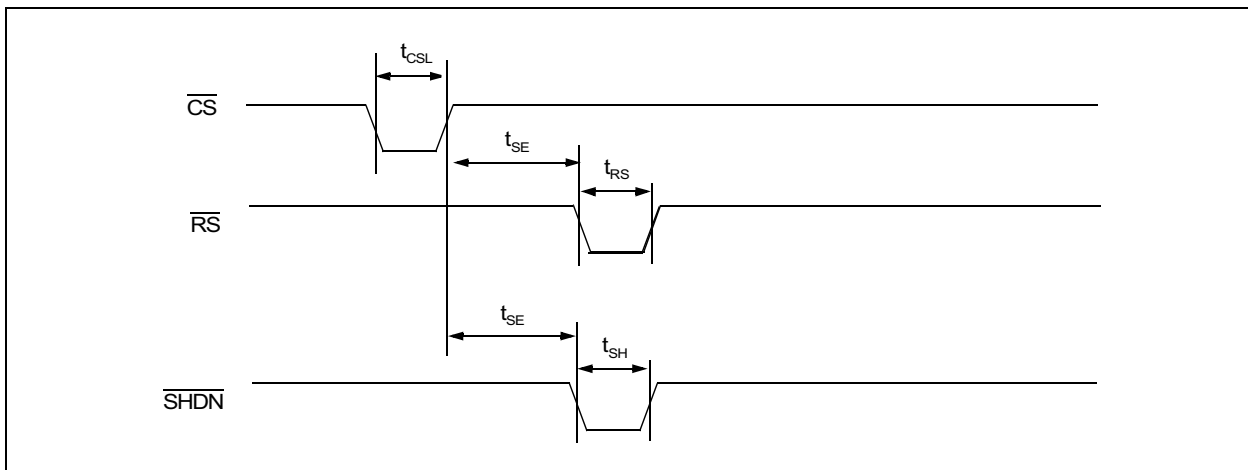
# MCP41XXX/42XXX



**Figure 1-1:** Detailed Serial interface Timing



**Figure 1-2:** Reset Timing

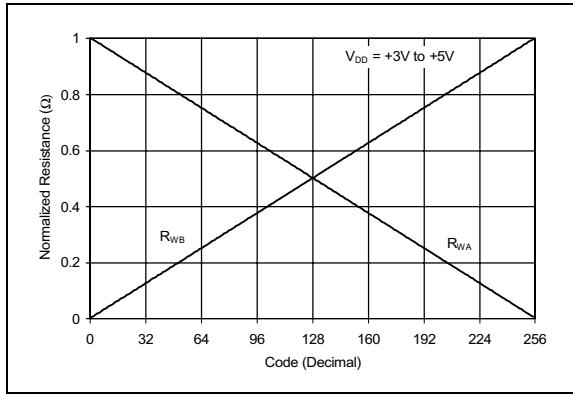


**Figure 1-3:** Software Shutdown Exit Timing

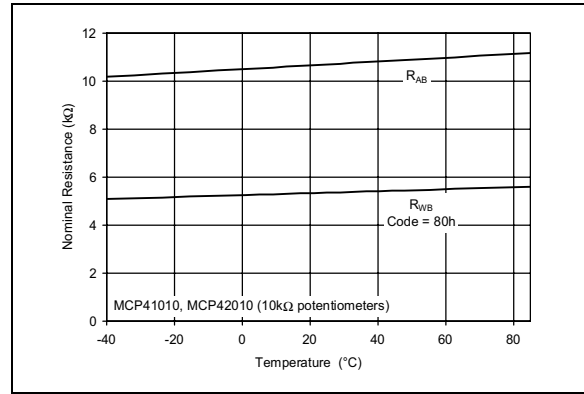
## 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

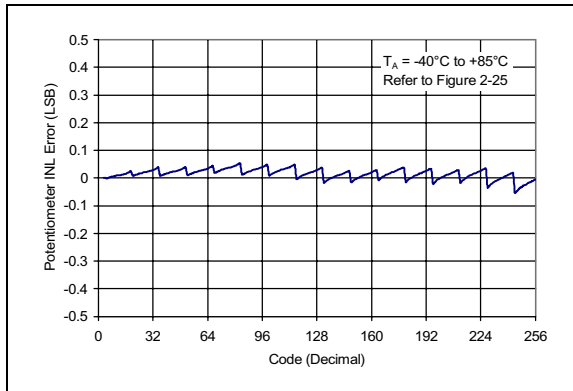
**Note:** Unless otherwise indicated, curve represents 10 k $\Omega$ , 50 k $\Omega$ , and 100 k $\Omega$  devices,  
 $V_{DD} = 5V$ ,  $V_{SS} = 0V$ ,  $T_A = 25^\circ C$ ,  $V_B = 0V$ .



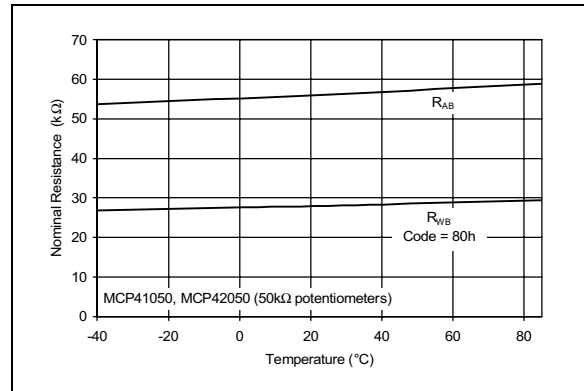
**Figure 2-1:** Normalized Wiper to End Terminal Resistance vs. Code



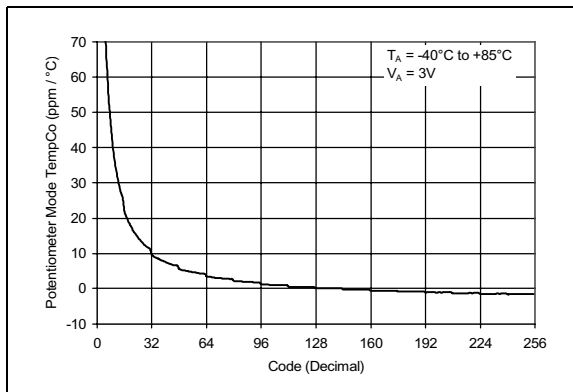
**Figure 2-4:** Nominal Resistance 10 k $\Omega$  vs. Temperature



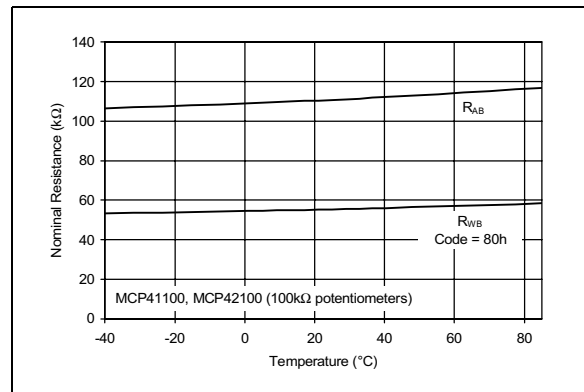
**Figure 2-2:** Potentiometer INL Error vs. Code



**Figure 2-5:** Nominal Resistance 50 k $\Omega$  vs. Temperature



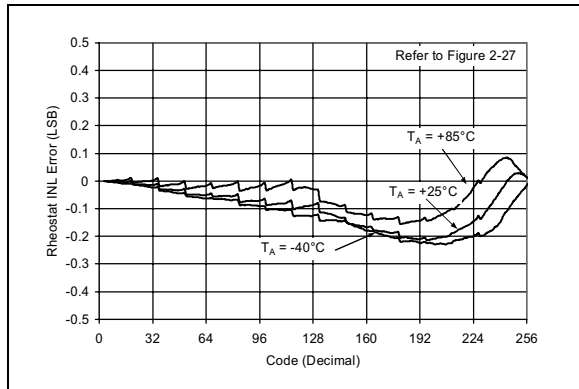
**Figure 2-3:** Potentiometer Mode Tempco vs. Code



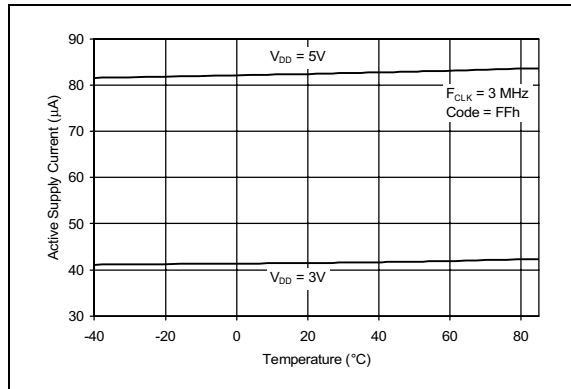
**Figure 2-6:** Nominal Resistance 100 k $\Omega$  vs. Temperature

# MCP41XXX/42XXX

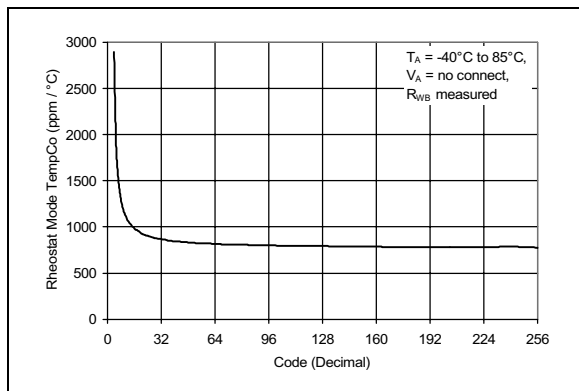
**Note:** Unless otherwise indicated, curve represents 10 k $\Omega$ , 50 k $\Omega$ , and 100 k $\Omega$  devices,  
 $V_{DD} = 5V$ ,  $V_{SS} = 0V$ ,  $T_A = 25^\circ C$ ,  $V_B = 0V$ .



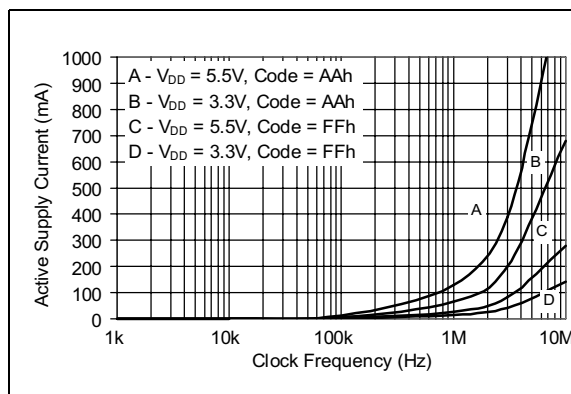
**Figure 2-7:** Rheostat INL Error vs. Code



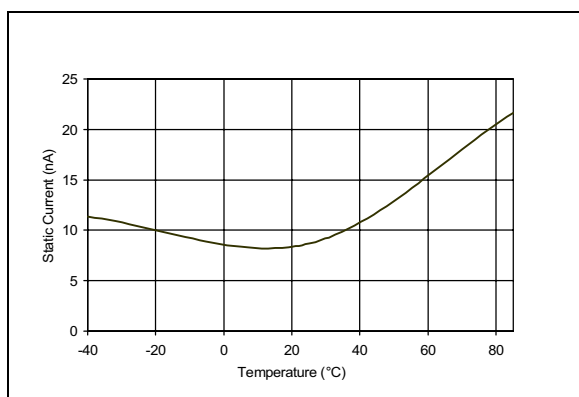
**Figure 2-10:** Active Supply Current vs. Temperature



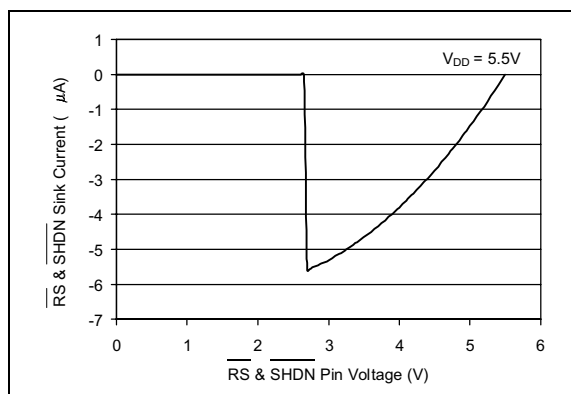
**Figure 2-8:** Rheostat Mode TempCo vs. Code



**Figure 2-11:** Active Supply Current vs. Clock Frequency



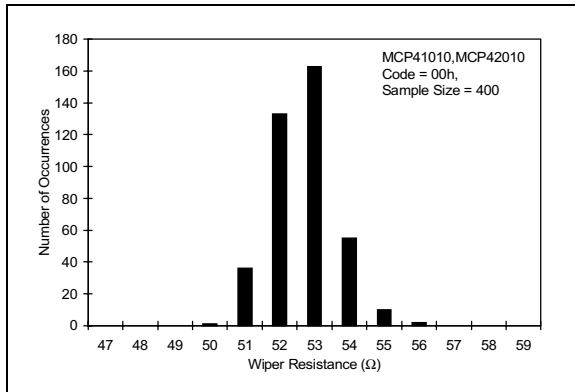
**Figure 2-9:** Static Current vs. Temperature



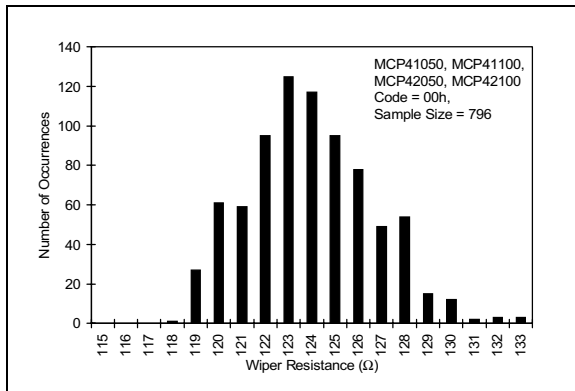
**Figure 2-12:** Reset & Shutdown Pins Current vs. Voltage

# MCP41XXX/42XXX

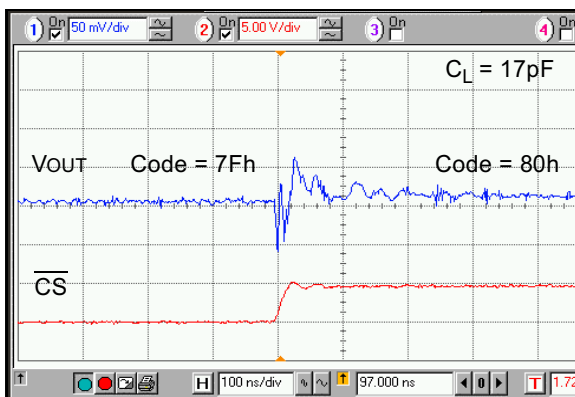
**Note:** Unless otherwise indicated, curve represents 10 k $\Omega$ , 50 k $\Omega$ , and 100 k $\Omega$  devices,  
 $V_{DD} = 5V$ ,  $V_{SS} = 0V$ ,  $T_A = 25^\circ C$ ,  $V_B = 0V$ .



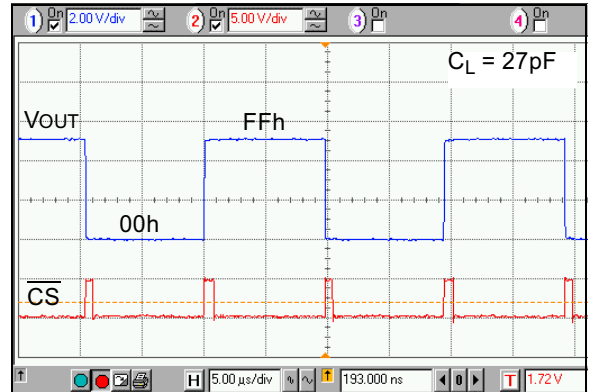
**Figure 2-13:** 10 k $\Omega$  Device Wiper Resistance Histogram



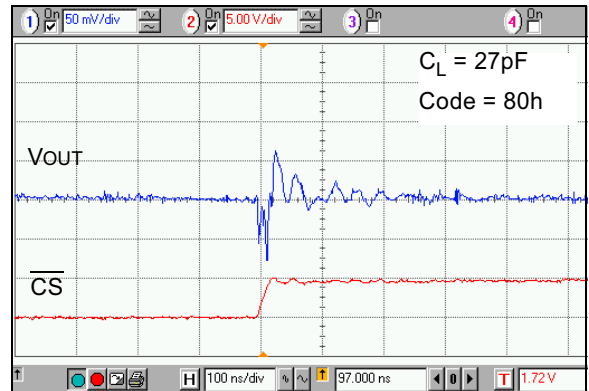
**Figure 2-14:** 50 k $\Omega$ , 100 k $\Omega$  Device Wiper Resistance Histogram



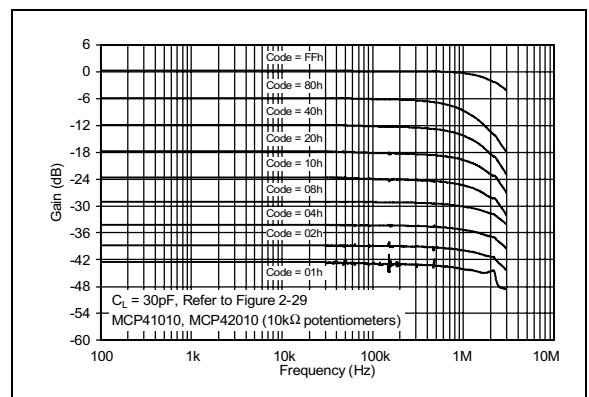
**Figure 2-15:** One Position Settling Time



**Figure 2-16:** Full Scale Settling Time



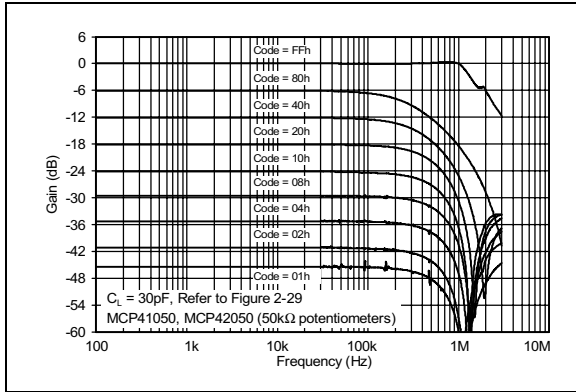
**Figure 2-17:** Digital Feedthrough vs. Time



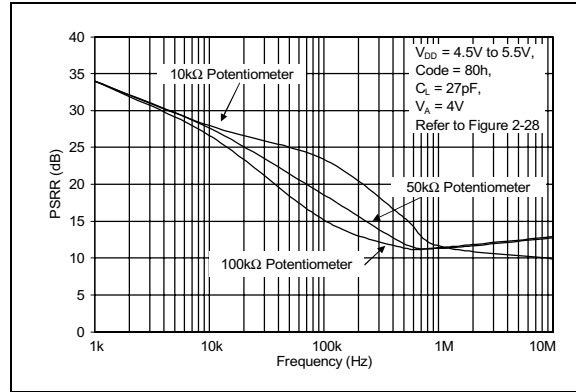
**Figure 2-18:** Gain vs. Frequency for 10 k $\Omega$  Potentiometer

# MCP41XXX/42XXX

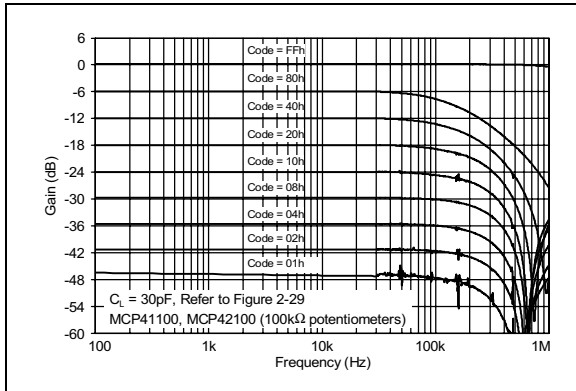
**Note:** Unless otherwise indicated, curve represents 10 k $\Omega$ , 50 k $\Omega$ , and 100 k $\Omega$  devices,  
 $V_{DD} = 5V$ ,  $V_{SS} = 0V$ ,  $T_A = 25^\circ C$ ,  $V_B = 0V$ .



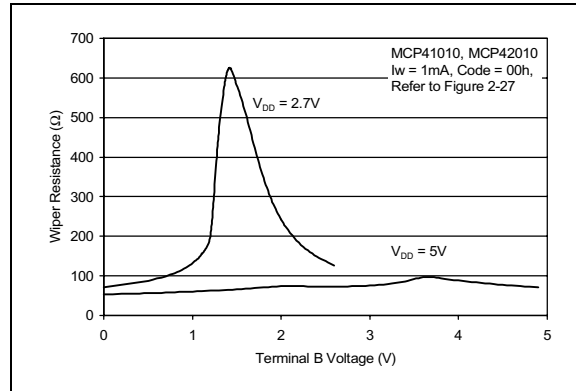
**Figure 2-19:** Gain vs. Frequency for 50k $\Omega$  Potentiometer



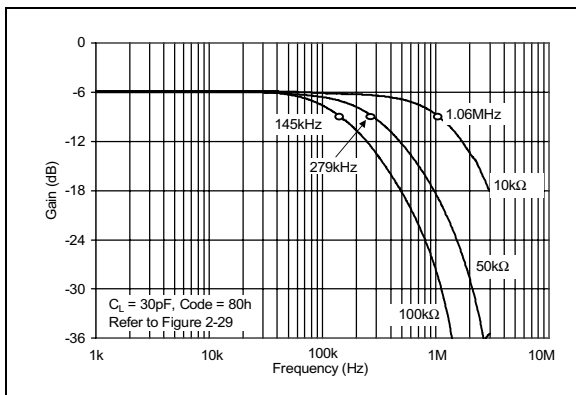
**Figure 2-22:** Power Supply Rejection Ratio vs. Frequency



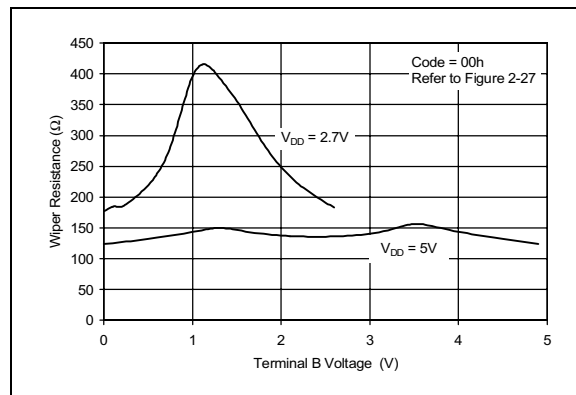
**Figure 2-20:** Gain vs. Frequency for 100k $\Omega$  Potentiometer



**Figure 2-23:** 10 k $\Omega$  Wiper Resistance vs. Voltage

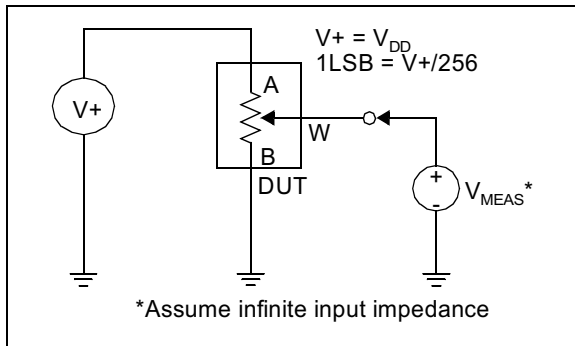


**Figure 2-21:** -3 dB Bandwidths

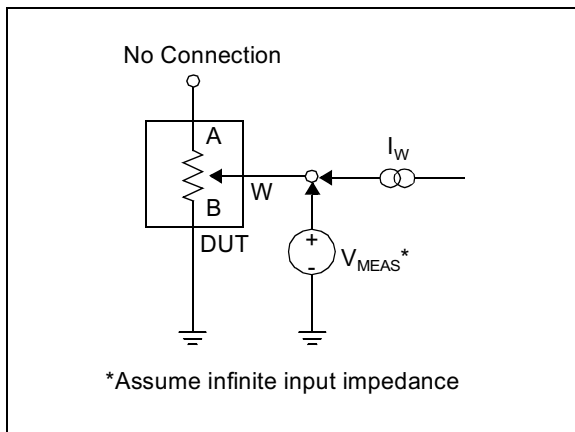


**Figure 2-24:** 50 k $\Omega$  & 100 k $\Omega$  Wiper Resistance vs. Voltage

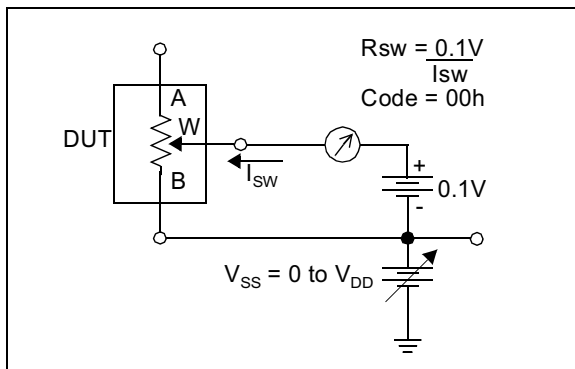
## 2.1 Parametric Test Circuits



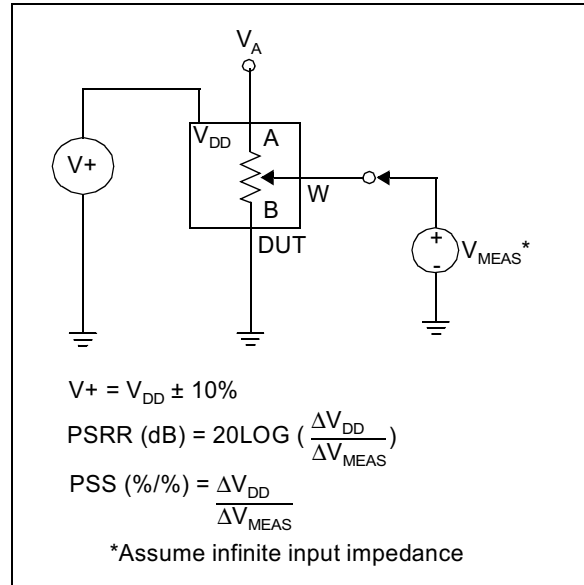
**Figure 2-25:** Potentiometer Divider Non-Linearity Error Test Circuit (DNL, INL)



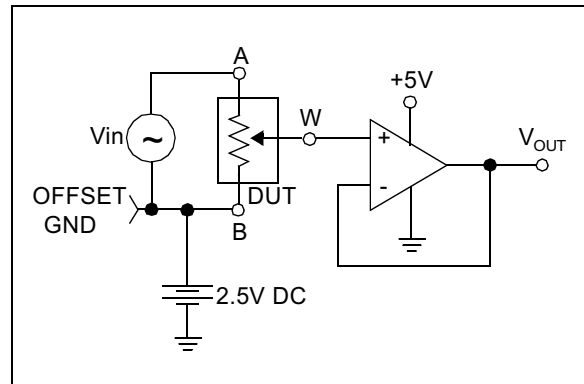
**Figure 2-26:** Resistor Position Non-Linearity Error Test Circuit (Rheostat operation DNL, INL)



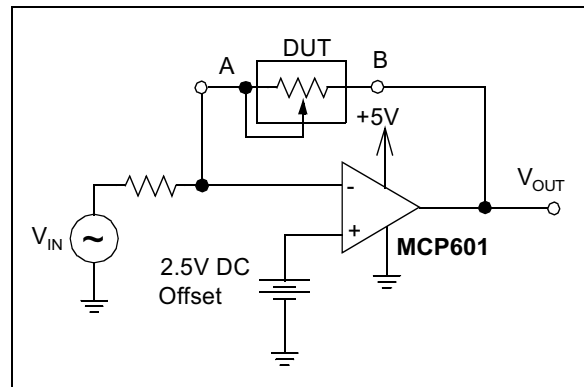
**Figure 2-27:** Wiper Resistance Test Circuit



**Figure 2-28:** Power Supply Sensitivity Test Circuit (PSS, PSRR)



**Figure 2-29:** Gain vs. Frequency Test Circuit



**Figure 2-30:** Capacitance Test Circuit

# MCP41XXX/42XXX

## 3.0 PIN DESCRIPTIONS

### 3.1 PA0, PA1

Potentiometer Terminal A Connection.

### 3.2 PB0, PB1

Potentiometer Terminal B Connection.

### 3.3 PW0, PW1

Potentiometer Wiper Connection.

### 3.4 Chip Select ( $\overline{CS}$ )

This is the SPI port chip select pin and is used to execute a new command after it has been loaded into the shift register. This pin has a Schmitt Trigger input.

### 3.5 Serial Clock (SCK)

This is the SPI port clock pin and is used to clock in new register data. Data is clocked into the SI pin on the rising edge of the clock and out the SO pin on the falling edge of the clock. This pin is gated to the  $\overline{CS}$  pin, i.e., the device will not draw any more current if the SCK pin is toggling when the  $\overline{CS}$  pin is high. This pin has a Schmitt Trigger input.

### 3.6 Serial Data Input (SI)

This is the SPI port serial data input pin. The command and data bytes are clocked into the shift register using this pin. This pin is gated to the  $\overline{CS}$  pin, i.e., the device will not draw any more current if the SI pin is toggling when the  $\overline{CS}$  pin is high. This pin has a Schmitt Trigger input.

### 3.7 Serial Data Output (SO) (MCP42XXX devices only)

This is the SPI port serial data output pin used for daisy chaining more than one device. Data is clocked out of the SO pin on the falling edge of clock. This is a push-pull output and **does not** go to a high impedance state when  $\overline{CS}$  is high. It will drive a logic low when  $\overline{CS}$  is high.

### 3.8 Reset ( $\overline{RS}$ ) (MCP42XXX devices only)

The Reset pin will set all potentiometers to mid-scale (Code 80h) if this pin is brought low for at least 150ns. This pin should not be toggled low when the  $\overline{CS}$  pin is low. It is possible to toggle this pin when the SHDN pin is low. In order to minimize power consumption, this pin has an active pull-up circuit. The performance of this circuit is shown in Figure 2-12. This pin will draw negligible current at logic level 0 and logic level 1.

### 3.9 Shutdown ( $\overline{SHDN}$ ) (MCP42XXX devices only)

The Shutdown pin has a Schmitt Trigger input. Pulling this pin low will put the device in a power saving mode where A terminal is opened and the B and W terminals are connected for all potentiometers. This pin should not be toggled low when the  $\overline{CS}$  pin is low. In order to minimize power consumption, this pin has an active pull-up circuit. The performance of this circuit is shown in Figure 2-12. This pin will draw negligible current at logic level 0 and logic level 1.

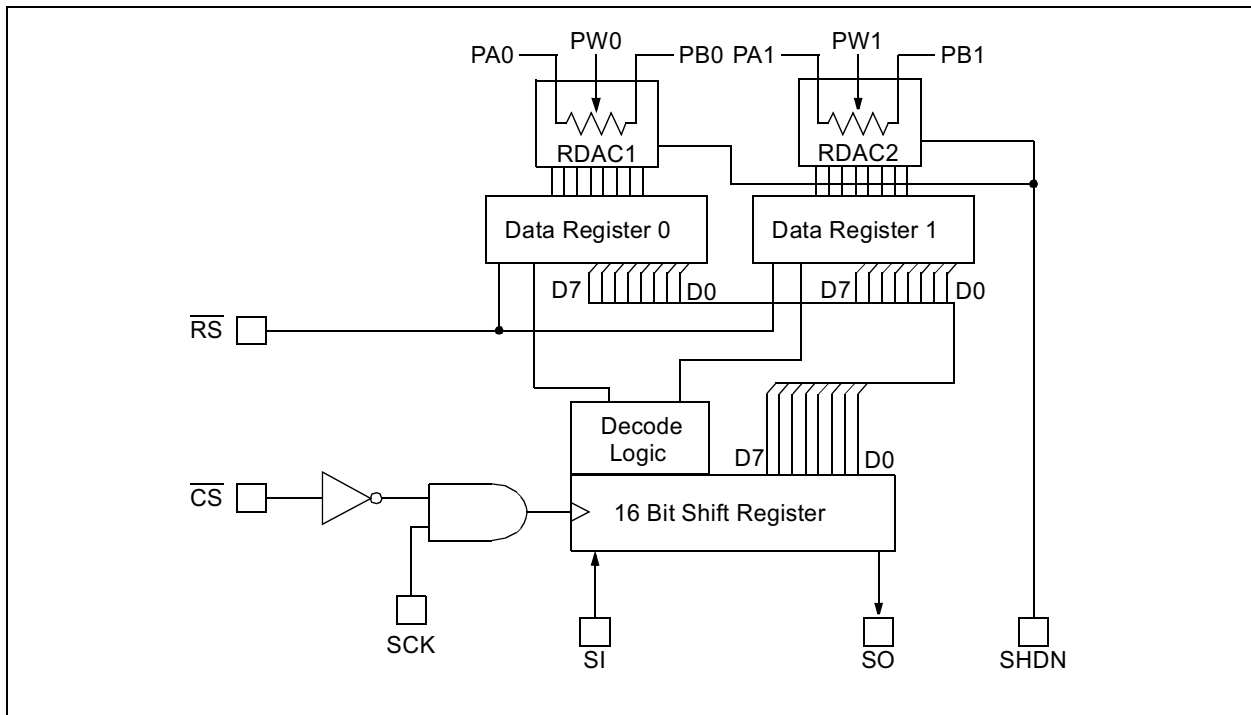
MCP41XXX PINS		
PIN #	NAME	FUNCTION
1	$\overline{CS}$	Chip Select
2	SCK	Serial Clock
3	SI	Serial Data Input
4	$V_{SS}$	Ground
5	PA0	Terminal A Connection For Pot 0
6	PW0	Wiper Connection For Pot 0
7	PB0	Terminal B Connection For Pot 0
8	$V_{DD}$	Power

MCP42XXX PINS		
PIN #	NAME	FUNCTION
1	$\overline{CS}$	Chip Select
2	SCK	Serial Clock
3	SI	Serial Data Input
4	$V_{SS}$	Ground
5	PB1	Terminal B Connection For Pot 1
6	PW1	Wiper Connection For Pot 1
7	PA1	Terminal A Connection For Pot 1
8	PA0	Terminal A Connection For Pot 0
9	PW0	Wiper Connection For Pot 0
10	PB0	Terminal B Connection For Pot 0
11	$\overline{RS}$	Reset Input
12	$\overline{SHDN}$	Shutdown Input
13	SO	Data Out for Daisy Chaining
14	$V_{DD}$	Power

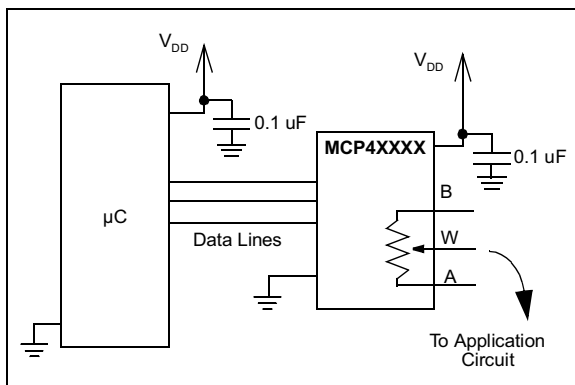
## 4.0 APPLICATIONS INFORMATION

The MCP41XXX/42XXX devices are 256 tap single and dual digital potentiometers that can be used in place of standard mechanical pots. Resistance values of 10 k $\Omega$ , 50 k $\Omega$  and 100 k $\Omega$  are available. As shown in Figure 4-1, each potentiometer is made up of a variable resistor and an 8-bit (256 position) data register that determines the wiper position. There is a nominal wiper resistance of 52  $\Omega$  for the 10 k $\Omega$  version and 125  $\Omega$  for the 50 k $\Omega$  and 100 k $\Omega$  versions. For the dual devices, the channel to channel matching variation is less than 1%. The resistance between the wiper and either of the resistor endpoints varies linearly according to the value stored in the data register. Code 00h effectively con-

nects the wiper to the B terminal. At power up, all data registers will automatically be loaded with the mid-scale value, 80h. The serial interface provides the means for loading data into the shift register which is then transferred to the data registers. The serial interface also provides the means to place individual potentiometers in the shutdown mode for maximum power savings. The  $\overline{\text{SHDN}}$  pin can also be used to put all potentiometers in shutdown mode and the  $\overline{\text{RS}}$  pin is provided to set all potentiometers to mid-scale, 80h.



**Figure 4-1:** Block diagram showing the MCP42XXX dual digital potentiometer. Data register 0 and data register 1 are 8-bit registers allowing 256 tap positions for each wiper. Standard SPI pins are used with the addition of the Shutdown (SHDN) and Reset (RS) pins. As shown, reset affects the data register and wipers, bringing them to mid-scale. Shutdown disconnects the A terminal and connects the wiper to B, without changing the state of the data registers.



When laying out the circuit for your digital potentiometer, bypass capacitors should be used. These capacitors should be placed as close as possible to the device pin. A bypass capacitor value of 0.1  $\mu\text{F}$  is recommended. Digital and analog traces should be separated as much as possible on the board, and no traces should run underneath the device or the bypass capacitor. Extra precautions should be taken to keep traces with high frequency signals (such as clock lines) as far as possible from analog traces. Use of an analog ground plane is recommended in order to keep the ground potential the same for all devices on the board.

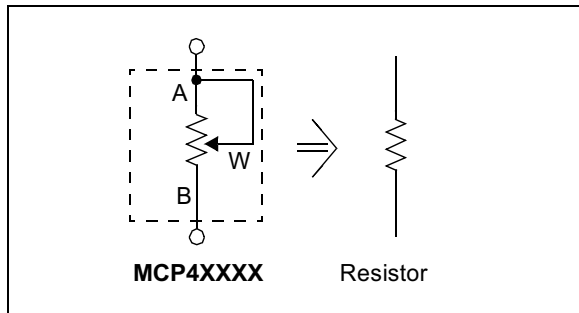
# MCP41XXX/42XXX

## 4.1 Modes of Operation

Digital potentiometer applications can be divided up into two categories: rheostat mode and potentiometer or voltage divider mode.

### 4.1.1 RHEOSTAT MODE

In the rheostat mode, the potentiometer is used as a two terminal resistive element. The unused terminal should be tied to the wiper as shown in Figure 4-2. Note that reversing the polarity of the A and B terminals will not affect operation.



**Figure 4-2:** Two terminal or rheostat configuration for the digital potentiometer. Acting as a resistive element in the circuit, resistance is controlled by changing the wiper setting.

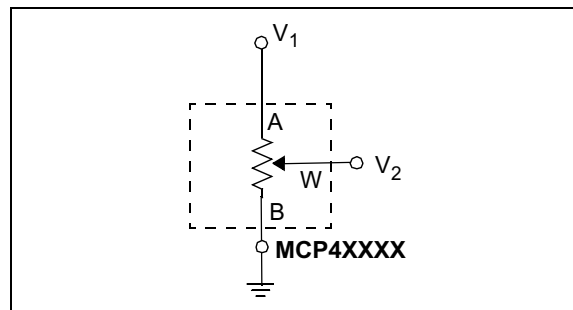
Using the device in this mode allows control of the total resistance between the two nodes. The total measured resistance would be the least at code 00h, where the wiper is tied to the B terminal. The resistance at this code is equal to the wiper resistance, typically 52  $\Omega$  for the 10 k $\Omega$  devices (MCP4X010), 125  $\Omega$  for the 50 k $\Omega$  (MCP4X050), and 100 k $\Omega$  (MCP4X100) devices. For the 10 k $\Omega$  device, the LSB size would be 39.0625  $\Omega$  (assuming 10 k $\Omega$  total resistance). The resistance would then increase with this LSB size until the total measured resistance at code FFh would be 9985.94  $\Omega$ . The wiper will never directly connect to the A terminal of the resistor stack.

In the 00h state, the total resistance is the wiper resistance. To avoid damage to the internal wiper circuitry in this configuration, care should be taken to insure the current flow never exceeds 1 mA.

For dual devices, the variation of channel-to-channel matching of the total resistance from A to B is less than 1%. The device-to-device matching however can vary up to 30%. In the rheostat mode, the resistance has a positive temperature coefficient. The change in wiper-to-end terminal resistance over temperature is shown in Figure 2-8. The most variation over temperature will occur in the first 6% of codes (code 00h to 0Fh) due to the wiper resistance coefficient affecting the total resistance. The remaining codes are dominated by the total resistance tempco  $R_{AB}$ , typically 800 ppm/ $^{\circ}\text{C}$ .

### 4.1.2 POTENTIOMETER MODE

In the potentiometer mode, all three terminals of the device are tied to different nodes in the circuit. This allows the potentiometer to output a voltage proportional to the input voltage. This mode is sometimes called voltage divider mode. The potentiometer is used to provide a variable voltage by adjusting the wiper position between the two endpoints as shown in Figure 4-3. Note that reversing the polarity of the A and B terminals will not affect operation.



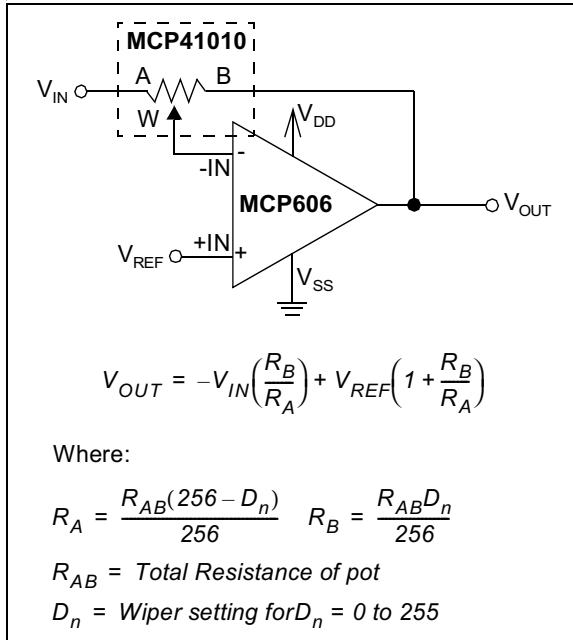
**Figure 4-3:** Three terminal or voltage divider mode

In this configuration, the ratio of the internal resistances define the temperature coefficient of the device. The resistor matching of the  $R_{WB}$  resistor to the  $R_{AB}$  resistor performs with a typical temperature coefficient of 1 ppm/ $^{\circ}\text{C}$  (measured at code 80h). At lower codes, the wiper resistance temperature coefficient will dominate. Figure 2-3 shows the effect of the wiper. Above the lower codes, this figure shows that 70% of the states will typically have a temperature coefficient of less than 5 ppm/ $^{\circ}\text{C}$ . 30% of the states will typically have a ppm/ $^{\circ}\text{C}$  of less than 1.

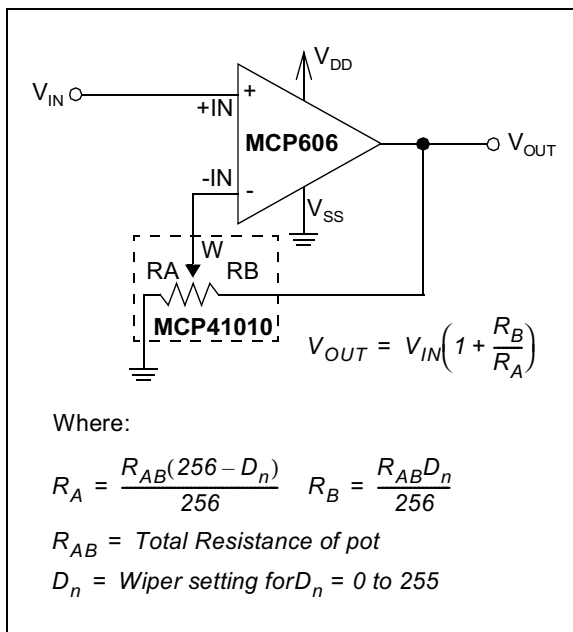
## 4.2 Typical Applications

### 4.2.1 PROGRAMMABLE SINGLE ENDED AMPLIFIERS

Potentiometers are often used to adjust system reference levels or gain. Programmable gain circuits using digital potentiometers can be realized in a number of different ways. An example of a single supply inverting gain amplifier is shown in Figure 4-4. Due to the high input impedance of the amplifier, the wiper resistance is not included in the transfer function. For a single supply non-inverting gain configuration, the circuit in Figure 4-5 can be used.



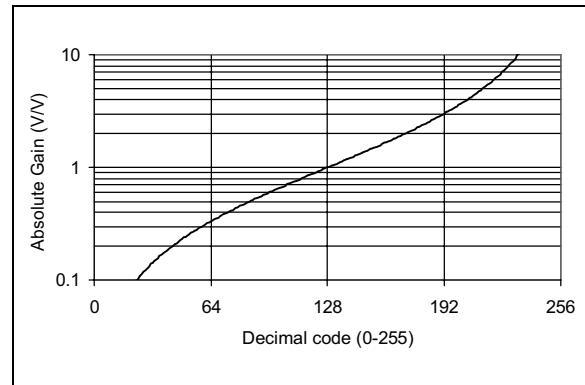
**Figure 4-4:** Single supply programmable inverting gain amplifier using a digital potentiometer.



**Figure 4-5:** Single Supply Programmable Non-inverting gain amplifier

In order for these circuits to work properly, care must be taken in a few areas. For linear operation, the analog input and output signals must be in the range of  $V_{SS}$  to  $V_{DD}$  for the potentiometer and input and output rails of the op-amp. The circuit in Figure 4-4 requires a virtual ground or reference input to the non-inverting input of the amplifier. Refer to Application Note AN-682, "Using Single Supply Operational Amplifiers in Embedded Systems" for more detail. At power up or reset (RS), the resistance is set to mid-scale and  $R_A$  and  $R_B$  match.

Based on the transfer function for the circuit, the gain is -1 V/V. As the code is increased and the wiper moves towards the A terminal and the gain increases. Conversely, when the wiper is moved towards the B terminal, the gain decreases. Figure 4-6 shows this relationship. Notice the pseudo-logarithmic gain around decimal code 128. As the wiper approaches either terminal, the step size in the gain calculation increases dramatically. Due to the mismatched ratio of  $R_A$  and  $R_B$  at the extreme high and low codes, small increments in wiper position can dramatically affect the gain. As shown in Figure 4-3, recommended gains lie between 0.1 and 10V/V.

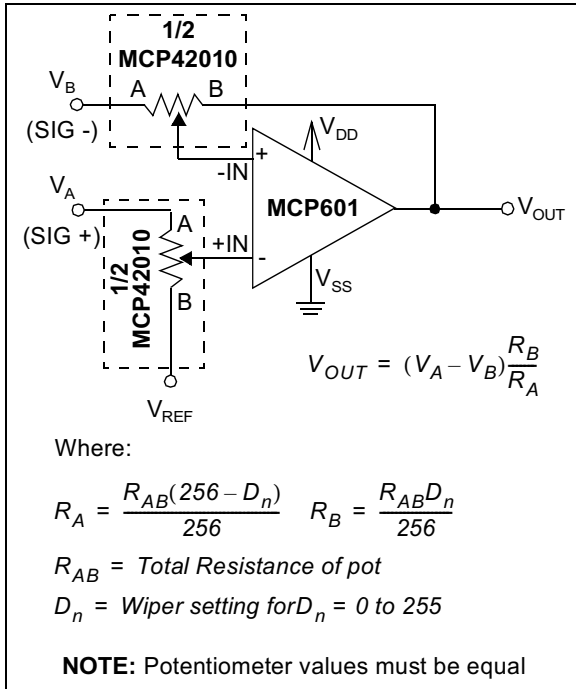


**Figure 4-6:** Gain vs. Code for inverting and differential amplifier circuits.

## 4.2.2 PROGRAMMABLE DIFFERENTIAL AMPLIFIER

An example of a differential input amplifier using digital potentiometers is shown in Figure 4-7. For the transfer function to hold, both pots must be programmed to the same code. The resistor matching from channel-to-channel within a dual device can be used as an advantage in this circuit. This circuit will also show stable operation over temperature due to the low potentiometer temperature coefficient. Figure 4-6 also shows the relationship between gain and code for this circuit. As the wiper approaches either terminal, the step size in the gain calculation increases dramatically. This circuit is recommended for gains between 0.1 and 10V/V.

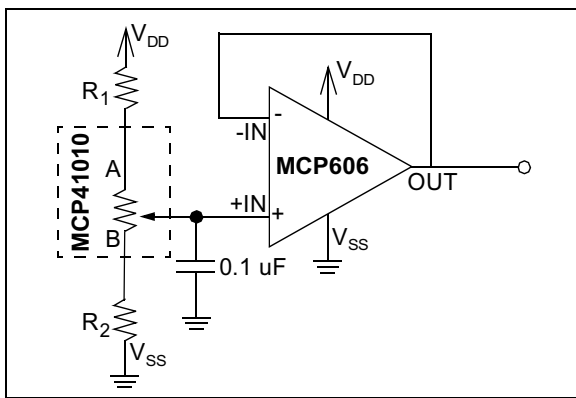
# MCP41XXX/42XXX



**Figure 4-7:** Single Supply programmable differential amplifier using digital potentiometers.

## 4.2.3 PROGRAMMABLE OFFSET TRIM

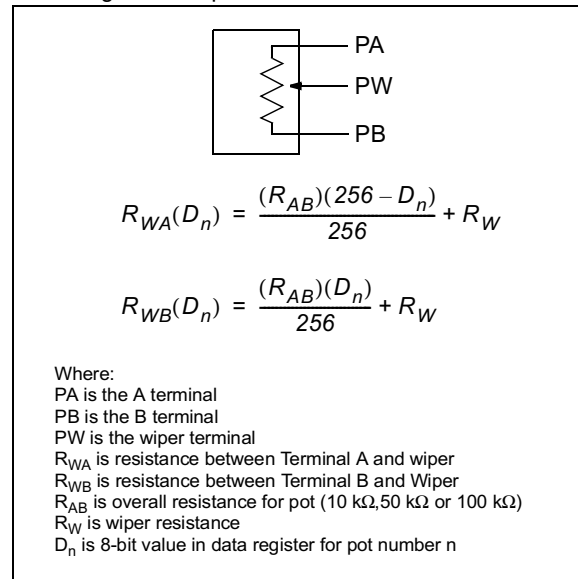
For applications requiring only a programmable voltage reference, the circuit in Figure 4-8 can be used. This circuit shows the device used in the potentiometer mode along with two resistors and a buffered output. This creates a circuit with a linear relationship between voltage out and programmed code. Resistors  $R_1$  and  $R_2$  can be used to increase or decrease the output voltage step size. The potentiometer in this mode is stable over temperature. The operation of this circuit over temperature is shown in Figure 2-3. The worst performance over temperature will occur at the lower codes due to the dominating wiper resistance.  $R_1$  and  $R_2$  can also be used to affect the boundary voltages thereby eliminating the use of these lower codes.



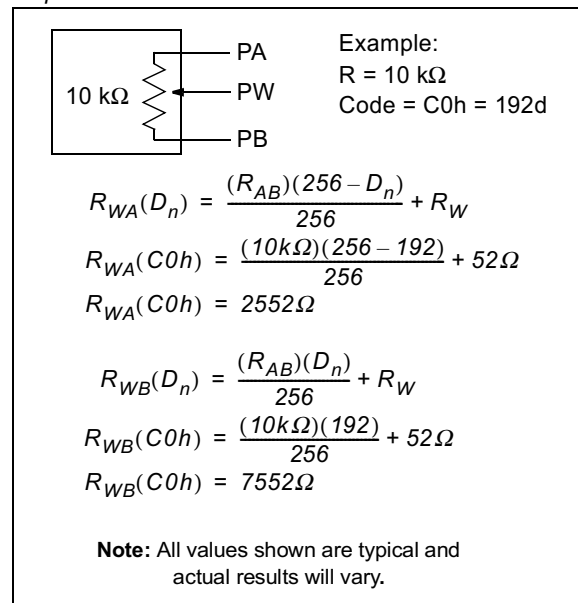
**Figure 4-8:** By changing the values of  $R_1$  and  $R_2$ , the voltage output resolution of this programmable voltage reference circuit is affected.

## 4.3 Calculating Resistances

When programming the digital potentiometer settings, the following equations can be used to calculate the resistances. Programming code 00h effectively brings the wiper to the B terminal, leaving only the wiper resistance. Programming higher codes will bring the wiper closer to the A terminal of the potentiometer. The equations in Figure 4-9 can be used to calculate the terminal resistances. Figure 4-10 shows an example calculation using a 10 k $\Omega$  potentiometer.



**Figure 4-9:** Potentiometer resistances are a function of code. It should be noted that when using these equations for most feedback amplifier circuits (see Figure 4-4 and Figure 4-5), the wiper resistance can be omitted due to the high impedance input of the amplifier.



**Figure 4-10:** Example Resistance calculations.

## 5.0 SERIAL INTERFACE

Communications from the controller to the MCP41XXX/42XXX digital potentiometers is done using the SPI serial interface. This interface allows three commands:

1. Write a new value to the potentiometer data register(s).
2. Cause a channel to enter low power shutdown mode.
3. NOP (No Operation) command.

Executing any command is done by setting  $\overline{CS}$  low, and then clocking in a command byte followed by a data byte into the 16-bit shift register. The command is executed when  $\overline{CS}$  is raised. Data is clocked in on the rising edge of clock and out the SO pin on the falling edge of the clock. See Figure 5-1. The device will track the number of clocks (rising edges) while  $\overline{CS}$  is low and will abort all commands if the number of clocks is not a multiple of 16.

### 5.1 Command Byte

The first byte sent is always the command byte, followed by the data byte. The command byte contains two command select bits and two potentiometer select bits. Unused bits are don't care bits. The command select bits are summarized in Figure 5-2. The command select bits C1 and C0 (bits 4:5) of the command byte determine which command will be executed. If the command bits are both 0's or 1's, then a NOP command will be executed after all 16 bits have been loaded. This command is useful when using the daisy-chain configuration. When the command bits are 0,1 a write command will be executed with the 8 bits sent in the data byte. The data will be written to the potentiometer(s) determined by the potentiometer select bits. If the command bits are 1,0 then a shutdown command will be executed on the potentiometers determined by the potentiometer select bits.

For the MCP42XXX devices, the potentiometer select bits P1 and P0 (bits 0:1) determine which potentiometers are to be acted upon by the command. A corresponding one in the position signifies that the command for that potentiometer will get executed and a zero signifies that the command will not effect that potentiometer. See Figure 5-2.

### 5.2 Writing Data Into Data Registers

When new data is written into one or more of the potentiometer data registers, the write command is followed by the data byte for the new value. The command select bits C1, C0 are set to 0,1. The potentiometer selection bits P1 and P0 allow new values to be written to potentiometer 0, potentiometer 1 or both with a single command. A one for either P1 or P0 will cause the data to be written to the respective data register and a zero for P1 or P0 will cause no change. See Figure 5-2 for the command format summary.

### 5.3 Using The Shutdown Command

The shutdown command allows the user to put the application circuit into a power saving mode. In this mode, the A terminal is open circuited and the B and W terminals are shorted together. The command select bits C1, C0 are set to 1,0. The potentiometer selection bits P1 and P0 allow each potentiometer to be shut-down independently. If either P1 or P0 are high, the respective potentiometer will enter shutdown mode. A zero for P1 or P0 will have no effect. The eight data bits following the command byte still need to be transmitted for the shutdown command but they are don't care bits. See Figure 5-2 for command format summary. Once a particular potentiometer has entered the shutdown mode, it will remain in this mode until:

- A new value is written to the potentiometer data register, provided that the  $\overline{SHDN}$  pin is high. The device will remain in the shutdown mode until the rising edge of the  $\overline{CS}$  is detected, at which time the device will come out of shutdown mode and the new value will be written to the data register(s). If the  $\overline{SHDN}$  pin is low when the new value is received, the registers will still be set to the new value, but the device will remain in shutdown mode. This scenario assumes that a valid command was received. If an invalid command was received, the command will be ignored and the device will remain in the shutdown mode.

It is also possible to use the hardware shutdown pin and reset pin to remove a device from software shutdown. To do this, a low pulse on the chip select line must first be sent. For multiple devices, sharing a single  $\overline{SHDN}$  or  $\overline{RESET}$  line, allows you to pick an individual device on that chain to remove from software shutdown mode. See Figure 1-3 for timing. With a preceding chip select pulse, either of these situations will also remove a device from software shutdown:

- A falling edge is seen on the  $\overline{RS}$  pin and held low for at least 150 ns, provided that the  $\overline{SHDN}$  pin is high. If the  $\overline{SHDN}$  pin is low, the registers will still be set to mid-scale but the device will remain in shutdown mode. This condition assumes that  $\overline{CS}$  is high, as bringing the  $\overline{RS}$  pin low while  $\overline{CS}$  is low is an invalid state and results are indeterminate.
- A rising edge on the  $\overline{SHDN}$  pin is seen after being low for at least 100ns, provided that the  $\overline{CS}$  pin is high. Toggling the  $\overline{SHDN}$  pin low while  $\overline{CS}$  is low is an invalid state and results are indeterminate.
- The device is powered down and back up.

**Note:** The hardware  $\overline{SHDN}$  pin will always put the device in shutdown regardless of whether a potentiometer has already been put in the shutdown mode using the software command.

# MCP41XXX/42XXX

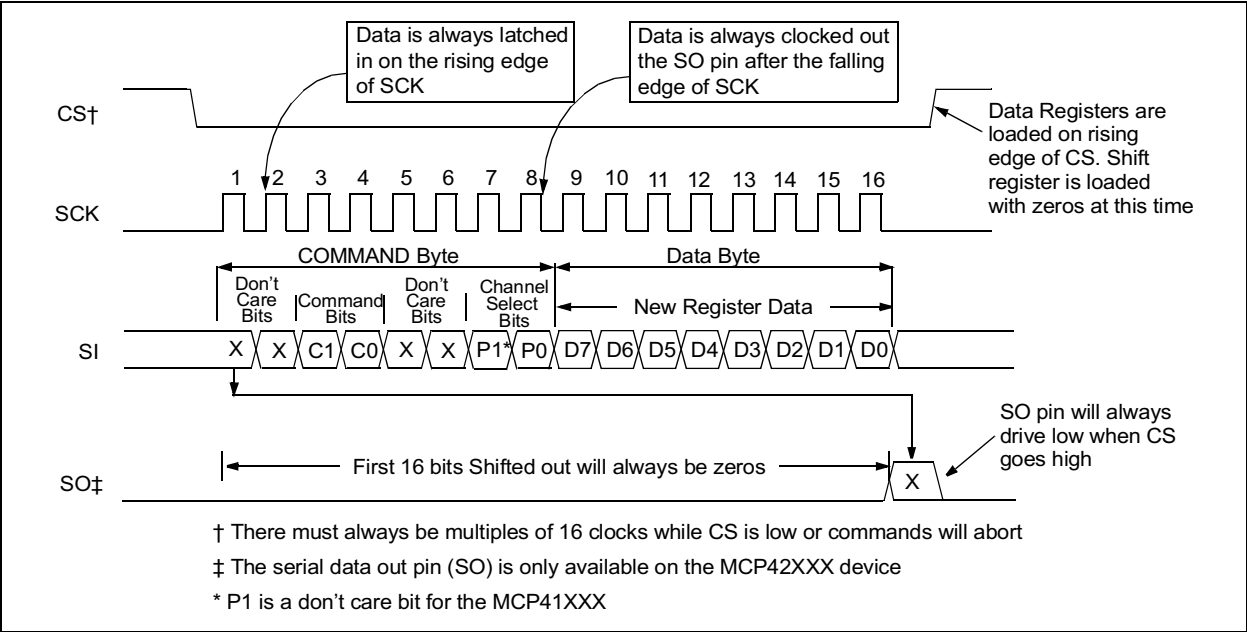


Figure 5-1: Timing Diagram for Writing Instructions or Data to a Digital Potentiometer

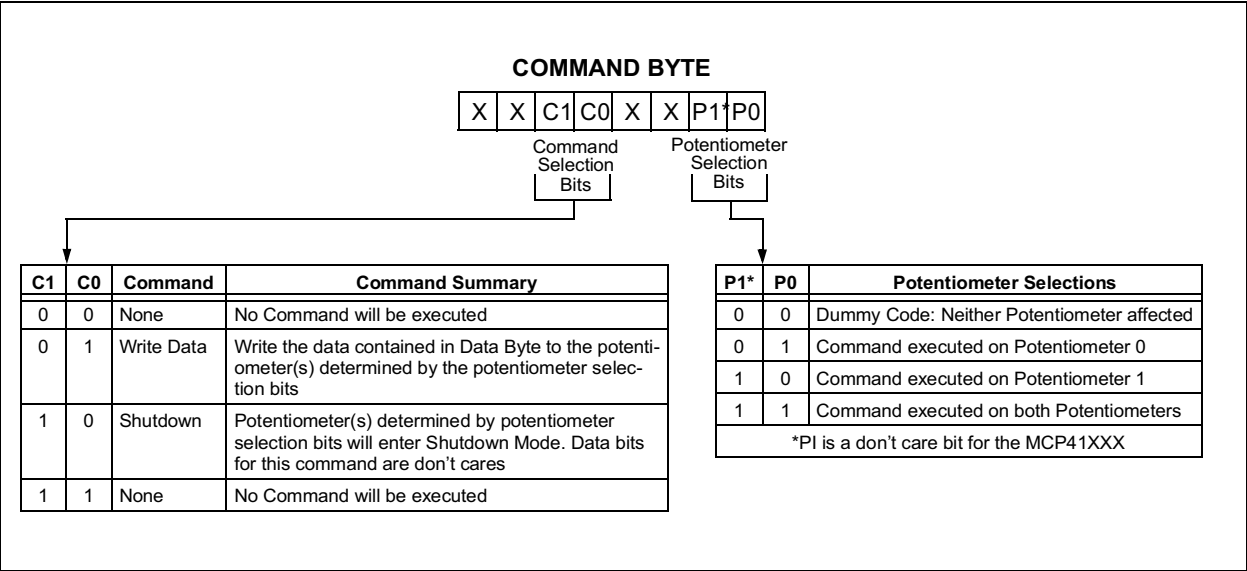


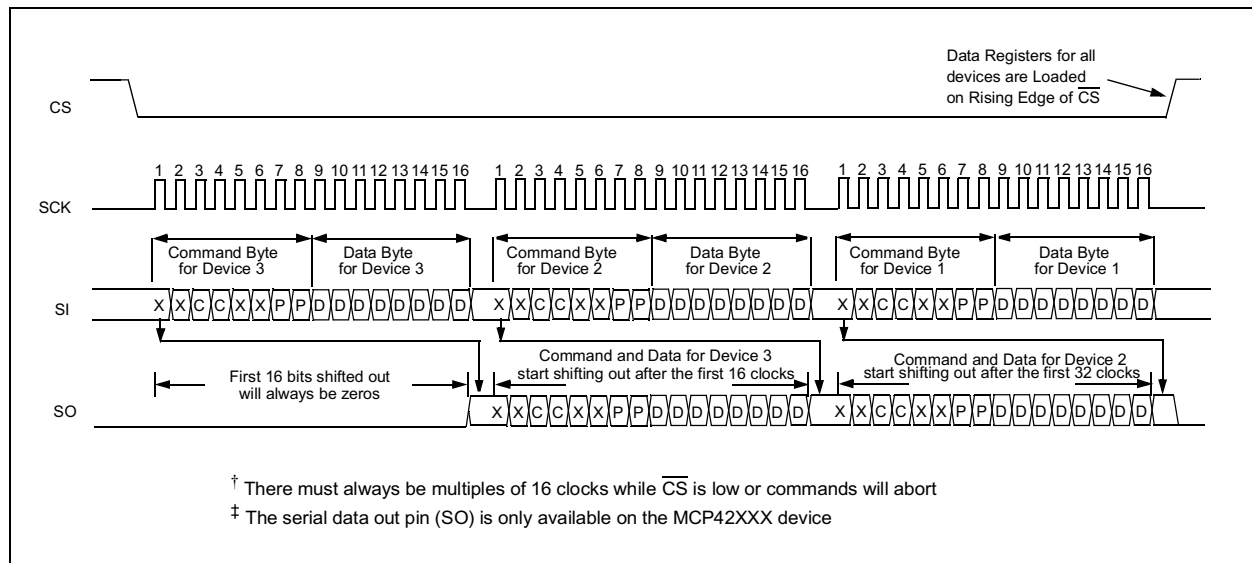
Figure 5-2: Command Byte Format

## 5.4 Daisy-Chain Configuration

Multiple MCP42XXX devices can be connected in a daisy-chain configuration as shown in Figure 5-4, by connecting the SO pin from one device to the SI pin on the next device. The data on the SO pin is the output of the 16-bit shift register. The daisy-chain configuration allows the system designer to communicate with several devices without using a separate CS line for each device. The example shows a daisy chain configuration with three devices, although any number of devices (with or without the same resistor values) can be configured this way. While it is not possible to use a MCP41XXX at the beginning or middle of a daisy-chain because it does not provide the serial data out (SO) pin, it is possible to use the device at the end of a chain. As shown in the timing diagram in Figure 5-3, data will be clocked out of the SO pin on the falling edge of the clock. The SO pin has a CMOS push-pull output and will drive low when  $\overline{CS}$  goes high. SO **will not** go to a high impedance state when  $\overline{CS}$  is held high.

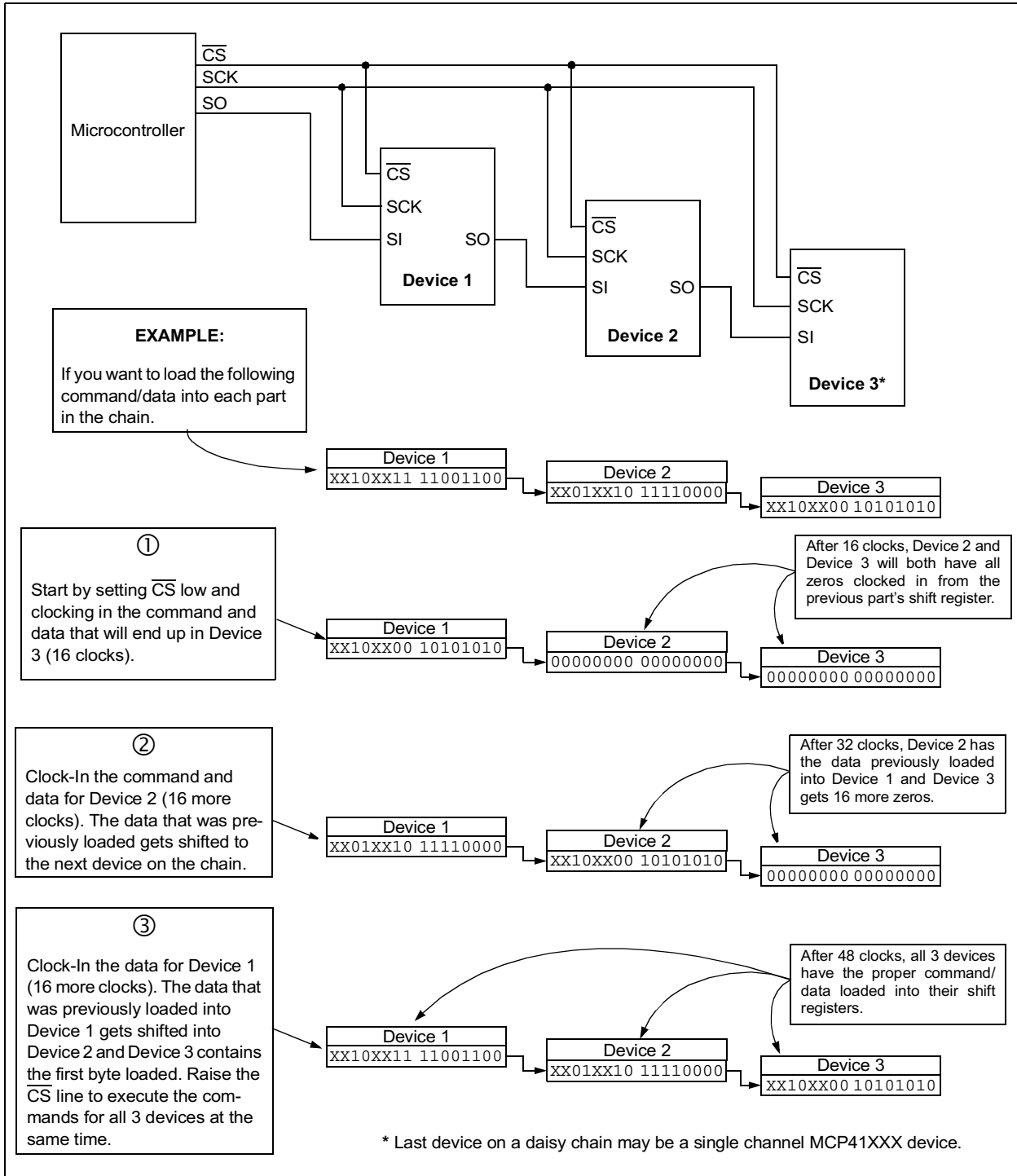
When using the daisy-chain configuration, the maximum clock speed possible is reduced to ~5.8 MHz because of the propagation delay of the data coming out of the SO pin.

When using the daisy-chain configuration, keep in mind that the shift register of each device is automatically loaded with zeros whenever a command is executed ( $\overline{CS} = \text{high}$ ). Because of this, the first 16 bits that come out of the SO pin after the  $\overline{CS}$  line goes low will always be zeros. This means that when the first command is being loaded into a device, it will always shift a NOP command into the next device on the chain because the command bits (and all the other bits) will be zeros. This feature makes it necessary only to send command and data bytes to the device farthest down the chain that needs a new command. For example, if there were three devices on the chain and it was desired to send a command to the device in the middle, only 32 bytes of data need to be transmitted. The last device on the chain will have a NOP loaded from the previous device so no registers will be affected when the  $\overline{CS}$  pin is raised to execute the command. **The user must always ensure that multiples of 16 clocks are always provided (while  $\overline{CS}$  is low) as all commands will abort if the number of clocks provided is not a multiple of 16.**



**Figure 5-3:** Timing Diagram for Daisy-Chain Configuration

# MCP41XXX/42XXX



**Figure 5-4:** Daisy-Chain Configuration

## 5.5 Reset ( $\overline{RS}$ ) Pin Operation

The Reset pin ( $\overline{RS}$ ) will automatically set all potentiometer data latches to mid scale (Code 80h) when pulled low (provided that the pin is held low at least 150 ns and  $\overline{CS}$  is high). The reset will execute regardless of the position of the SCK,  $\overline{SHDN}$  and SI pins. It is possible to toggle  $\overline{RS}$  low and back high while  $\overline{SHDN}$  is low. In this case, the potentiometer registers will reset to mid-scale but the potentiometer will remain in shutdown mode until the  $\overline{SHDN}$  pin is raised.

**Note:** Bringing the  $\overline{RS}$  pin low while the  $\overline{CS}$  pin is low constitutes an invalid operating state and will result in indeterminate results when  $\overline{RS}$  and/or  $\overline{CS}$  are brought high.

## 5.6 Shutdown ( $\overline{SHDN}$ ) Pin Operation

When held low, the shutdown pin causes the application circuit to go into a power saving mode by open circuiting the A terminal and shorting the B and W terminals for all potentiometers. Data register contents are not affected by entering shutdown mode, i.e., when the  $\overline{SHDN}$  pin is raised, the data register contents are the same as before the shutdown mode was entered.

While in shutdown mode, it is still possible to clock in new values for the data registers as well as toggling the  $\overline{RS}$  pin to cause all data registers to go to mid-scale. The new values will take affect when the  $\overline{SHDN}$  pin is raised.

If the device is powered up with the  $\overline{SHDN}$  pin held low, it will power up in the shutdown mode with the data registers set to mid-scale.

**Note:** Bringing the  $\overline{SHDN}$  pin low while the  $\overline{CS}$  pin is low constitutes an invalid operating state and will result in indeterminate results when  $\overline{SHDN}$  and/or  $\overline{CS}$  are brought high.

## 5.7 Power-up Considerations

When the device is powered on, the data registers will be set to mid-scale (80h). A power-on reset circuit is utilized to insure that the device powers up in this known state.

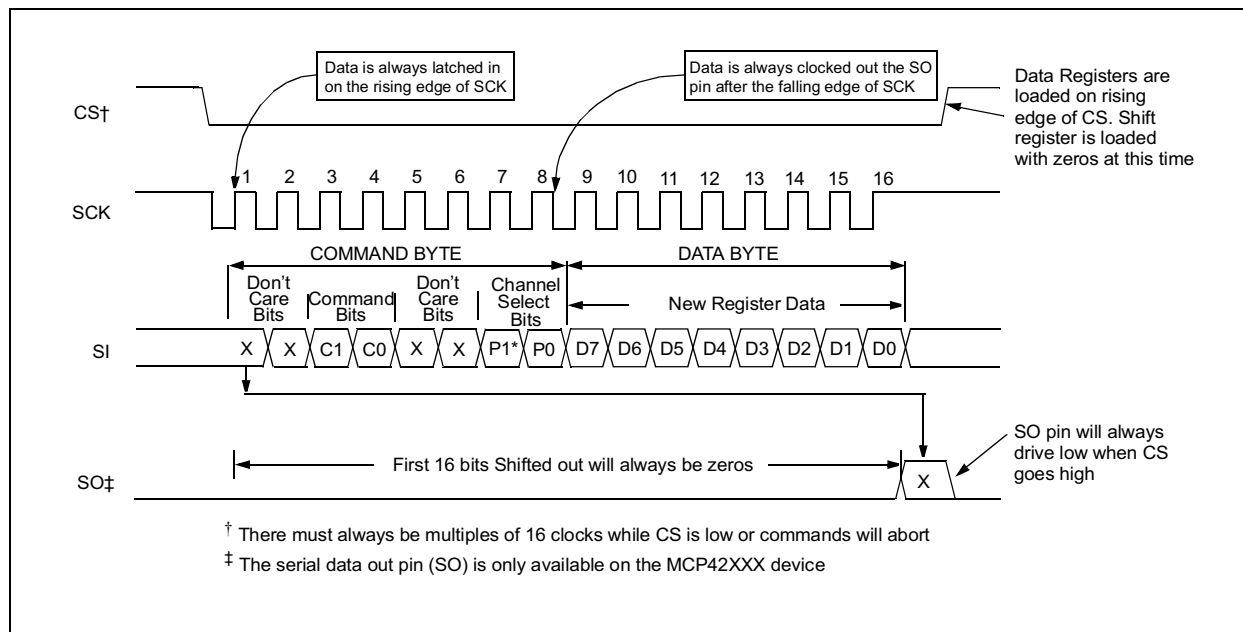
**Table 5-1** Truth Table for Logic Inputs

SCK	$\overline{CS}$	$\overline{RS}$	$\overline{SHDN}$	Action
X	$\emptyset$	H	H	Communication is initiated with device. Device comes out of standby mode.
L	L	H	H	No action, device is waiting for data to be clocked into shift register or $\overline{CS}$ to go high to execute command.
1	L	H	X	Shift one bit into shift register. The shift register can be loaded while the $\overline{SHDN}$ pin is low.
$\emptyset$	L	H	X	Shift one bit out of shift register on the SO pin. The SO pin is active while the $\overline{SHDN}$ pin is low.
X	1	H	H	Based on command bits, either load data from shift register into data latches or execute shutdown command. Neither command executed unless multiples of 16 clocks have been entered while $\overline{CS}$ is low. SO pin goes to a logic low.
X	H	H	H	Static Operation
X	H	$\emptyset$	H	All data registers set and latched to code 80h.
X	H	$\emptyset$	L	All data registers set and latched to code 80h. Device is in hardware shutdown mode and will remain in this mode.
X	H	H	$\emptyset$	All potentiometers put into hardware shutdown mode; terminal A is open and W is shorted to B
X	H	H	1	All potentiometers exit hardware shutdown mode. Potentiometers will also exit software shutdown mode if this rising edge occurs after a low pulse on $\overline{CS}$ . Contents of data latches are restored.

# MCP41XXX/42XXX

## 5.8 Using the MCP41XXX/42XXX in SPI Mode 1,1

It is possible to operate the devices in SPI modes 0,0 and 1,1. The only difference between these two modes is that when using mode 1,1 the clock idles in the high state and in mode 0,0 the clock idles in the low state. In both modes, data is clocked into the devices on the rising edge of SCK and data is clocked out the SO pin after the falling edge of SCK. Operations using mode 0,0 are shown in Figure 5-1. The example in Figure 5-5 shows mode 1,1.



**Figure 5-5:** Timing Diagram for SPI Mode 1,1 Operation

## 6.0 PACKAGING INFORMATION

### 6.1 Package Marking Information

8-Lead PDIP (300 mil)



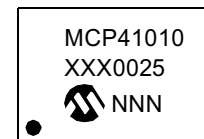
Example



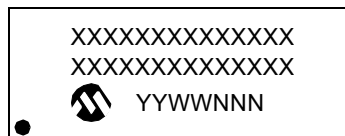
8-Lead SOIC (150 mil)



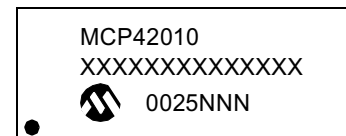
Example



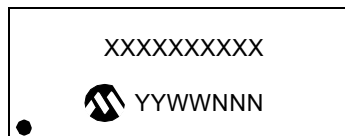
14-Lead PDIP (300 mil)



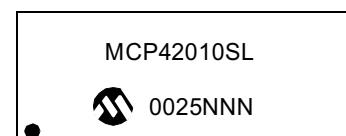
Example



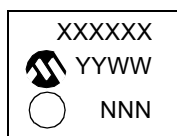
14-Lead SOIC (150 mil)



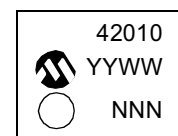
Example



14-Lead TSSOP



Example

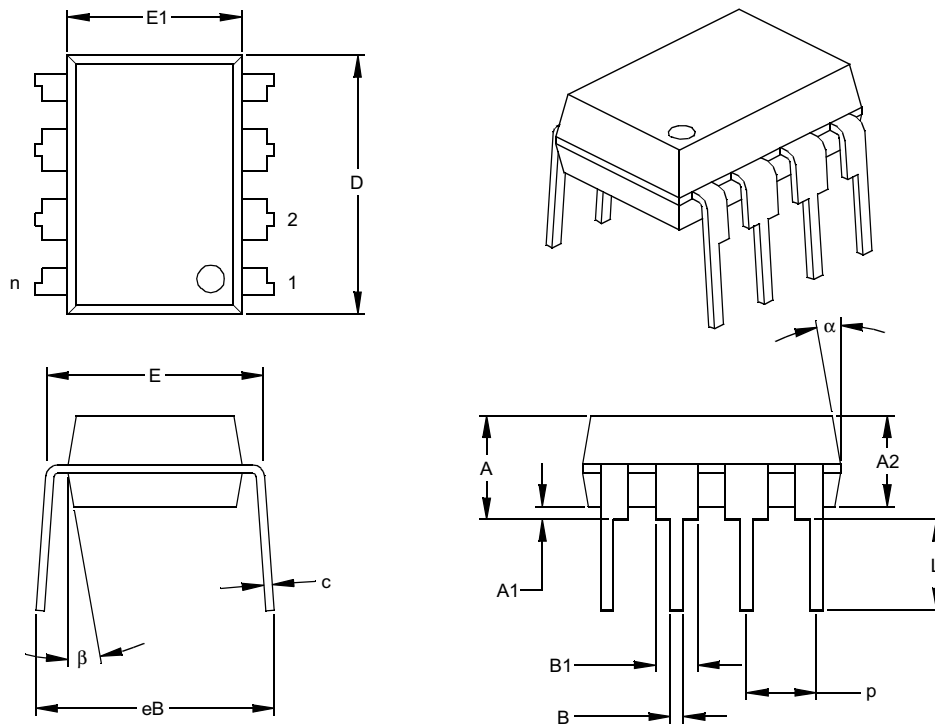


<b>Legend:</b>	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
<b>Note:</b>	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.	

\* Standard OTP marking consists of Microchip part number, year code, week code, facility code, mask rev#, and assembly code.

# MCP41XXX/42XXX

## 8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)



Units		INCHES*			MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing	§ eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

\* Controlling Parameter

§ Significant Characteristic

### Notes:

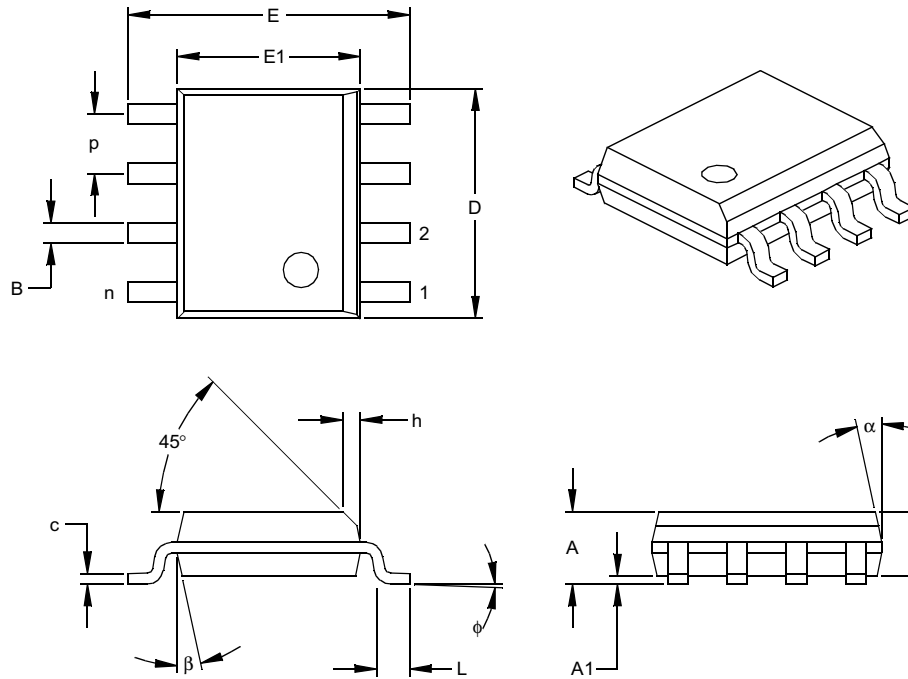
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-001

Drawing No. C04-018

# MCP41XXX/42XXX

## 8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

\* Controlling Parameter

§ Significant Characteristic

Notes:

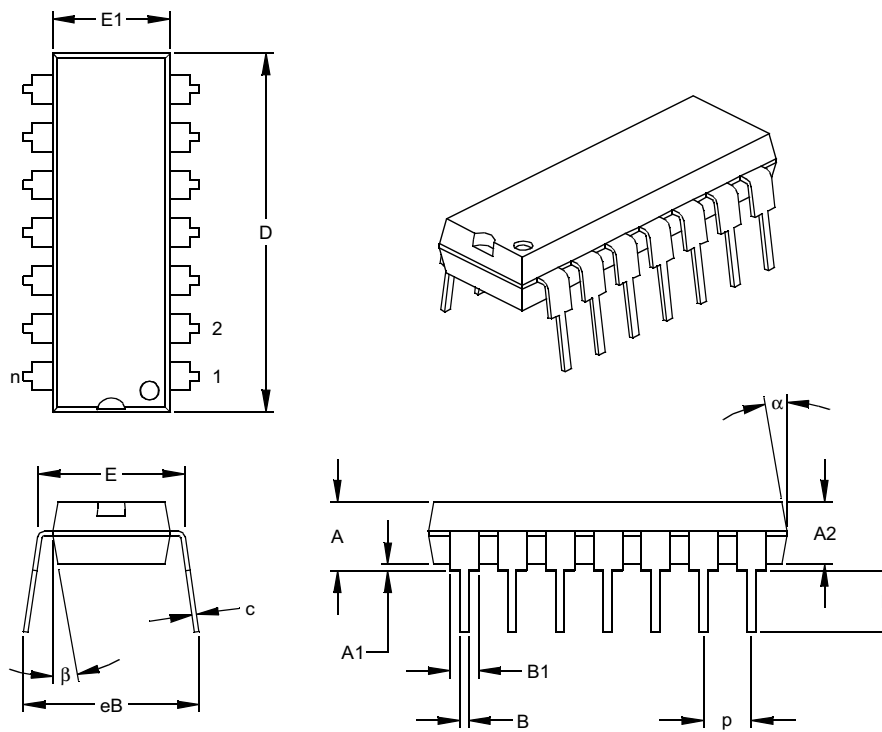
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-012

Drawing No. C04-057

# MCP41XXX/42XXX

## 14-Lead Plastic Dual In-line (P) – 300 mil (PDIP)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.740	.750	.760	18.80	19.05	19.30
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing	§ eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

\* Controlling Parameter

§ Significant Characteristic

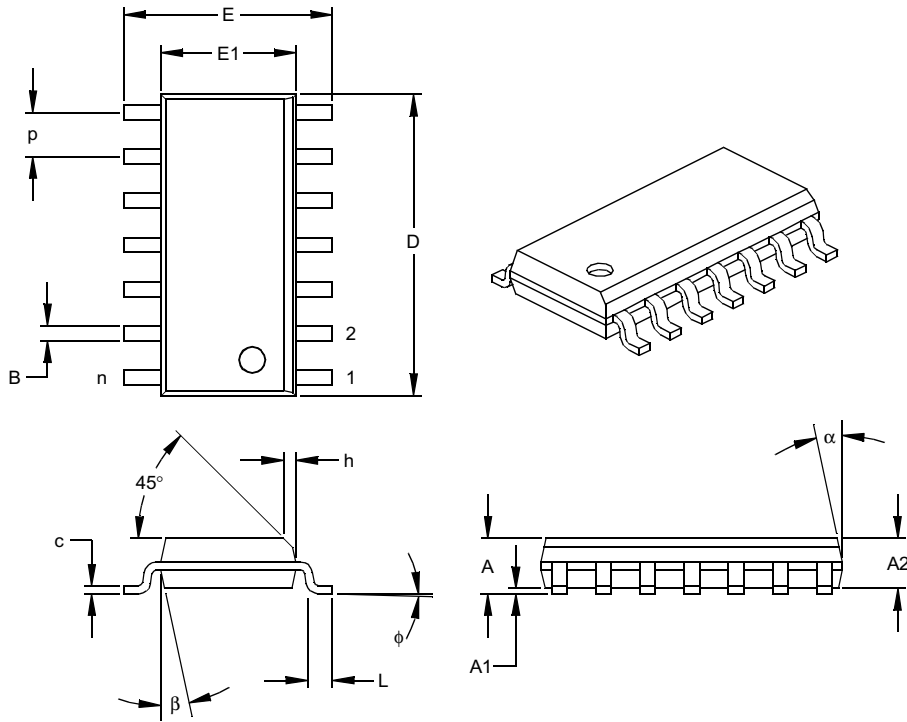
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-001

Drawing No. C04-005

## 14-Lead Plastic Small Outline (SL) – Narrow, 150 mil (SOIC)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.236	.244	5.79	5.99	6.20
Molded Package Width	E1	.150	.154	.157	3.81	3.90	3.99
Overall Length	D	.337	.342	.347	8.56	8.69	8.81
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

\* Controlling Parameter

§ Significant Characteristic

Notes:

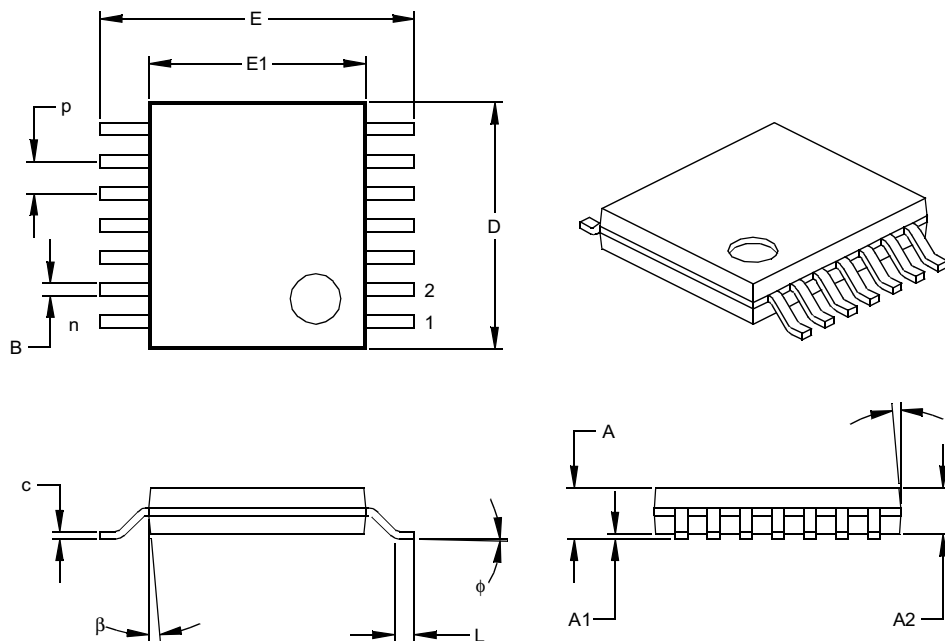
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-012

Drawing No. C04-065

# MCP41XXX/42XXX

## 14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.026			0.65	
Overall Height	A			.043			1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.193	.197	.201	4.90	5.00	5.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B1	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

\* Controlling Parameter

§ Significant Characteristic

### Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side.

JEDEC Equivalent: MO-153

Drawing No. C04-087

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## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>X</u>	<u>/XX</u>
Device	Temperature Range	Package
<div>Device:  MCP41010: Single Digital Potentiometer (10 k<math>\Omega</math>) MCP41010T: Single Digital Potentiometer (10 k<math>\Omega</math>) (Tape and Reel) MCP41050: Single Digital Potentiometer (50 k<math>\Omega</math>) (Tape and Reel) MCP41050T: Single Digital Potentiometer (50 k<math>\Omega</math>) (Tape and Reel) MCP41100: Single Digital Potentiometer (100 k<math>\Omega</math>) (Tape and Reel) MCP41100T: Single Digital Potentiometer (100 k<math>\Omega</math>) (Tape and Reel)  MCP42010: Dual Digital Potentiometer (10 k<math>\Omega</math>) MCP42010T: Dual Digital Potentiometer (10 k<math>\Omega</math>) (Tape and Reel) MCP42050: Dual Digital Potentiometer (50 k<math>\Omega</math>) (Tape and Reel) MCP42050T: Dual Digital Potentiometer (50 k<math>\Omega</math>) (Tape and Reel) MCP42100: Dual Digital Potentiometer (100 k<math>\Omega</math>) (Tape and Reel) MCP42100T: Dual Digital Potentiometer (100 k<math>\Omega</math>) (Tape and Reel)</div> <div>Temperature Range: I = -40°C to +85°C</div> <div>Package: P = Plastic DIP (300 mil Body), 8-lead, 14-lead SN = Plastic SOIC (150 mil Body), 8-lead SL = Plastic SOIC (150 mil Body), 14-lead ST = TSSOP (4.4mm Body), 14-lead</div>		
<div><b>Examples:</b>  a) MCP41010-I/P: Industrial Temperature, PDIP package. b) MCP41010-I/SN: Industrial Temperature, SOIC 8-lead package. c) MCP41010T-I/SN: Tape and Reel, Industrial Temperature, SOIC package. d) MCP42010-I/SL: Industrial Temperature, SOIC 14-lead package. e) MCP42050-I/ST: Industrial Temperature, TSSOP package.</div>		

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# MCP41XXX/42XXX

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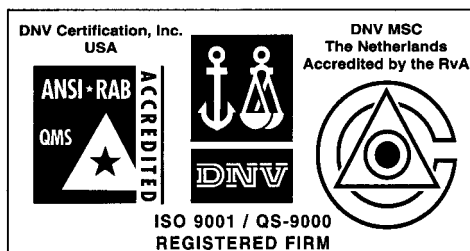
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