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ON Semiconductor®

FCB070N65S3

N-Channel SuperFET® III MOSFET

650 V, 44 A, 70 mΩ

Features

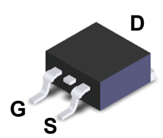
- 700 V @ T_J = 150 °C
- $R_{DS(on)}$ = 62 mΩ (Typ.)
- Ultra Low Gate Charge (Typ. Q_g = 78 nC)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)}$ = 715 pF)
- 100% Avalanche Tested
- RoHS Compliant

Applications

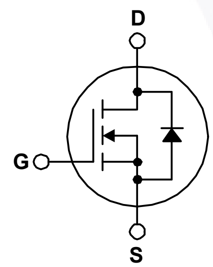
- Telecom / Server Power Supplies
- Industrial Power Supplies
- UPS / Solar

Description

SuperFET® III MOSFET is ON Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advance technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate. Consequently, SuperFET III MOSFET is very suitable for various AC/DC power conversion for system miniaturization and higher efficiency.



D²-PAK



Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter		FCB070N65S3	Unit
V_{DSS}	Drain to Source Voltage		650	V
V_{GSS}	Gate to Source Voltage	- DC	±30	V
		- AC (f>1 Hz)	±30	
I_D	Drain Current	- Continuous (T_C = 25°C)	44	A
		- Continuous (T_C = 100°C)	28	
I_{DM}	Drain Current	- Pulsed (Note 1)	110	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		214	mJ
I_{AS}	Avalanche Current (Note 1)		4.8	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		3.12	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt (Note 3)		20	
P_D	Power Dissipation	(T_C = 25°C)	312	W
		- Derate Above 25°C	2.5	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	°C

Thermal Characteristics

Symbol	Parameter	FCB070N65S3	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.4	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Minimum Pad of 2-oz Copper), Max.	62.5	
	Thermal Resistance, Junction to Ambient (1 in² Pad of 2-oz Copper), Max.	40	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCB070N65S3	FCB070N65S3	D^2-PAK	Tape and Reel	330 mm	24 mm	800 units

Electrical Characteristics $T_C = 25^oC$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit

Off Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 1 mA, T_J = 25°C	650	-	-	V
		V_{GS} = 0 V, I_D = 1 mA, T_J = 150°C	700	-	-	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 1 mA, Referenced to 25°C	-	0.72	-	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 650 V, V_{GS} = 0 V	-	-	1	μA
		V_{DS} = 520 V, V_{GS} = 0 V, T_C = 125°C	-	2.2	-	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±30 V, V_{DS} = 0 V	-	-	±100	nA

On Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, I_D = 4.4 mA	2.5	-	4.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 22 A	-	62	70	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 20 V, I_D = 22 A	-	29	-	S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input Capacitance	V_{DS} = 400 V, V_{GS} = 0 V, f = 1 MHz	-	3090	-	pF
C_{oss}	Output Capacitance		-	68	-	pF
$C_{oss(eff.)}$	Effective Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	-	715	-	pF
$C_{oss(er.)}$	Energy Related Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	-	104	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	V_{DS} = 400 V, I_D = 22 A, V_{GS} = 10 V (Note 4)	-	78	-	nC
Q_{gs}	Gate to Source Gate Charge		-	18	-	nC
Q_{gd}	Gate to Drain “Miller” Charge		-	30	-	nC
ESR	Equivalent Series Resistance	f = 1 MHz	-	0.6	-	Ω

Switching Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 400 V, I_D = 22 A, V_{GS} = 10 V, R_g = 4.7 Ω (Note 4)	-	26	-	ns
t_r	Turn-On Rise Time		-	52	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	89	-	ns
t_f	Turn-Off Fall Time		-	16	-	ns

Drain-Source Diode Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_S	Maximum Continuous Source to Drain Diode Forward Current		-	-	44	A
I_{SM}	Maximum Pulsed Source to Drain Diode Forward Current		-	-	110	A
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 22 A	-	-	1.2	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 22 A, dI_F/dt = 100 A/μs	-	435	-	ns
Q_{rr}	Reverse Recovery Charge		-	9.2	-	μC

Notes:

1. Repetitive rating: pulse width limited by maximum junction temperature.
2. I_{AS} = 4.8 A, R_G = 25 Ω, starting T_J = 25°C.
3. $I_{SD} \leq$ 44 A, di/dt $\leq$ 200 A/μs, $V_{DD} \leq BV_{DSS}$, starting T_J = 25°C.
4. Essentially independent of operating temperature typical characteristic.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

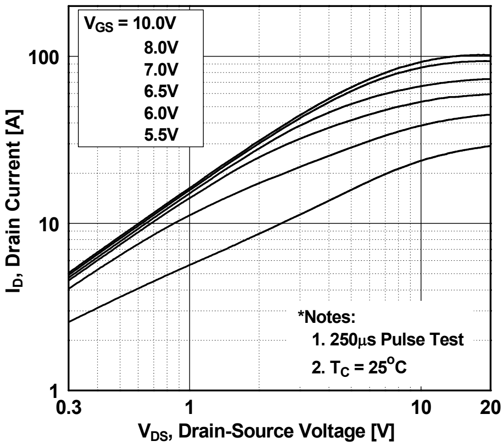


Figure 2. Transfer Characteristics

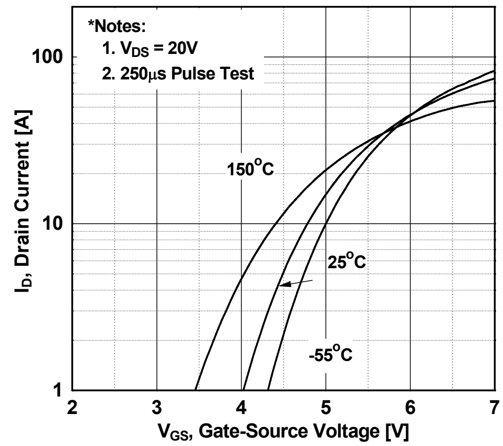


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

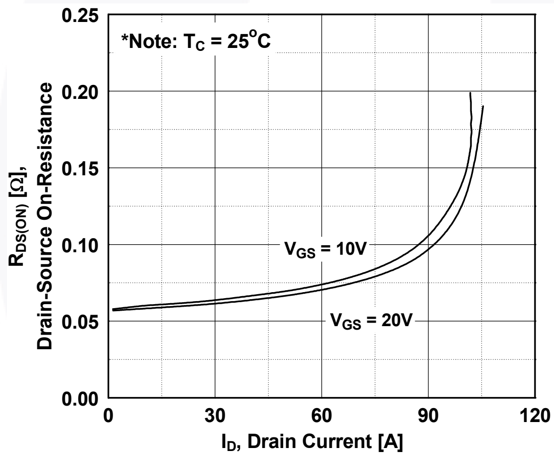


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

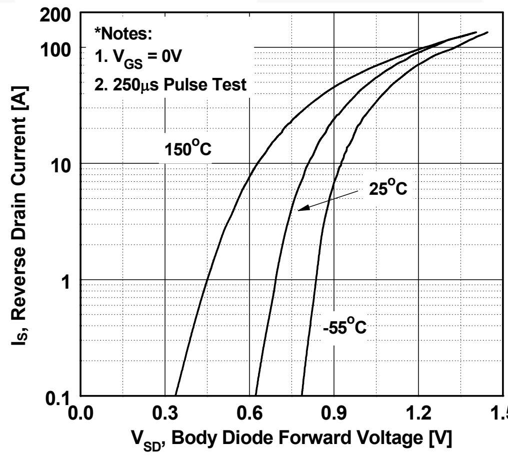


Figure 5. Capacitance Characteristics

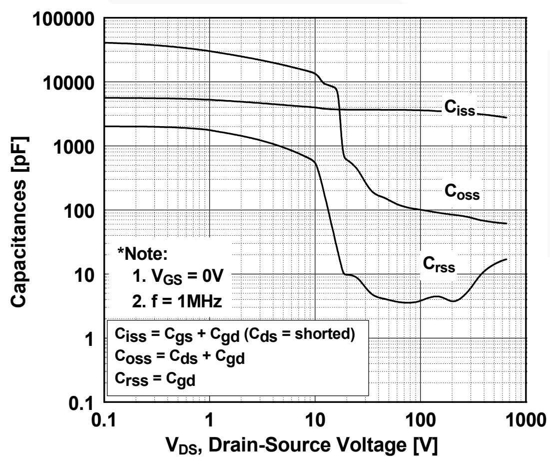
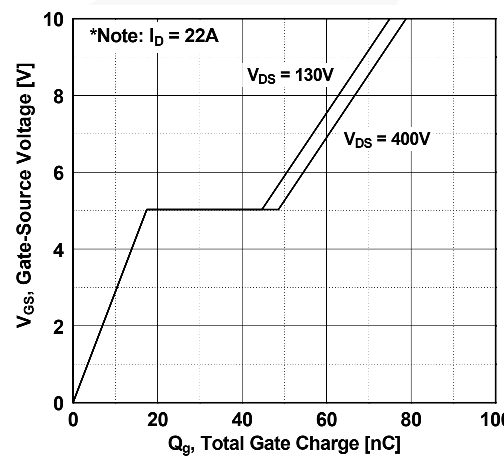


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

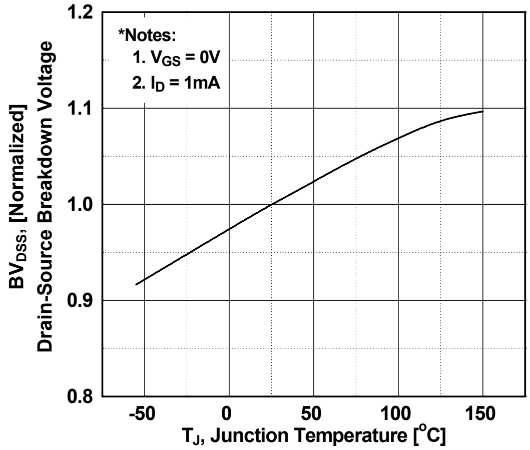


Figure 8. On-Resistance Variation vs. Temperature

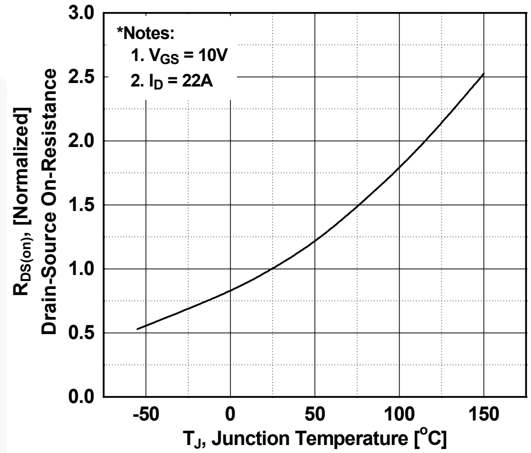


Figure 9. Maximum Safe Operating Area

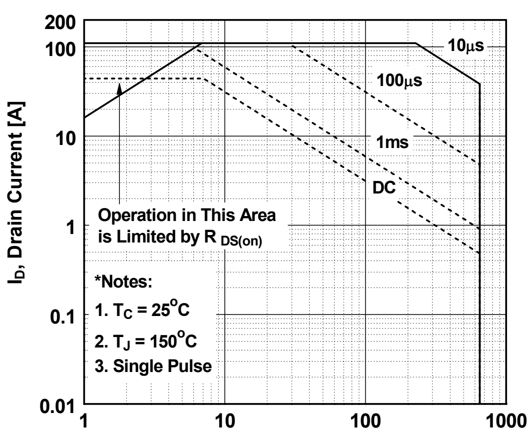


Figure 10. Maximum Drain Current vs. Case Temperature

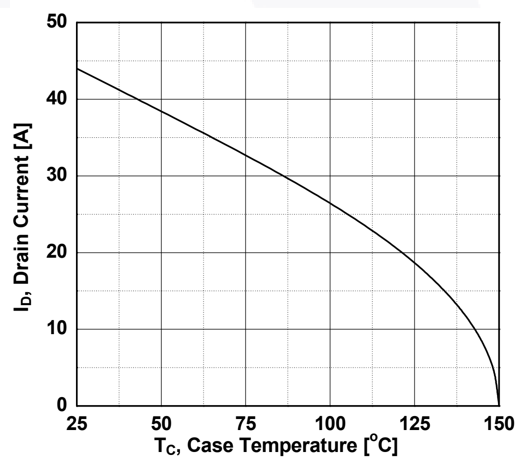
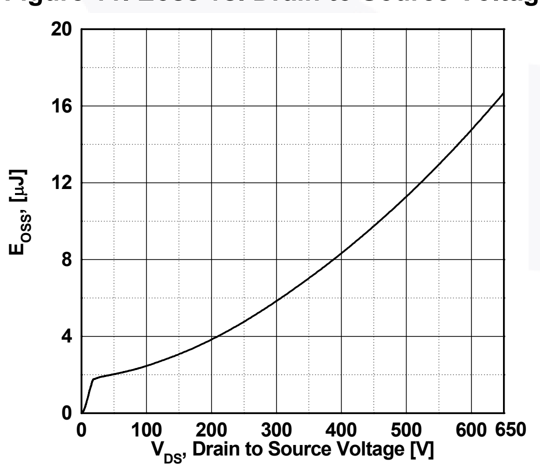
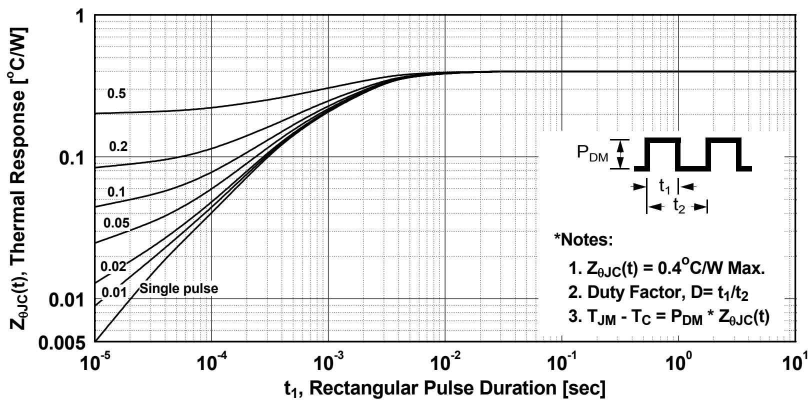


Figure 11. Eoss vs. Drain to Source Voltage



Typical Performance Characteristics (Continued)

Figure 12. Transient Thermal Response Curve



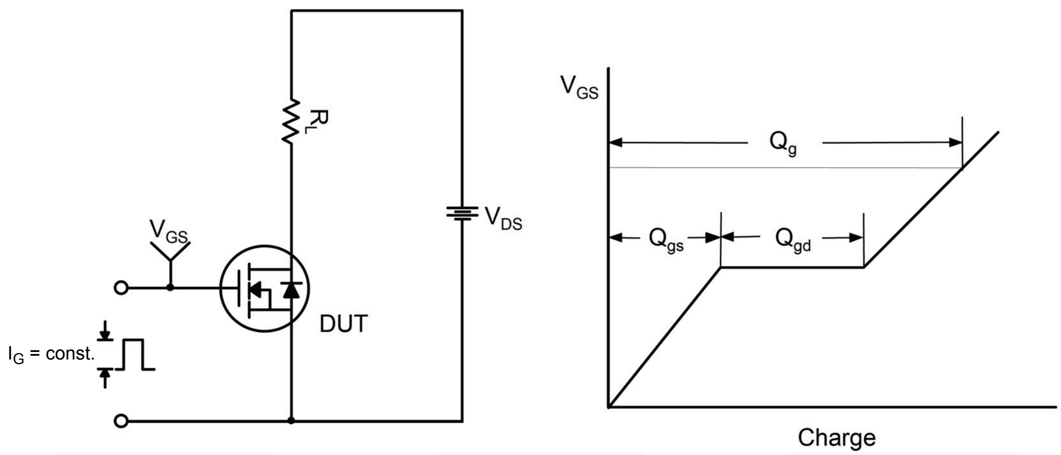


Figure 13. Gate Charge Test Circuit & Waveform

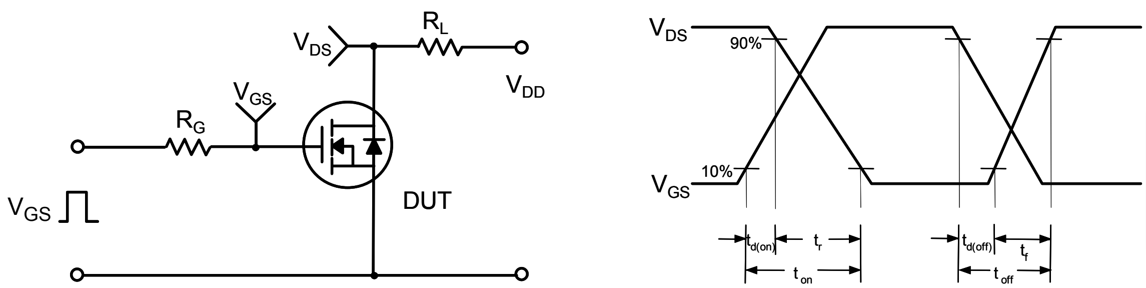


Figure 14. Resistive Switching Test Circuit & Waveforms

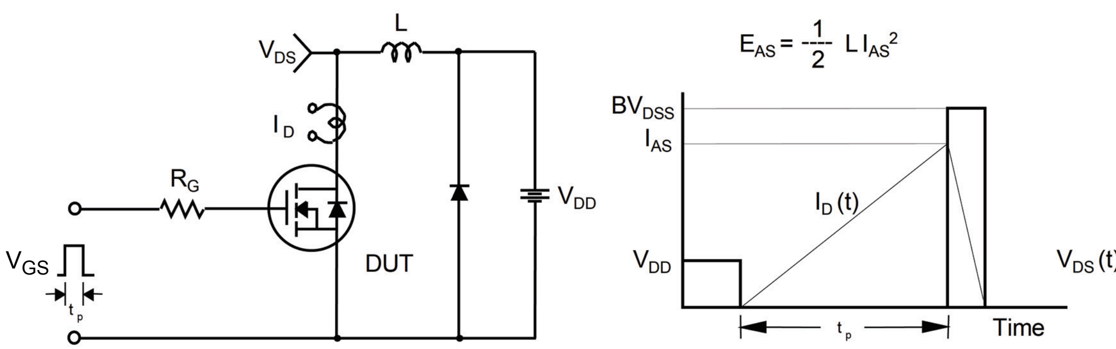


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

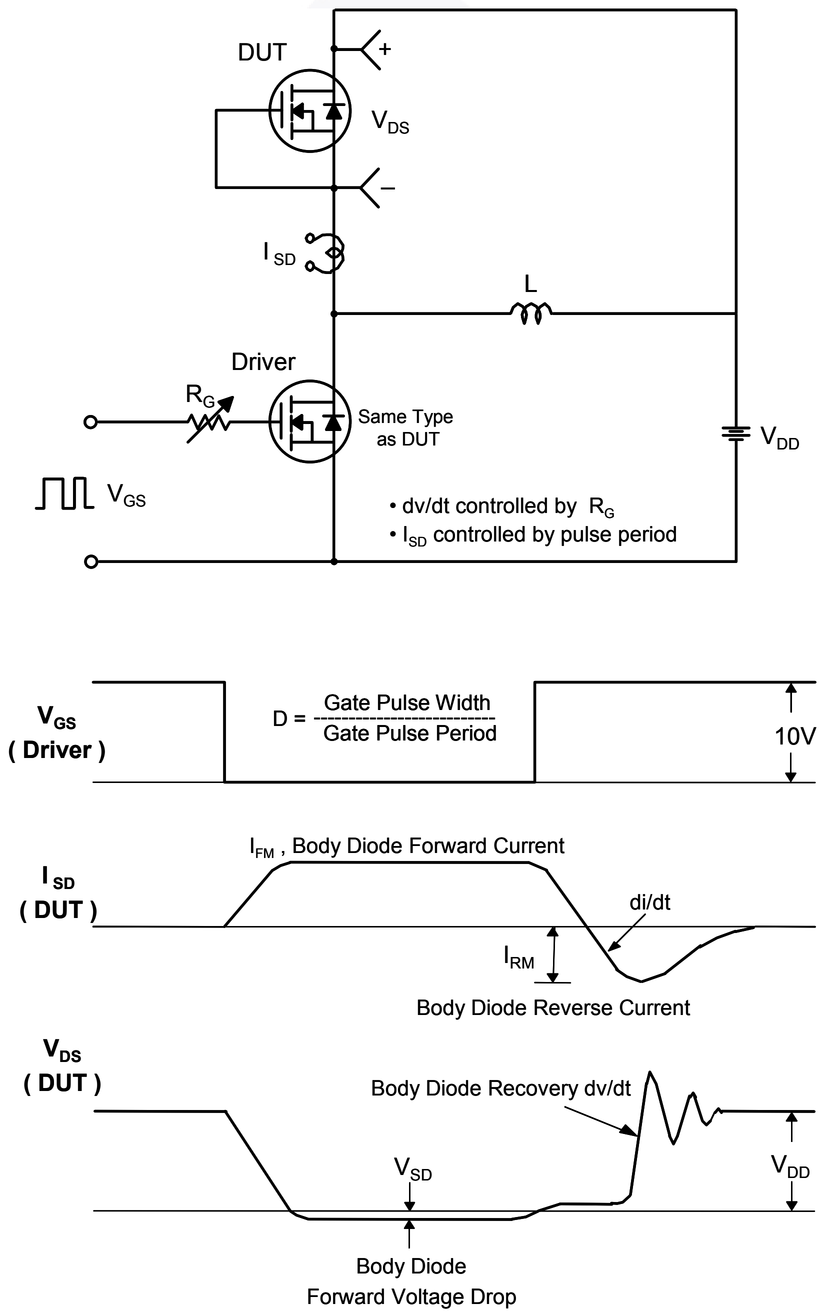
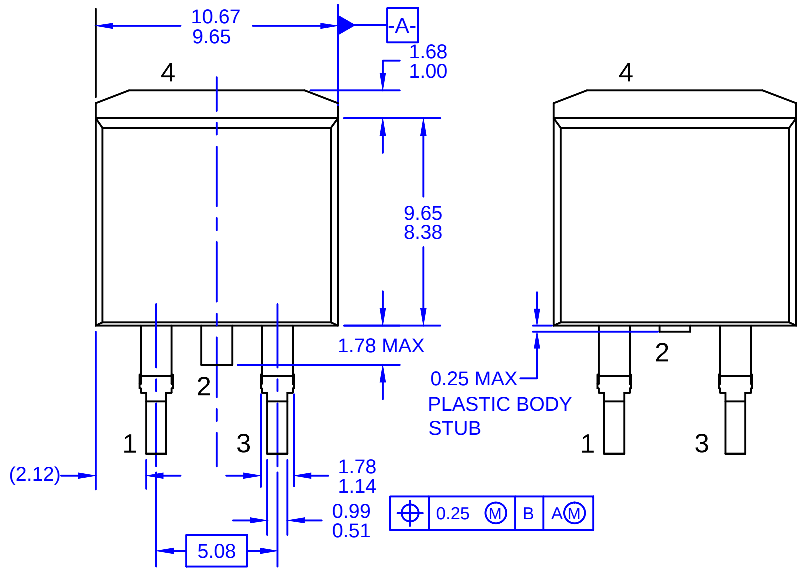
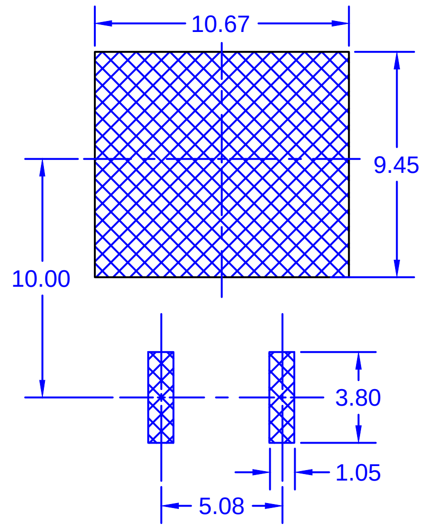


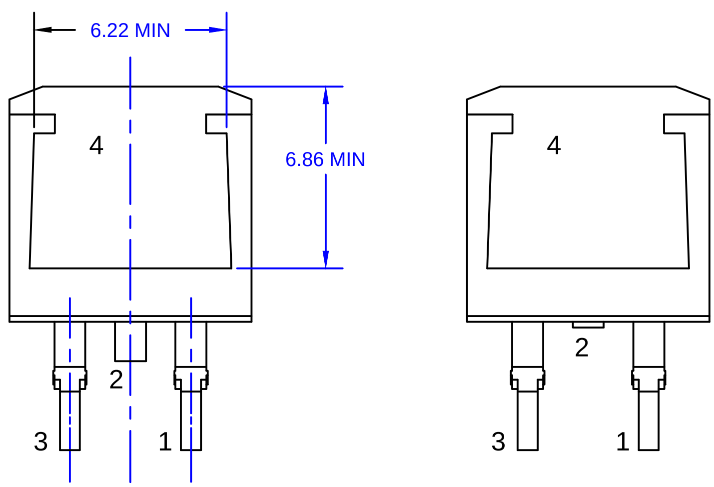
Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms



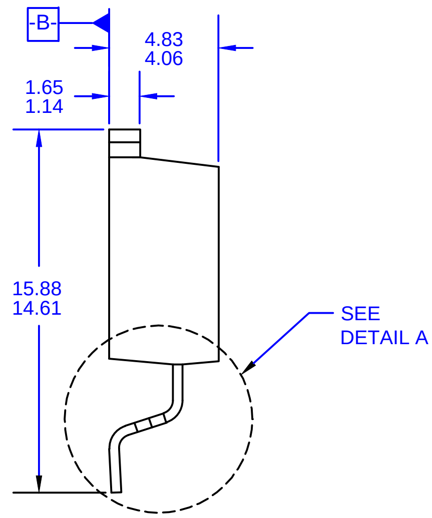
FRONT VIEW - DIODE PRODUCTS VERSION
ALTERNATIVE SUPPLIER DETAIL

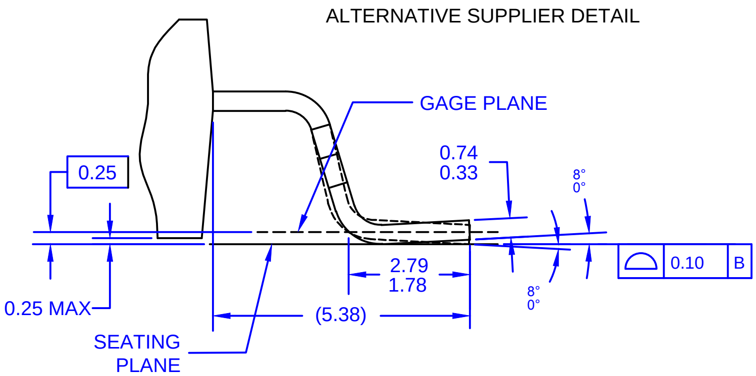


LAND PATTERN RECOMMENDATION
UNLESS NOTED, ALL DIMS TYPICAL



BACK VIEW - DIODE PRODUCTS VERSION
ALTERNATIVE SUPPLIER DETAIL





DETAIL A, ROTATED 90°
SCALE: 2X

NOTES: UNLESS OTHERWISE SPECIFIED

A) ALL DIMENSIONS ARE IN MILLIMETERS.
B) REFERENCE JEDEC, TO-263, VARIATION AB.
C) DIMENSIONING AND TOLERANCING PER DIMENSIONING AND TOLERANCING PER ASME Y14.5 - 2009.
D) LOCATION OF THE PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE).
E) LANDPATTERN RECOMMENDATION PER IPC TO254P1524X482-3N
F) FILENAME: TO263A02REV8

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