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FDP26N40

N-Channel UniFET™ MOSFET

400 V, 26 A, 160 mΩ

Features

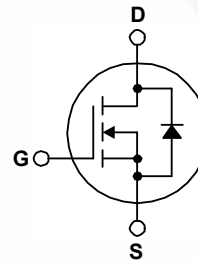
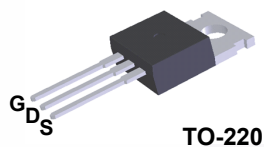
- $R_{DS(on)} = 130 \text{ m}\Omega$ (Typ.) @ $V_{GS} = 10 \text{ V}$, $I_D = 13 \text{ A}$
- Low Gate Charge (Typ. 48 nC)
- Low C_{rss} (Typ. 30 pF)
- 100% Avalanche Tested
- RoHS Compliant

Applications

- Uninterruptible Power Supply
- AC-DC Power Supply

Description

UniFET™ MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FDP26N40	Unit
V_{DSS}	Drain to Source Voltage	400	V
V_{GSS}	Gate to Source Voltage	± 30	V
I_D	Drain Current	- Continuous ($T_C = 25^\circ\text{C}$)	26
		- Continuous ($T_C = 100^\circ\text{C}$)	15.6
I_{DM}	Drain Current	- Pulsed (Note 1)	104
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	1352
I_{AR}	Avalanche Current	(Note 1)	26
E_{AR}	Repetitive Avalanche Energy	(Note 1)	26.5
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	265
		- Derate Above 25°C	2.0
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	FDP26N40	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.5	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDP26N40	FDP26N40	TO-220	Tube	N/A	N/A	50 units

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}, T_J = 25^\circ\text{C}$	400	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, Referenced to 25°C	-	0.5	-	$V/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 400 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	1	μA
		$V_{DS} = 320 \text{ V}, T_C = 125^\circ\text{C}$	-	-	10	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 30 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 13 \text{ A}$	-	0.13	0.16	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 20 \text{ V}, I_D = 13 \text{ A}$	-	25.5	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	2400	3185	pF
C_{oss}	Output Capacitance		-	390	520	pF
C_{rss}	Reverse Transfer Capacitance		-	30	45	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 320 \text{ V}, I_D = 26 \text{ A}, V_{GS} = 10 \text{ V}$	-	48	60	nC
Q_{gs}	Gate to Source Gate Charge		-	15	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		(Note 4)	-	20	-

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 200 \text{ V}, I_D = 26 \text{ A}, V_{GS} = 10 \text{ V}, R_G = 25 \Omega$	-	45	100	ns
t_r	Turn-On Rise Time		-	100	210	ns
$t_{d(off)}$	Turn-Off Delay Time		-	115	240	ns
t_f	Turn-Off Fall Time		(Note 4)	-	66	140

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	26	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	104	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{SD} = 26 \text{ A}$	-	-	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0 \text{ V}, I_{SD} = 26 \text{ A}, di_F/dt = 100 \text{ A}/\mu\text{s}$	-	406	-	ns
Q_{rr}	Reverse Recovery Charge		-	5.17	-	μC

Notes:

- 1: Repetitive rating: pulse-width limited by maximum junction temperature.
- 2: $L = 4 \text{ mH}, I_{AS} = 26 \text{ A}, V_{DD} = 50 \text{ V}, R_G = 25 \Omega$, starting $T_J = 25^\circ\text{C}$.
- 3: $I_{SD} \leq 26 \text{ A}, di/dt \leq 200 \text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$.
- 4: Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

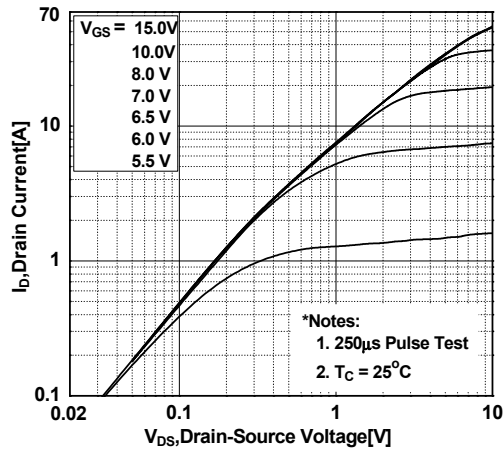


Figure 2. Transfer Characteristics

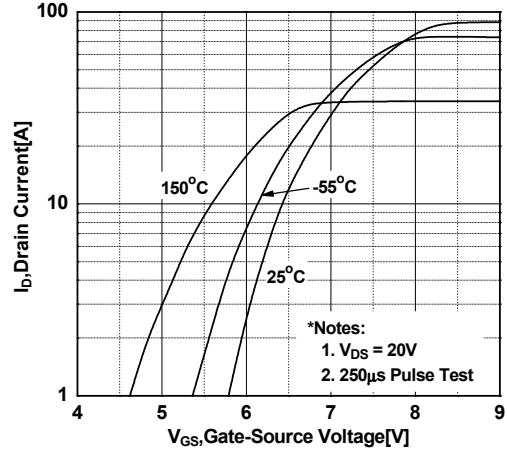


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

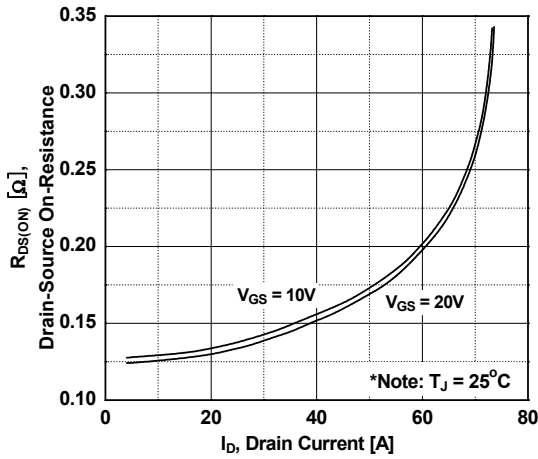


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

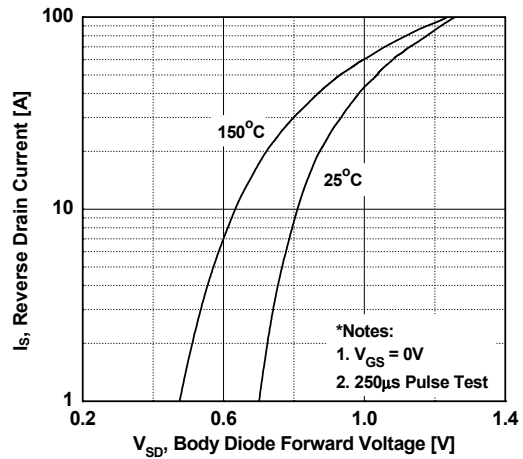


Figure 5. Capacitance Characteristics

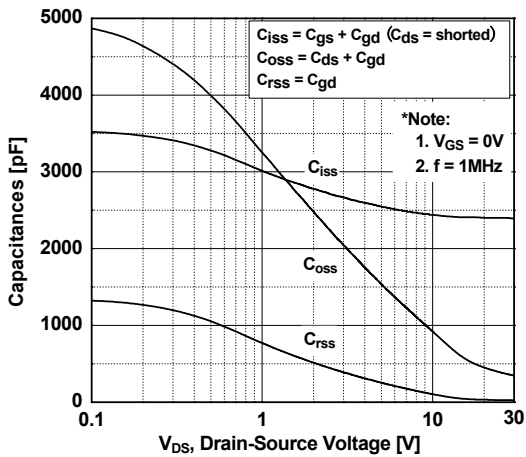
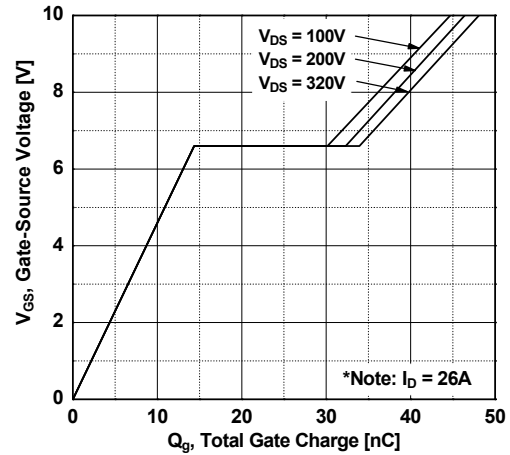


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

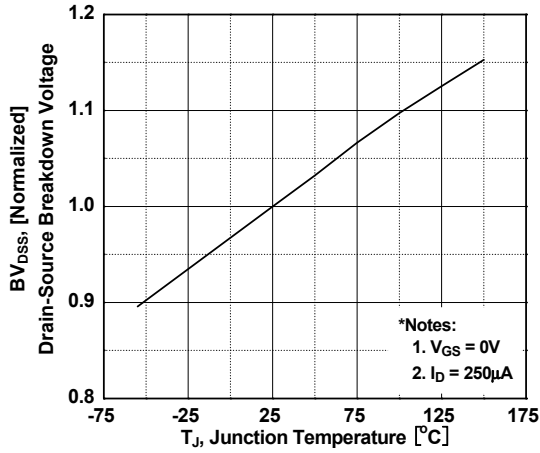


Figure 8. On-Resistance Variation vs. Temperature

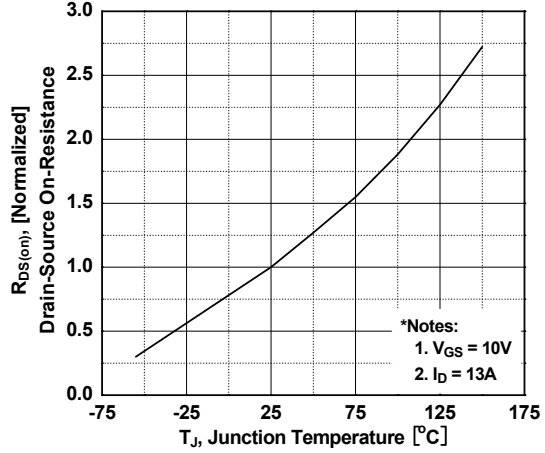


Figure 9. Maximum Safe Operating Area

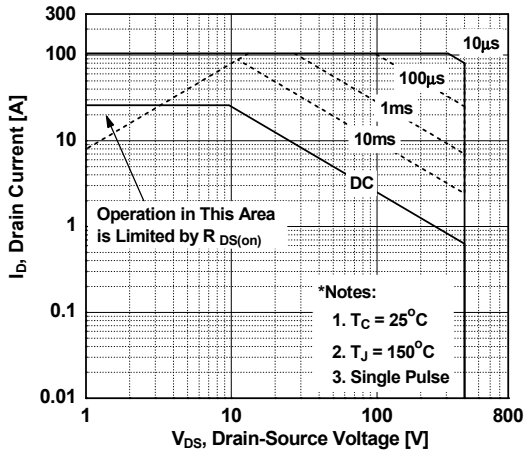


Figure 10. Maximum Drain Current vs. Case Temperature

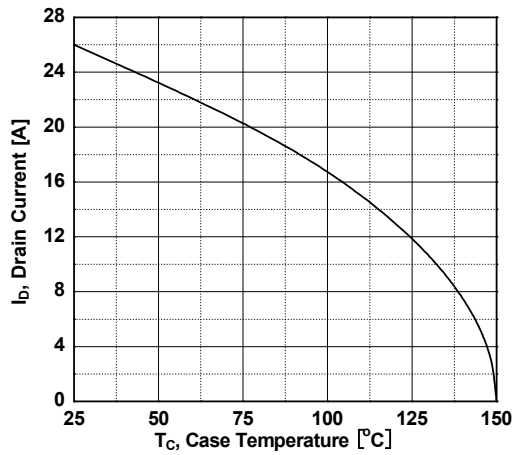
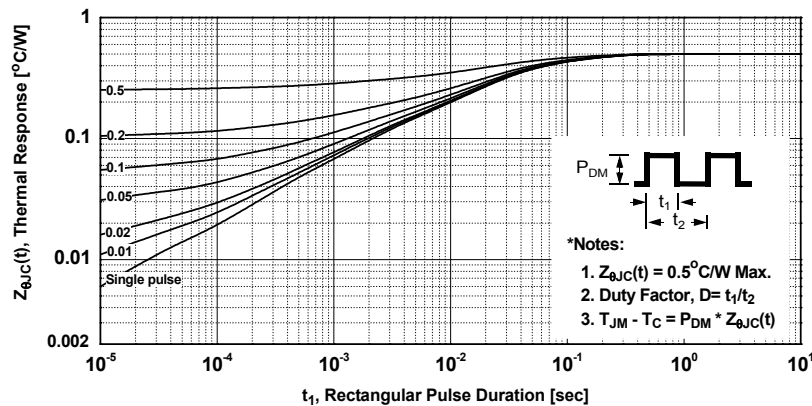


Figure 11. Transient Thermal Response Curve



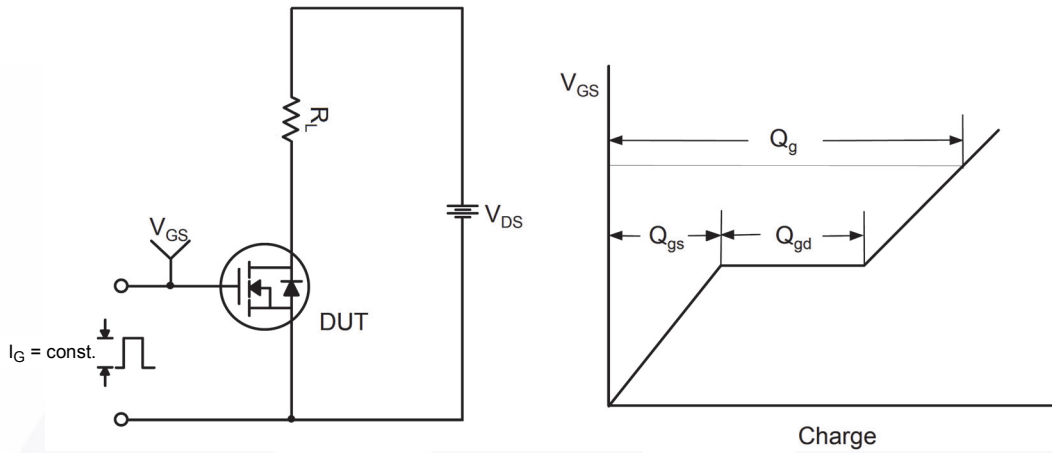


Figure 12. Gate Charge Test Circuit & Waveform

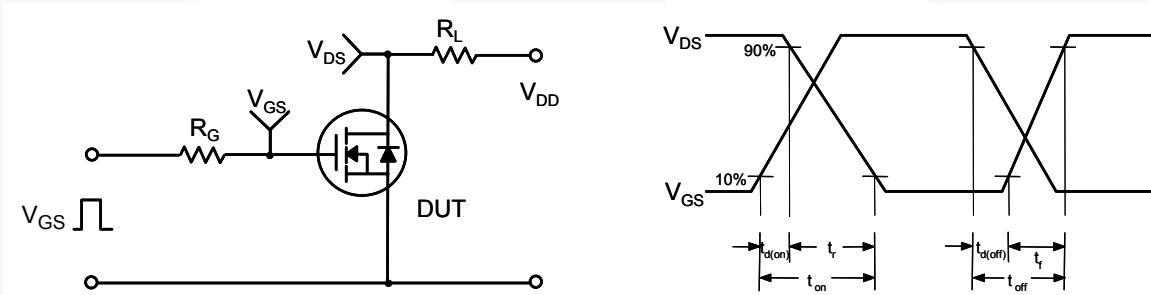


Figure 13. Resistive Switching Test Circuit & Waveforms

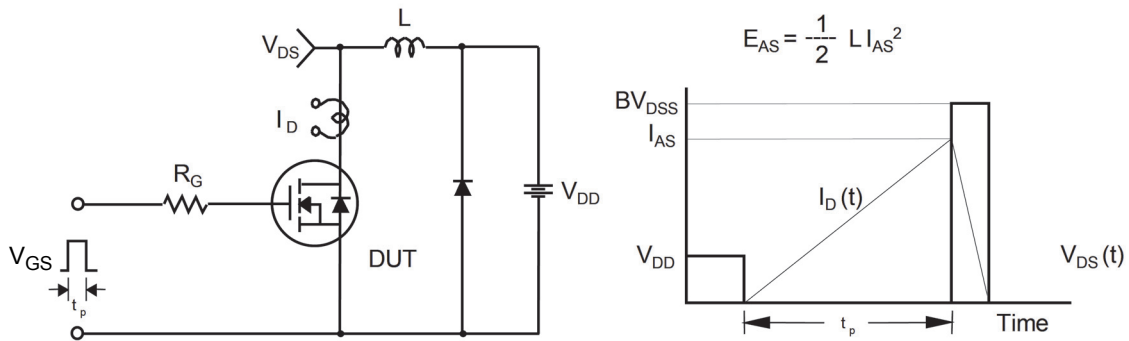
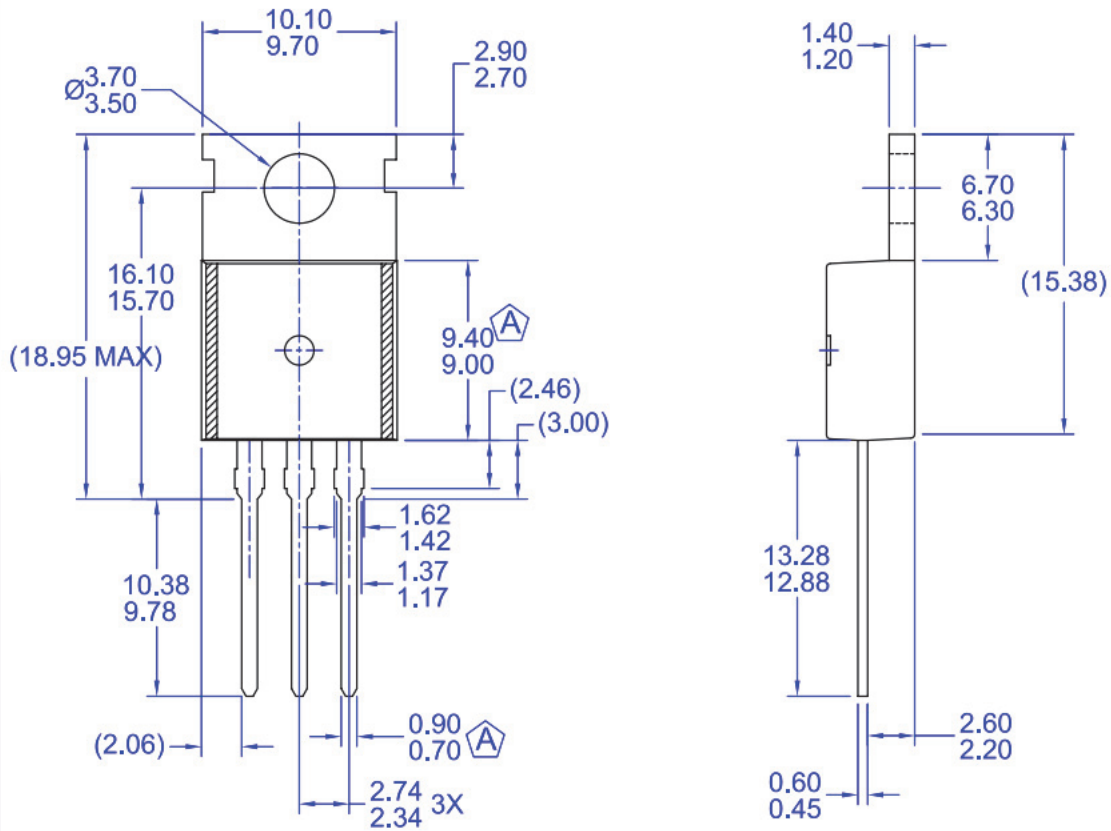


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions



NOTES:

- A) CONFORMS TO JEDEC TO-220 VARIATION AB EXCEPT WHERE NOTED
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D) DRAWING FILE/REVISION: MKT-TO220Y03REV1

Figure 16. TO220, Molded, 3-Lead, Jedec Variation AB

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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