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FAIRCHILD SEMICONDUCTOR®

April 2013

NC7WZ07
TinyLogic® UHS Dual Buffer (Open-Drain Outputs)

Features

- Ultra-High Speed: t_{PZL} 2.3 ns (Typical)
- High I_{OL} Output Drive: ±24 mA at 3 V V_{CC}
- Broad V_{CC} Operating Range: 1.65 V to 5.50 V
- Power Down High Impedance Inputs/Outputs
- Over-Voltage Tolerance Inputs Facilitate 5 V to 3 V Translation
- Proprietary Noise/EMI Reduction Circuitry
- Ultra-Small MicroPak™ Packages

Description

The NC7WZ07 is a dual buffer with open-drain outputs from Fairchild's Ultra-High Speed (UHS) series of TinyLogic®. The device is fabricated with advanced CMOS technology to achieve ultra-high speed with high output drive, while maintaining low static power dissipation over a broad V_{CC} operating range. The device is specified to operate over a very broad V_{CC} operating range. The device is specified to operate over the 1.65 V to 5.5 V V_{CC} range. The inputs and outputs are high impedance when V_{CC} is 0 V. Inputs tolerate voltages up to 7 V independent of V_{CC} operating voltage.

Ordering Information

Part Number	Top Mark	Package	Packing Method
NC7WZ07P6X	Z07	6-Lead SC70, EIAJ SC88 1.25 mm Wide	3000 Units on Tape & Reel
NC7WZ07L6X	D3	6-Lead MicroPak™, 1.00 mm Wide	5000 Units on Tape & Reel
NC7WZ07FHX	D3	6-Lead, MicroPak2™, 1x1 mm Body, .35 mm Pitch	5000 Units on Tape & Reel

Connection Diagrams

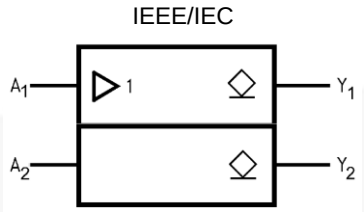


Figure 1. Logic Symbol

Pin Configurations

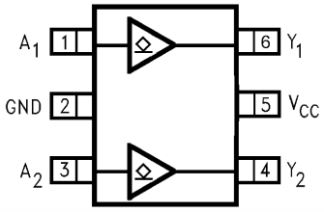


Figure 2. SC70 (Top View)

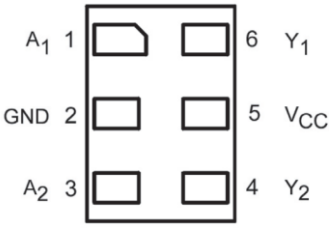


Figure 3. MicroPak™ (Top Through View)

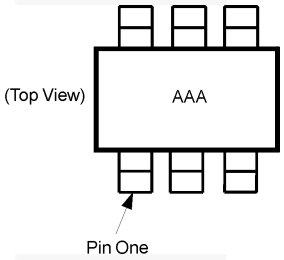


Figure 4. Pin 1 Orientation

Notes:
1. AAA represents product code top mark (*see Ordering Information*).
2. Orientation of top mark determines pin one location.
3. Reading the top mark left to right, pin one is the lower left pin.

Pin Definitions

Pin # SC70	Pin # MicroPak™	Name	Description
1	1	A_1	Input
2	2	GND	Ground
3	3	A_2	Input
4	4	Y_2	Output
5	5	V_{CC}	Supply Voltage
6	6	Y_1	Output

Function Table

Y= A

Inputs	Output
A	**Y**
LOW Logic Level	LOW Logic Level
HIGH Logic Level	High Impedance Output State, Open Drain

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage		-0.5	7.0	V
V_{IN}	DC Input Voltage		-0.5	7.0	V
V_{OUT}	DC Output Voltage		-0.5	7.0	V
I_{IK}	DC Input Diode Current	V_{IN} < -0.5 V		-50	mA
I_{OK}	DC Output Diode Current	V_{OUT} < -0.5 V		-50	mA
I_{OUT}	DC Output Current			±50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current			±100	mA
T_{STG}	Storage Temperature Range		-65	+150	°C
T_J	Junction Temperature Under Bias			+150	°C
T_L	Junction Lead Temperature (Soldering, 10 Seconds)			+260	°C
P_D	Power Dissipation at +85°C	SC70-6		150	mW
		MicroPak™-6		130	
		MicroPak2™-6		120	
ESD	Human Body Model, JEDEC:JESD22-A114			4000	V
	Charge Device Model, JEDEC:JESD22-C101			2000	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{CC}	Supply Voltage Operating		1.65	5.50	V
	Supply Voltage Data Retention		1.5	5.5	
V_{IN}	Input Voltage		0	5.5	V
V_{OUT}	Output Voltage		0	5.5	V
t_r, t_f	Input Rise and Fall Times	V_{CC} at 1.8 V, ±0.15 V, 2.5 V ± 0.2 V	0	20	ns/V
		V_{CC} at 3.3 V ±0.3 V	0	10	
		V_{CC} at 5.0 V ±0.5 V	0	5	
T_A	Operating Temperature		-40	+85	°C
θ_{JA}	Thermal Resistance	SC70-6		425	°C/W
		MicroPak™-6		500	
		MicroPak2™-6		560	

Note:

4. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

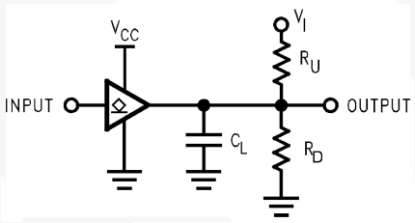
Symbol	Parameter	V_{CC}	Conditions	T_A=+25°C			T_A=-40 to +85°C		Units
				Min.	Typ.	Max.	Min.	Max.	
V_{IH}	HIGH Level Input Voltage	1.65 to 1.95		0.75V_{CC}			0.75V_{CC}		V
		2.30 to 5.50		0.70V_{CC}			0.70V_{CC}		
V_{IL}	LOW Level Input Voltage	1.65 to 1.95				0.25V_{CC}		0.25V_{CC}	V
		2.30 to 5.50				0.30V_{CC}		0.30V_{CC}	
I_{LKG}	HIGH Level Output Leakage Current	1.65 to 5.50	V_{IN}=V_{IH}, V_{OUT}=V_{CC} or GND			±5		±10	µA
V_{OL}	LOW Level Output Voltage	1.65	V_{IN}=V_{IL}, I_{OL}=100 µA		0.00	0.10		0.00	V
		1.80			0.00	0.10		0.10	
		2.30			0.00	0.10		0.10	
		3.00			0.00	0.10		0.10	
		4.50			0.00	0.10		0.10	
		1.65	I_{OL}=4 mA		0.80	0.24		0.24	
		2.30	I_{OL}=8 mA		0.10	0.30		0.30	
		3.00	I_{OL}=16 mA		0.16	0.40		0.40	
		3.00	I_{OL}=24 mA		0.24	0.55		0.55	
		4.50	I_{OL}=32 mA		0.25	0.55		0.55	
I_{IN}	Input Leakage Current	0 to 5.5	0 ≤ V_{IN} ≤ 5.5 V			±0.1		±1.0	µA
I_{OFF}	Power Off Leakage Current	0	V_{IN} or V_{OUT}=5.5 V			1		10	µA
I_{CC}	Quiescent Supply Current	1.65 to 5.50	V_{IN}=5.5 V, GND			1		10	µA

AC Electrical Characteristics

Symbol	Parameter	V_{CC}	Conditions	T_A=+25°C			T_A=-40 to +85°C		Units	Figure
				Min.	Typ.	Max.	Min.	Max.		
t_{PZL}, t_{PLZ}	Propagation Delay	1.65	C_L=50 pF, RU=500 Ω, RD=500 Ω, V_I=2 x V_{CC}	1.8	6.6	11.5	1.8	12.6	ns	Figure 5 Figure 6
		1.80		1.8	5.5	9.5	1.8	10.5		
		2.50 ± 0.20		1.2	3.7	5.8	1.2	6.4		
		3.30 ± 0.30		0.8	2.9	4.4	0.8	4.8		
		5.00 ± 0.50		0.5	2.3	3.5	0.5	3.9		
		1.65	C_L=50 pF, RU=500 Ω, RD=500 Ω, V_I=2 x V_{CC}	1.8	5.5	11.5	1.8	12.6		
		1.80		1.8	4.3	9.5	1.8	10.5		
		2.50 ± 0.20		1.2	2.8	5.8	1.2	6.4		
		3.30 ± 0.30		0.8	2.1	4.4	0.8	4.8		
		5.00 ± 0.50		0.5	1.4	3.5	0.5	3.9		
C_{IN}	Input Capacitance	0			2.5				pF	
C_{OUT}	Output Capacitance	0			4.0					
C_{PD}	Power Dissipation Capacitance(5)	3.30			3				pF	Figure 7
		5.00			4					

Note:

5. C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. C_{PD} is related to I_{CCD} dynamic operating current by the expression: $I_{CCD}=(C_{PD})(V_{CC})(f_{IN})+(I_{CC}static)$.



Notes:

6. C_L includes load and stray capacitance.
7. Input PRR = 1.0MHz, t_W = 500ns.

Figure 5. AC Test Circuit

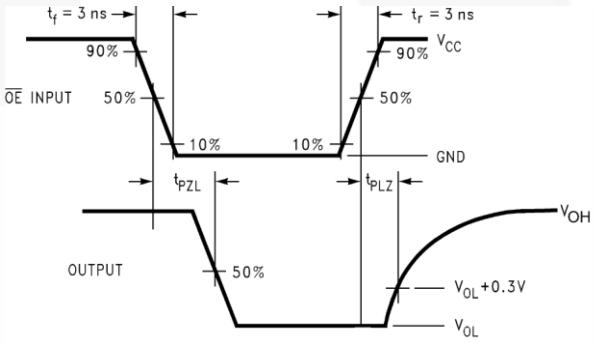
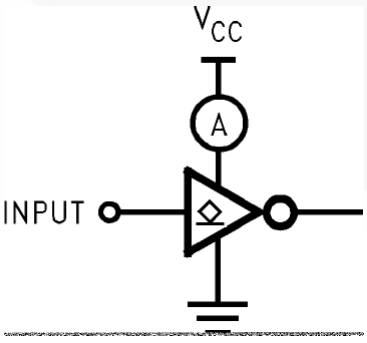


Figure 6. AC Waveforms



Note:

8. Input=AC Waveform; t_r=t_f=1.8ns.
9. PRR=Variable; Duty Cycle=50%.

Figure 7. I_{CCD} Test Circuit

Physical Dimensions

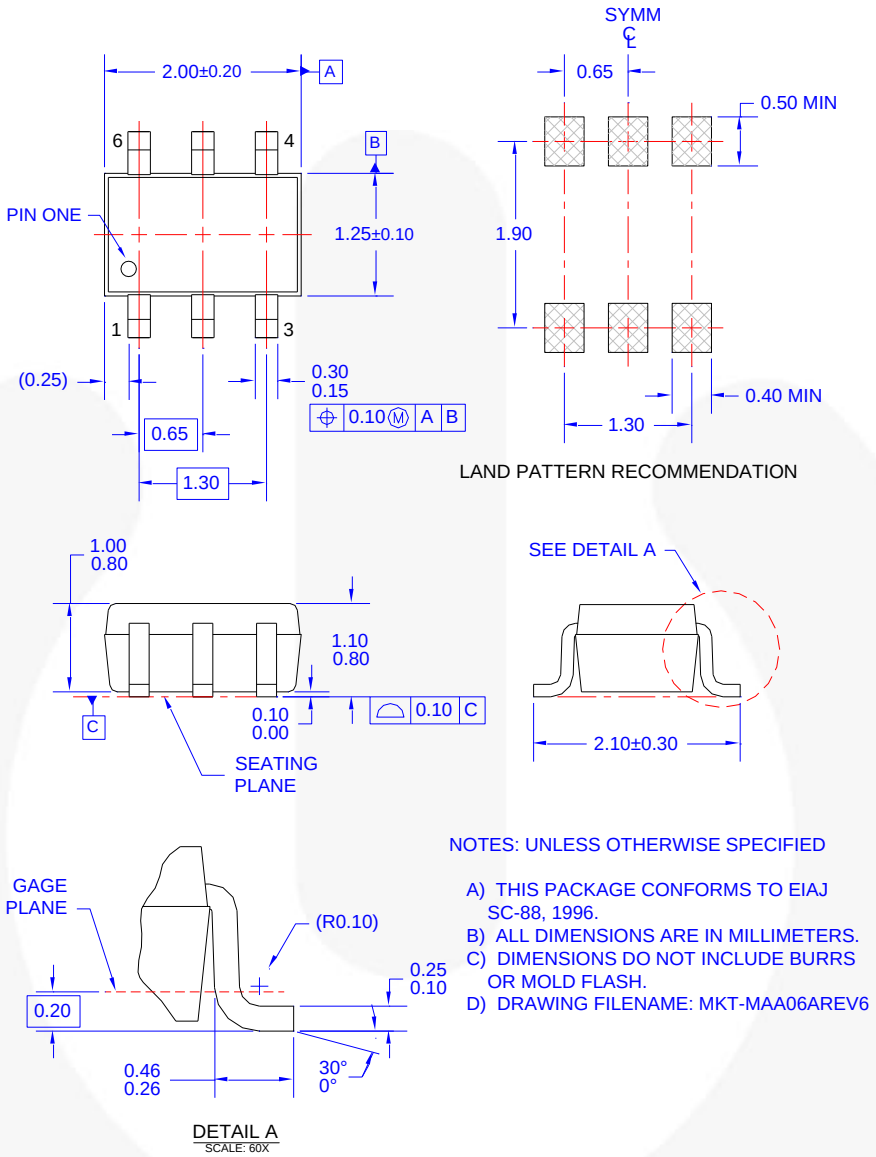


Figure 8. 6-Lead, SC70, EIAJ SC88, 1.25 mm Wide

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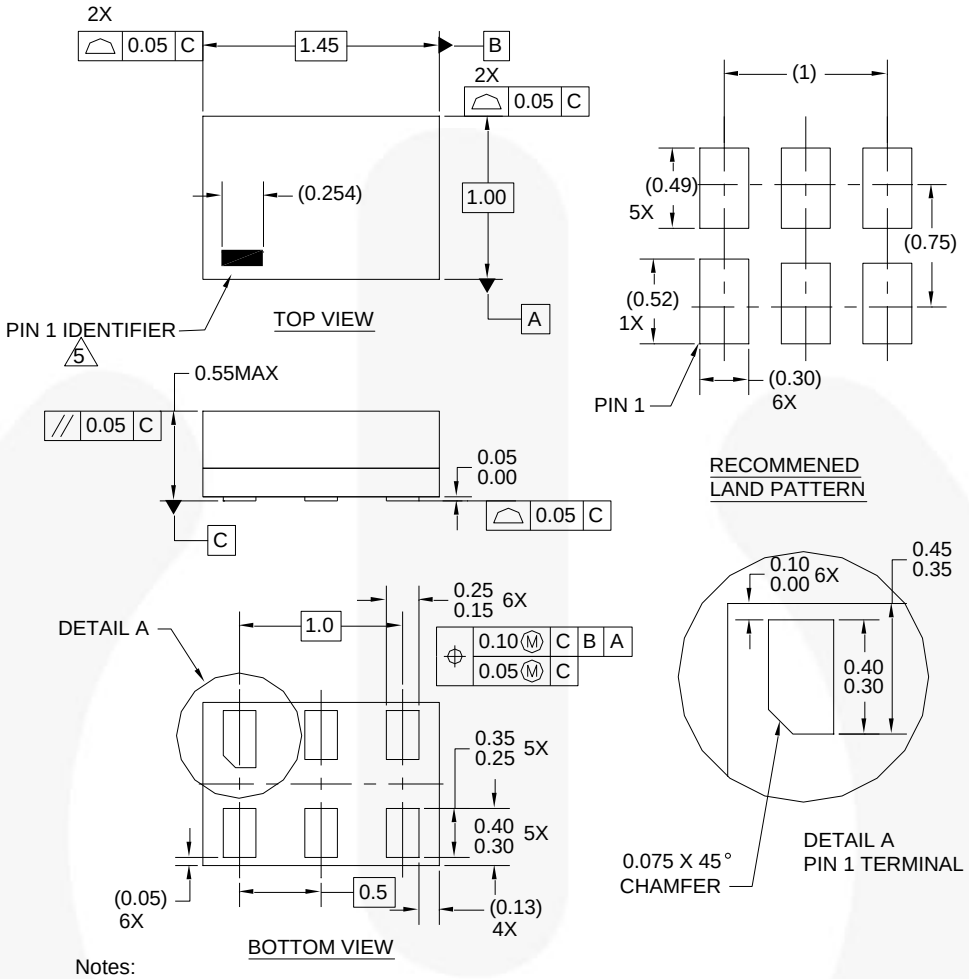
Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
P6X	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

Physical Dimensions



Notes:

1. CONFORMS TO JEDEC STANDARD M0-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-1994
4. FILENAME AND REVISION: MAC06AREV4
5. PIN ONE IDENTIFIER IS 2X LENGTH OF ANY OTHER LINE IN THE MARK CODE LAYOUT.

Figure 9. 6-Lead, MicroPak™, 1.0 mm Wide

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Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
L6X	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

Physical Dimensions

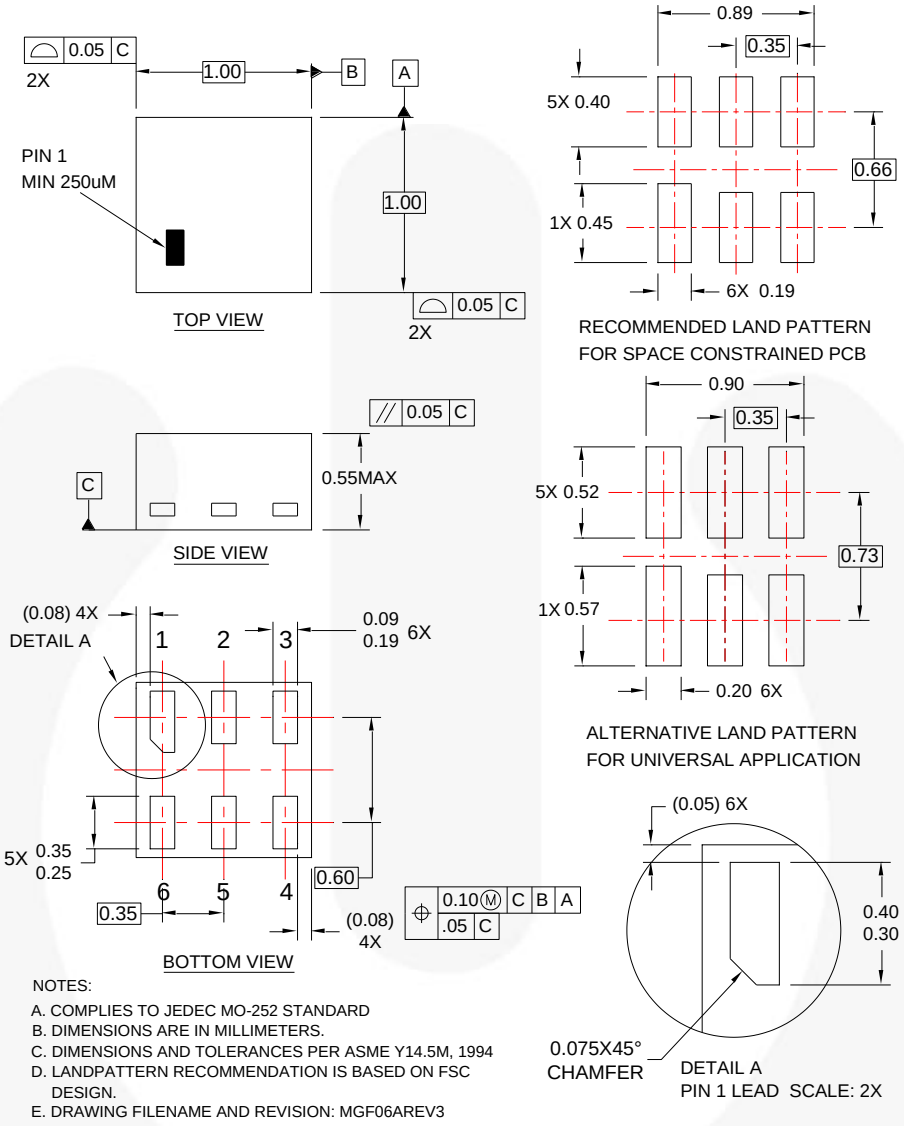

Figure 10. 6-Lead, MicroPak2™, 1x1 mm Body, .35 mm Pitch

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Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
FHX	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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