Product Change Notice (PCN)

Subject: Datasheet Specification Change for Listed Intersil ISL78365ARZ* Products
Publication Date: 10/31/2016
Effective Date: 5/1/2017

Revision Description:
Initial Release

Description of Change:
This notice is to inform you, that as a result of our continuous improvement activities, Intersil has updated the electrical specification table limits. The changes to parameters apply to the following products:

ISL78365ARZ ISL78365ARZ-T ISL78365ARZ-T7A

Reason for Change:
The change aligns the data sheet with the product characteristics. Details regarding the change are contained on the following page. To request an updated data sheet please used the link on the Intersil web site shown below:
http://www.intersil.com/en/products/end-market-specific/automotive-ics/laser-diode-drivers/ISL78365.html?utm_source=intersil&utm_medium=data-short&utm_campaign=isl78365-short-header#

Product Identification:
There have been no changes to the die/silicon or product itself. There will be no change in the external marking of the packaged parts. Product affected by this change is identifiable via Intersil's internal traceability system.

Qualification status: Not applicable
Sample availability: 10/31/2016
Device material declaration: Available upon request

Questions or requests pertaining to this change notice, including additional data or samples, must be sent to Intersil within 30 days of the publication date.

For additional information regarding this notice, please contact your regional change coordinator (below)			
Americas: PCN-US@INTERSIL.COM	Europe: PCN-EU@INTERSIL.COM	Japan: PCN-JP@INTERSIL.COM	Asia Pac: PCN-APAC@INTERSIL.COM

FROM:

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
I_{STBY}	Standby Mode Quiescent Current	Total supply current (V_{DDA}, V_{DD}) when chip is enabled, DACs disabled: Reg 07h = 01h		4.7	8	mA
I_{LOWP}	LOWP Mode Quiescent Current	LOWP Sleep mode Four outputs enabled mode 0; Register 10h, 20h, 30h, 40h = D0h; Register 15h, 25h, 35h, 45h = FFh		15	18	mA
I_{S-ENA}	Supply Currents	Four outputs enabled mode 0; All registers set to default value except: Register 10h, 20h, 30h, 40h = 90h; Register 13h, 23h, 33h, 43h = FFh		80	115	mA
I_{S-ENA}	Supply Currents No Bias	Four outputs enabled mode 0; Color DACs = 0; Everything at default except: Register 15h, 25h, 35h, 45h = 00h		15	17	mA
I_{S-ENA}	Supply Currents Low Bias	Four outputs enabled mode 0; Everything at default except: Color DACs = 01; Register 15h, 25h, 35h, 45h = 11h		45	60	mA
I_{ACTIVE}	Active Mode Quiescent Current	Four outputs enabled mode 0; Everything at default except: Color DACs = 01; Register 15h, 25h, 35h, 45h = FFh Supply Currents High Biased		110	150	mA
I_{RSET}	R_{SET} Bias Current	R_{SET} resistor = 13kΩ		105	110	µA

TO:

DC Electrical Specifications Unless otherwise indicated, the following apply to this table: $V_{DD} = V_{DD\_A1} = V_{DD\_A2} = V_{DD\_DAC} = 3.3V$, $V_{SL} = 1.8V$, $T_A = +25°C$. **Boldface limits apply across the operating temperature range, -40°C to +125°C.**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
V_{DD_A}	Chip Supply Voltage	Applies to V_{DD}, V_{DD_A1}, V_{DD_A2}, V_{DD_DAC}	3.0	3.3	3.6	V
V_{SL}	Voltage Supply to Logics	Reg 0x08[B7:6] = 1Xb	3.0	3.3	3.6	V
		Reg 0x08[B7:6] = 01b	2.2	2.5	2.7	V
		Reg 0x08[B7:6] = 00b	1.7	1.8	1.9	V
I_{VSL}	Parallel Port Logic Supply Current	PLL Enabled, V_{SL}= 3.3V		200	450	µA
I_{DIS}	Disabled Mode Quiescent Current	Chip Enable = 0; Register 10h, 20h, 30h, 40h = 0h; LOWP = 0; L_EN = 1		0.32	1.25	mA
I_{STBY}	Standby Mode Quiescent Current	Total supply current (V_{DD}, V_{DD_A1}, V_{DD_A2}, V_{DD_DAC}) when chip is enabled, DACs disabled: Reg 07h = 01h		4.7	7.6	mA
I_{LOWP}	LOWP Mode Quiescent Current	LOWP Sleep mode Four outputs enabled Mode 0; Register 10h, 20h, 30h, 40h = 90h; Register 15h, 25h, 35h, 45h = FFh All other registers set to default		11	17	mA
I_{S-ENA}	Supply Currents	All I_{OUT} enabled and input Mode 0; Register 10h, 20h, 30h, 40h = 90h; Register 13h, 23h, 33h, 43h = FCh All other registers set to default		67	90	mA
I_{S-ENA}	Supply Currents No Bias	All I_{OUT} enabled and input Mode 0; Color DACs = 0h; Register 10h, 20h, 30h, 40h = 90h; Register 15h, 25h, 35h, 45h = 00h All other registers set to default		11	17	mA
I_{S-ENA}	Supply Currents Low Bias	All I_{OUT} enabled and input Mode 0; Color DACs = 01h; Register 10h, 20h, 30h, 40h = 90h; Register 15h, 25h, 35h, 45h = 11h		37	59	mA
I_{ACTIVE}	Active Mode Quiescent Current	All I_{OUT} enabled and input Mode 0; Color DACs = 01h; Register 10h, 20h, 30h, 40h = 90h; Register 14h, 24h, 34h, 44h bit 2 = 1 Register 15h, 25h, 35h, 45h = FFh All other registers set to default		92	115	mA
I_{RSET}	R_{SET} Bias Current	R_{SET} resistor = 13kΩ		88	90	µA

FROM:

I_{OUTx} Color DACs Specifications $V_{DD} = V_{DD\_A} = 3.3V$, $V_{SL} = 1.8V$, $R_{SET} = 13k\Omega$, $V_{IOUT} = 1V$, Color Scale = 3FFh, Bias = 0Fh, $T_A = +25°C$, unless otherwise indicated. **Boldface limits apply across the operating temperature range, -40°C to +125°C.**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
$IOUT_{MAX}$	Full-Scale Output Current	Input COLOR = 3FFh, V_{IOUTx} = 500mV, (Note 7), I_{OUTx} current offset reg0xX4 Bit 2 = 0	**280**		**560**	mA
		Input COLOR = 3FFh, V_{IOUTx} = 1V (Note 7) I_{OUTx} current offset reg0xX4 Bit 2 = 0	**375**		**700**	mA
		Input COLOR = 3FFh V_{IOUTx} = 500mV, (Note 7) I_{OUTx} current offset reg0xX4 Bit 2 = 1	**350**	500	**630**	mA
		Input COLOR = 3FFh, V_{IOUTx} = 1V (Note 7) I_{OUTx} current offset reg0xX4 Bit 2 = 1	**500**	740	**950**	mA
t_{RISE}	Rise Time	10% to 90% of zero to 200mA at 1V headroom; $R_{LOAD} = 4.0\Omega$		1.5		ns
t_{FALL}	Fall Time	90% to 10% of 200mA to zero at 1V headroom; $R_{LOAD} = 4.0\Omega$		1.5		ns
t_{DELAY}	Time Delay for I_{OUT}	After two output pixels	**10**		**40**	ns
t_{OFF}	Time Delay	From L_EN falling at 50% to I_{OUT} at 50%	**7**	10	**15**	ns
t_{WAKEUP}	Wake-Up Time Delay	From LOWP falling at 50% to I_{OUT} at 50%	**5**	35	**55**	ns
DNL	Differential Nonlinearity	(Note 8)	-1		1	LSB
INL	Integral Nonlinearity	(Note 9)	-4		18	LSB

TO:

I_{OUTx} Color DACs Specifications $V_{DD} = V_{DD\_A} = 3.3V$, $V_{SL} = 1.8V$, $R_{SET} = 13k\Omega$, $V_{IOUT} = 1V$, Color Scale = 3FFh, Bias = 0Fh, $T_A = +25°C$, unless otherwise indicated. **Boldface limits apply across the operating temperature range, -40°C to +125°C.**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
$IOUT_{MAX}$	Full-Scale Output Current	Input COLOR = 3FFh, V_{IOUTx} = 500mV, (Note 7), I_{OUTx} current offset reg0xX4 Bit 2 = 0	**309**	380	**475**	mA
		Input COLOR = 3FFh, V_{IOUTx} = 1V (Note 7) I_{OUTx} current offset reg0xX4 Bit 2 = 0	**335**	428	**566**	mA
		Input COLOR = 3FFh V_{IOUTx} = 500mV, (Note 7) I_{OUTx} current offset reg0xX4 Bit 2 = 1	**378**	460	**555**	mA
		Input COLOR = 3FFh, V_{IOUTx} = 1V (Note 7) I_{OUTx} current offset reg0xX4 Bit 2 = 1	**430**	600	**724**	mA
t_{RISE}	Rise Time	10% to 90% of zero to 200mA at 1V headroom; $R_{LOAD} = 4.0\Omega$		1.5		ns
t_{FALL}	Fall Time	90% to 10% of 200mA to zero at 1V headroom; $R_{LOAD} = 4.0\Omega$		1.5		ns
t_{DELAY}	Time Delay for I_{OUT}	After two output pixels	**10**		**40**	ns
t_{OFF}	Time Delay	From L_EN falling at 50% to I_{OUT} at 50%	**7**	10	**15**	ns
t_{WAKEUP}	Wake-Up Time Delay	From LOWP falling at 50% to I_{OUT} at 50%	**5**	35	**55**	ns
DNL	Differential Nonlinearity	(Note 8)	-2.5		2.5	LSB
INL	Integral Nonlinearity	(Note 9)		10		LSB

FROM:

I_{OUTx} Color Scale DAC DC Specifications $V_{DD} = V_{DD\_A} = 3.3V$, $V_{SL} = 1.8V$, $R_{SET} = 13k\Omega$, $V_{IOUT} = 1V$, Input COLOR = 3FFh, $T_A = +25°C$, unless otherwise indicated.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
SCALER-RANGE	Scaler DAC Range		0.03		75	% I_{OUT} MAX
DNL	Differential Nonlinearity	(Note 8)	-2.0		2.0	LSB
INL	Integral Nonlinearity	(Note 9)	-25		28	LSB

I_{OUTx} Threshold DAC DC Specifications $V_{DD} = V_{DD\_A} = 3.3V$, $V_{SL} = 1.8V$, $R_{SET} = 13k\Omega$, $V_{IOUT} = 1V$, Threshold Scale = 0xFC, $T_A = +25°C$, unless otherwise indicated. **Boldface limits apply across the operating temperature range, -40°C to +125°C.**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
$IOUT_{MAX}$	Full-Scale Output Current	Threshold = FFh, $V_{IOUTx} = 500mV$	**140**		**200**	mA
		Threshold = FFh, $V_{IOUTx} = 1V$	**150**		**290**	mA
DNL	Differential Nonlinearity	(Note 8)	-0.5		0.5	LSB
INL	Integral Nonlinearity	(Note 9)	-2.0		2.0	LSB

TO:

I_{OUTx} Color Scale DAC DC Specifications $V_{DD} = V_{DD\_A1} = V_{DD\_A2} = V_{DD\_DAC} = 3.3V$, $V_{SL} = 1.8V$, $R_{SET} = 13k\Omega$, $V_{IOUT} = 1V$, Input COLOR = 3FFh, $T_A = +25°C$, unless otherwise indicated.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
SCALER-RANGE	Scaler DAC Range		0		100	% I_{OUT} MAX
DNL	Differential Nonlinearity	(Note 8)	-2.0		2.0	LSB
INL	Integral Nonlinearity	(Note 9)	-5		5	LSB

I_{OUTx} Threshold DAC DC Specifications $V_{DD} = V_{DD\_A1} = V_{DD\_A2} = V_{DD\_DAC} = 3.3V$, $V_{SL} = 1.8V$, $R_{SET} = 13k\Omega$, $V_{IOUT} = 1V$, Threshold Scale = 0xFC, $T_A = +25°C$, unless otherwise indicated. **Boldface limits apply across the operating temperature range, -40°C to +125°C.**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
$IOUT_{MAX}$	Full-Scale Output Current	Threshold = FFh, $V_{IOUTx} = 500mV$	**120**	**150**	**178**	mA
		Threshold = FFh, $V_{IOUTx} = 1V$	**125**	**165**	**210**	mA
DNL	Differential Nonlinearity	(Note 8)	-0.6		0.8	LSB
INL	Integral Nonlinearity	(Note 9)	-1.6		1.5	LSB

FROM:

I_{OUTx} Threshold Scale DAC DC Specifications $V_{DD} = V_{DD\_A} = 3.3V$, $V_{SL} = 1.8V$, $R_{SET} = 13k\Omega$, $V_{IOUT} = 1V$, THRESHOLD = FFh, $T_A = +25°C$, unless otherwise indicated.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
THRESHOLD-SCALE-RANGE	Threshold Scale DAC Range		25		100	% I_{OUT} MAX
DNL	Differential Nonlinearity	(Note 8)	-8		8	LSB
INL	Integral Nonlinearity	(Note 9)	-7.50		1.75	LSB

Parallel Data Interface AC Performance Unless otherwise indicated, $V_{DD} = V_{DD\_A} = 3.3V$, $V_{SL} = 1.8V$, $R_{SET} = 13k\Omega$, $T_A = +25°C$.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN (Note 6)	TYP	MAX (Note 6)	UNIT
F_{DCLK}	Data Clock Frequency	Parallel data Interface in mode 0 and 1. Frequency is input mode dependent. PLL disabled.				150	MHz
tPM_{DH}	PLL Mode Data Hold to SYNC	PLL enabled, Maximum Input SYNC rate (see Figure 19 on page 20)	Mode 0	0.3		(1/4Tp)/2	ns
			Mode 1			(1/3Tp)/2	
t_P	Pixel Time	System dependent		20		150	MHz
t_{SYNC}	SYNC Pulse Width		Mode 0		1/3 Tp		ns
			Mode 1		1/4 Tp		
t_{IOUTd}	I_{OUT} Output from SYNC	All modes			2Tp + 6.6		ns

TO:

I_{OUTx} Threshold Scale DAC DC Specifications $V_{DD} = V_{DD\_A1} = V_{DD\_A2} = V_{DD\_DAC} = 3.3V$, $V_{SL} = 1.8V$, $R_{SET} = 13k\Omega$, $V_{IOUT} = 1V$, THRESHOLD = FFh, $T_A = +25°C$, unless otherwise indicated.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
THRESHOLD-SCALE-RANGE	Threshold Scale DAC Range		25		100	% I_{OUT} MAX
DNL	Differential Nonlinearity	(Note 8)	-1		1	LSB
INL	Integral Nonlinearity	(Note 9)		8		LSB

Parallel Data Interface AC Performance Unless otherwise indicated, $V_{DD} = V_{DD\_A1} = V_{DD\_A2} = V_{DD\_DAC} = 3.3V$, $V_{SL} = 1.8V$, $R_{SET} = 13k\Omega$, $T_A = +25°C$.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN (Note 6)	TYP	MAX (Note 6)	UNIT
F_{DCLK}	Data Clock Frequency	Parallel data Interface in Mode 0 and 1. Frequency is input mode dependent. PLL disabled.				200	MHz
Duty	Data Clock "H" Duty Cycle	PLL disabled		45	50	55	%
t_{DCL}	Data Clock Low Time	PLL disabled		2			ns
t_{DCH}	Data Clock High Time	PLL disabled		2			ns
tCM_{RS}, tCM_{FS}	Data Set-Up Time to CLK Edge	PLL disabled, $V_{SL} = 1.8V$, Register 08h: Bits[7:6] = 00b, D[9:0] and RTZ		-0.5			ns
tCM_{RH}, tCM_{FH}	Data Hold Time to CLK Edge	PLL disabled, $V_{SL} = 1.8V$, Register 08h: Bits[7:6] = 00b, D[9:0] and RTZ				1.5	ns
tCM_{SS}	SYNC Set-Up Time to CLK Edge	PLL disabled, $V_{SL} = 1.8V$, Register 08h: Bits[7:6] = 00b		-0.5			ns
tCM_{SH}	SYNC Hold Time to CLK Edge	PLL disabled, $V_{SL} = 1.8V$, Register 08h: Bits[7:6] = 00b				1.5	ns
tPM_{DS}	PLL Mode Data Set-Up to SYNC	PLL enabled, Maximum Input SYNC rate (see Figure 29 on page 22)	Mode 0	0.3		(1/4Tp)/2 - 0.3	ns
			Mode 1	0.3		(1/3Tp)/2 - 0.3	ns
tPM_{DH}	PLL Mode Data Hold to SYNC	PLL enabled, Maximum Input SYNC rate (see Figure 29 on page 22)	Mode 0	(1/4Tp)/2 + 0.3		1/4Tp	ns
			Mode 1	(1/3Tp)/2 + 0.3		1/3Tp	ns
t_P	Pixel Time	System dependent		20		150	MHz
t_{SYNC}	SYNC Pulse Width		Mode 0		1/3 Tp		ns
			Mode 1		1/4 Tp		
t_{IOUTd}	I_{OUT} Output from SYNC	All modes			2Tp + t_{DELAY}		ns
t_{LKPLL}	PLL Lock Time	SYNC at 136MHz, Data mode = 1, Reg 0x09 = 0xFF or 0x0, Reg 0x0A = 0x74, Reg 0x0B = 0x5F.				5	µs

FROM:

ADC DC Specifications Unless otherwise indicated, all of the following tables are: $V_{DD\_A} = V_{DD} = 3.3V$, $V_{SL} = 1.8V$, $R_{SET} = 13k\Omega$, $T_A = +25°C$. **Boldface limits apply across the operating temperature range, -40°C to +125°C.**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
FULL-SCALE	Voltage Generating Full-Scale Code		**1.15**	1.2	**1.40**	V
DNL	Differential Nonlinearity	(Note 8)	-0.65		0.65	LSB
INL	Integral Nonlinearity	(Note 9)	-2.00		2.05	LSB

DPM DAC DC Specifications Unless otherwise indicated, all of the following tables are: $V_{DD\_A} = V_{DD} = 3.3V$, $V_{SL} = 1.8V$, $R_{SET} = 13k\Omega$, $T_A = +25°C$. **Boldface limits apply across the operating temperature range, -40°C to +125°C.**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
I_{DPMX}	DPM Sink Current	DPMX enable bit = 1; DPMX scale = 00		12.5		µA
		DPMX enable bit = 1; DPMX scale = 01		25		
		DPMX enable bit = 1; DPMX scale = 10		50		
		DPMX enable bit = 1; DPMX scale = 11		100		

TO:

ADC DC Specifications Unless otherwise indicated, all of the following tables are: $V_{DD} = V_{DD\_A1} = V_{DD\_A2} = V_{DD\_DAC} = 3.3V$, $V_{SL} = 1.8V$, $R_{SET} = 13k\Omega$, $T_A = +25°C$. **Boldface limits apply across the operating temperature range, -40°C to +125°C.**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
FULL-SCALE	Voltage Generating Full-Scale Code		**1.15**	1.20	**1.40**	V
DNL	Differential Nonlinearity	(Note 8)	-0.5		0.5	LSB
INL	Integral Nonlinearity	(Note 9)	-2.00		2.05	LSB

DPM DAC DC Specifications Unless otherwise indicated, all of the following tables are: $V_{DD} = V_{DD\_A1} = V_{DD\_A2} = V_{DD\_DAC} = 3.3V$, $V_{SL} = 1.8V$, $R_{SET} = 13k\Omega$, $T_A = +25°C$. **Boldface limits apply across the operating temperature range, -40°C to +125°C.**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
I_{DPMX}	DPM Sink Current	DPMX enable bit = 1; DPMX scale = 00	9.2	12.5	15.2	µA
		DPMX enable bit = 1; DPMX scale = 01	20	25	30	µA
		DPMX enable bit = 1; DPMX scale = 10	40	50	60	µA
		DPMX enable bit = 1; DPMX scale = 11	80	100	120	µA