Micron Parallel NOR Flash Embedded Memory (P33-65nm)

RC28F256P33TFE, RC28F256P33BFE, RC28F256P33BFF, PC28F256P33TFE, PC28F256P33BFE, PC28F256P33BFF, PC28F256P33BFR, RC48F4400P0TB0EJ, PC48F4400P0TB0EE, PC48F4400P0TB0EH, JS28F256P33TFE, JS28F256P33BFE

Features

- High performance
  - 95ns initial access for Easy BGA
  - 105ns initial access for TSOP
  - 25ns 16-word asychronous page read mode
  - 52 MHz (Easy BGA) with zero WAIT states and 17ns clock-to-data output synchronous burst read mode
  - 4-, 8-, 16-, and continuous word options for burst mode
  - Buffered enhanced factory programming (BEFP) at 2 MB/s (TYP) using a 512-word buffer
  - 3.0V buffered programming at 1.14 MB/s (TYP) using a 512-word buffer
- Architecture
  - MLC: highest density at lowest cost
  - Asymmetrically blocked architecture
  - Four 32KB parameter blocks: top or bottom configuration
  - 128KB main blocks
  - Blank check to verify an erased block
- Voltage and power
  - V_{CC} (core) voltage: 2.3V to 3.6V
  - V_{CCQ} (I/O) voltage: 2.3V to 3.6V
  - Standy current: 65µA (TYP) for 256Mb
  - 52 MHz continuous synchronous read current: 21mA (TYP), 24mA (MAX)
- Security
  - One-time programmable register: 64 OTP bits, programmed with unique information from Micron; 2112 OTP bits available for customer programming
  - Absolute write protection: $V_{PP} = V_{SS}$
  - Power-transition erase/program lockout
  - Individual zero-latency block locking
  - Individual block lock-down
  - Password access
- Software
  - 25µs (TYP) program suspend
  - 25µs (TYP) erase suspend
  - Flash Data Integrator optimized
  - Basic command set and extended function Interface (EFI) command set compatible
  - Common flash interface
- Density and Packaging
  - 56-lead TSOP package (256Mb only)
  - 64-ball Easy BGA package (256Mb, 512Mb)
  - QUAD+ and SCSP packages (256Mb, 512Mb)
  - 16-bit wide data bus
- Quality and reliabilty
  - JESD47 compliant
  - Operating temperature: –40°C to +85°C
  - Minimum 100,000 ERASE cycles per block
  - 65nm process technology

Discrete and MCP Part Numbering Information

Devices are shipped from the factory with memory content bits erased to 1. For available options, such as packages or for further information, contact your Micron sales representative. Part numbers can be verified at www.micron.com. Feature and specification comparison by device type is available at www.micron.com/products. Contact the factory for devices not found.

Note: Not all part numbers listed here are available for ordering.

Table 1: Discrete Part Number Information

Part Number Category	Category Details
Package	JS = 56-lead TSOP, lead free
	PC = 64-ball Easy BGA, lead-free
	RC = 64-ball Easy BGA, leaded
Product Line	28F = Micron Flash memory
Density	256 = 256Mb
Product Family	P33 (V_{CC} = 2.3 to 3.6V; V_{CCQ} = 2.3 to 3.6V)
Parameter Location	B/T = Bottom/Top parameter
Lithography	F = 65nm
Features	*

Note: 1. The last digit is assigned randomly to cover packaging media, features, or other specific configuration information. Sample part number: JS28F256P33BF*

Table 2: MCP Part Number Information

Part Number Category	Category Details
Package	RC = 64-ball Easy BGA, leaded
	PC = 64-ball Easy BGA, lead-free
Product Line	48F = Micron Flash memory only
Density	0 = No die
	4 = 256Mb
Product Family	P = Micron Flash memory (P33)
	0 = No die
IO Voltage and Chip Configuration	X = Individual Chip Enables
	T = Virtual Chip Enables
	V_{CC} = 2.3 to 3.6V; V_{CCQ} = 2.3 to 3.6V
Parameter Location	B/T = Bottom/Top parameter
Ballout	0 = Discrete
Lithography	E = 65nm
Features	*

Note: 1. The last digit is assigned randomly to cover packaging media, features, or other specific configuration information. Sample part number: RC48F4400P0TB0E*

Table 3: Standard Part Numbers

Density	Configuration	Medium	JS	PC	RC
256Mb	Bottom boot	Tray	JS28F256P33BFE	PC28F256P33BFE	RC28F256P33BFE
		Tape and reel	–	PC28F256P33BFF	RC28F256P33BFF
	Top boot	Tray	JS28F256P33TFE	PC28F256P33TFE	RC28F256P33TFE
		Tape and reel	–	–	–
512Mb (256Mb/256Mb)	Top/bottom boot	Tray	–	PC48F4400P0TB0EE	RC48F4400P0TB0EJ
	–	Tape and reel	–	–	–

Table 4: OTP Feature Part Numbers

Density	Configuration	Medium	PC
256Mb	Bottom boot	Tray	PC28F256P33BFR
		Tape and reel	–
	Top boot	Tray	–
		Tape and reel	–
512Mb (256Mb/256Mb)	Top/bottom boot	Tray	PC48F4400P0TB0EH
	–	Tape and reel	–

Note: 1. This data sheet covers only standard parts. For OTP parts, contact your local Micron representative.

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General Description

The Micron Parallel NOR Flash memory is the latest generation of Flash memory devices. Benefits include more density in less space, high-speed interface device, and support for code and data storage. Features include high-performance synchronous-burst read mode, fast asynchronous access times, low power, flexible security options, and three industry-standard package choices. The product family is manufactured using Micron 65nm process technology.

The NOR Flash device provides high performance at low voltage on a 16-bit data bus. Individually erasable memory blocks are sized for optimum code and data storage.

Upon initial power up or return from reset, the device defaults to asynchronous page-mode read. Configuring the read configuration register enables synchronous burst-mode reads. In synchronous burst mode, output data is synchronized with a user-supplied clock signal. A WAIT signal provides easy CPU-to-flash memory synchronization.

In addition to the enhanced architecture and interface, the device incorporates technology that enables fast factory PROGRAM and ERASE operations. Designed for low-voltage systems, the devIce supports READ operations with V_{CC} at the low voltages, and ERASE and PROGRAM operations with V_{PP} at the low voltages or V_{PPH}. Buffered enhanced factory programming (BEFP) provides the fastest Flash array programming performance with V_{PP} at V_{PPH}, which increases factory throughput. With V_{PP} at low voltages, V_{CC} and V_{PP} can be tied together for a simple, ultra low-power design. In addition to voltage flexibility, a dedicated V_{PP} connection provides complete data protection when $V_{PP} \leq V_{PPLK}$.

A command user interface is the interface between the system processor and all internal operations of the device. The device automatically executes the algorithms and timings necessary for block erase and program. A status register indicates ERASE or PROGRAM completion and any errors that may have occurred.

An industry-standard command sequence invokes program and erase automation. Each ERASE operation erases one block. The erase suspend feature enables system software to pause an ERASE cycle to read or program data in another block. Program suspend enables system software to pause programming to read other locations. Data is programmed in word increments (16 bits).

The protection register enables unique device identification that can be used to increase system security. The individual block lock feature provides zero-latency block locking and unlocking. The device includes enhanced protection via password access; this new feature supports write and/or read access protection of user-defined blocks. In addition, the device also provides the full-device OTP security feature.

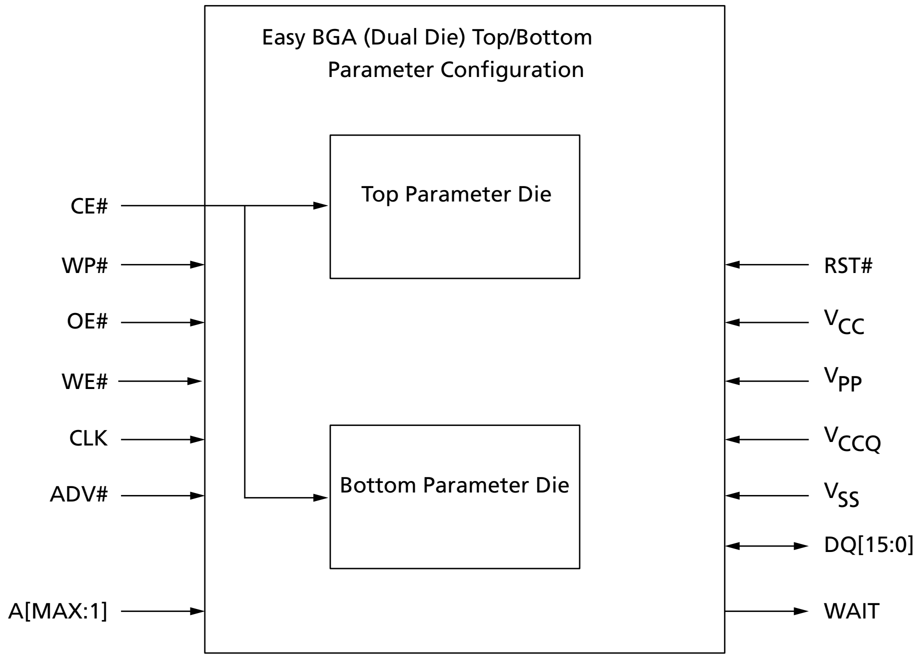
Virtual Chip Enable Description

The 512Mb device employs a virtual chip enable feature, which combines two 256Mb die with a common chip enable, CE# for Easy BGA packages. The maximum address bit is then used to select between the die pair with CE# asserted. When CE# is asserted and the maximum address bit is LOW, the lower parameter die is selected; when CE# is asserted and the maximum address bit is HIGH, the upper parameter die is selected.

Table 5: Virtual Chip Enable Truth Table for 512Mb (Easy BGA Packages)

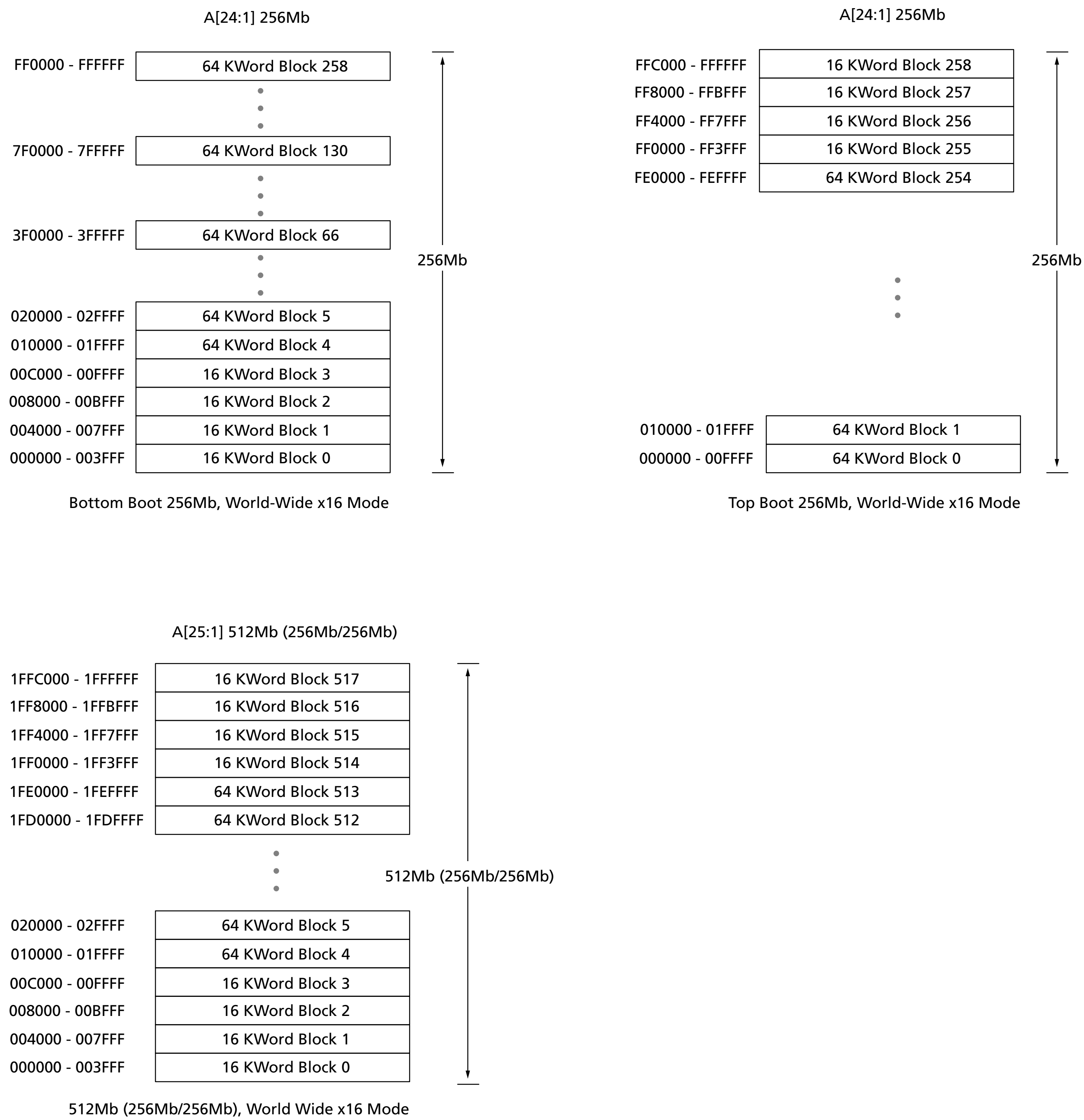
Die Selected	CE#	A25
Lower Param Die	L	L
Upper Param Die	L	H

Figure 1: 512Mb Easy BGA Block Diagram



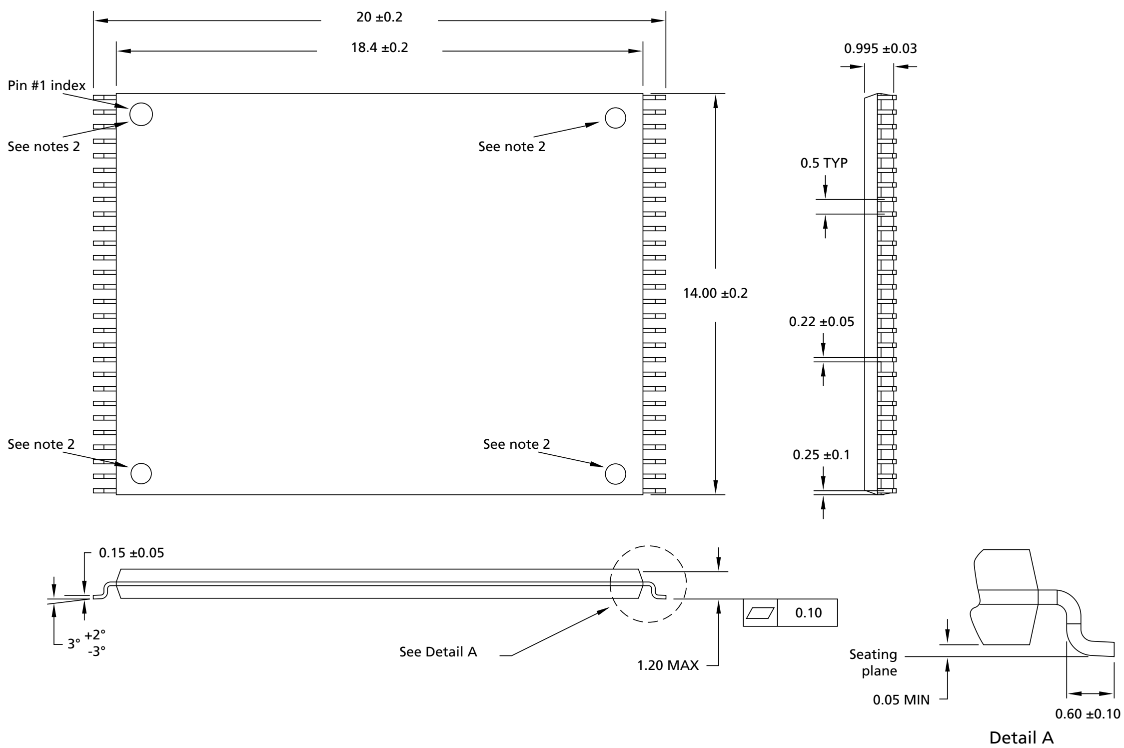
Memory Map

Figure 2: Memory Map – 256Mb and 512Mb



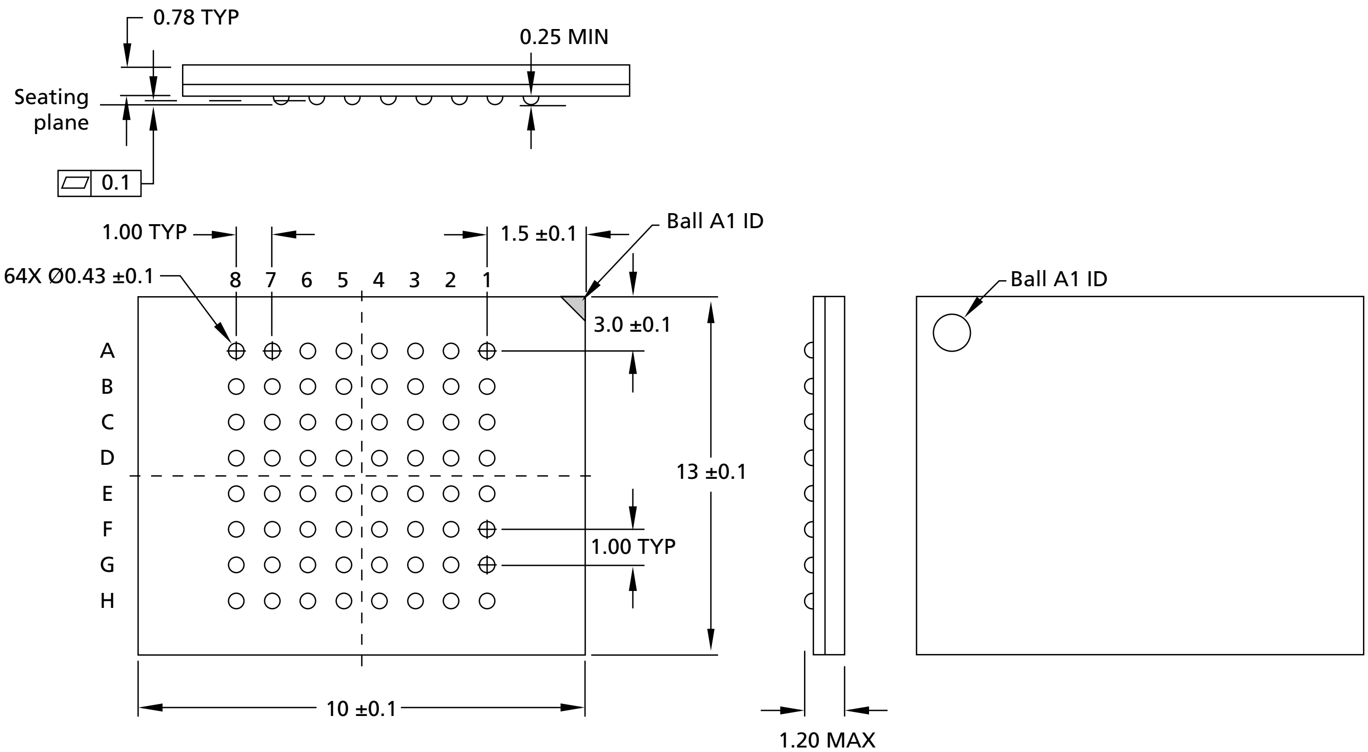
Package Dimensions

Figure 3: 56-Pin TSOP – 14mm x 20mm



Notes:
1. All dimensions are in millimeters. Drawing not to scale.
2. One dimple on package denotes pin 1; if two dimples, then the larger dimple denotes pin 1. Pin 1 will always be in the upper left corner of the package, in reference to the product mark.
3. For the lead width value of 0.22 ±0.05, there is also a legacy value of 0.15 ±0.05.

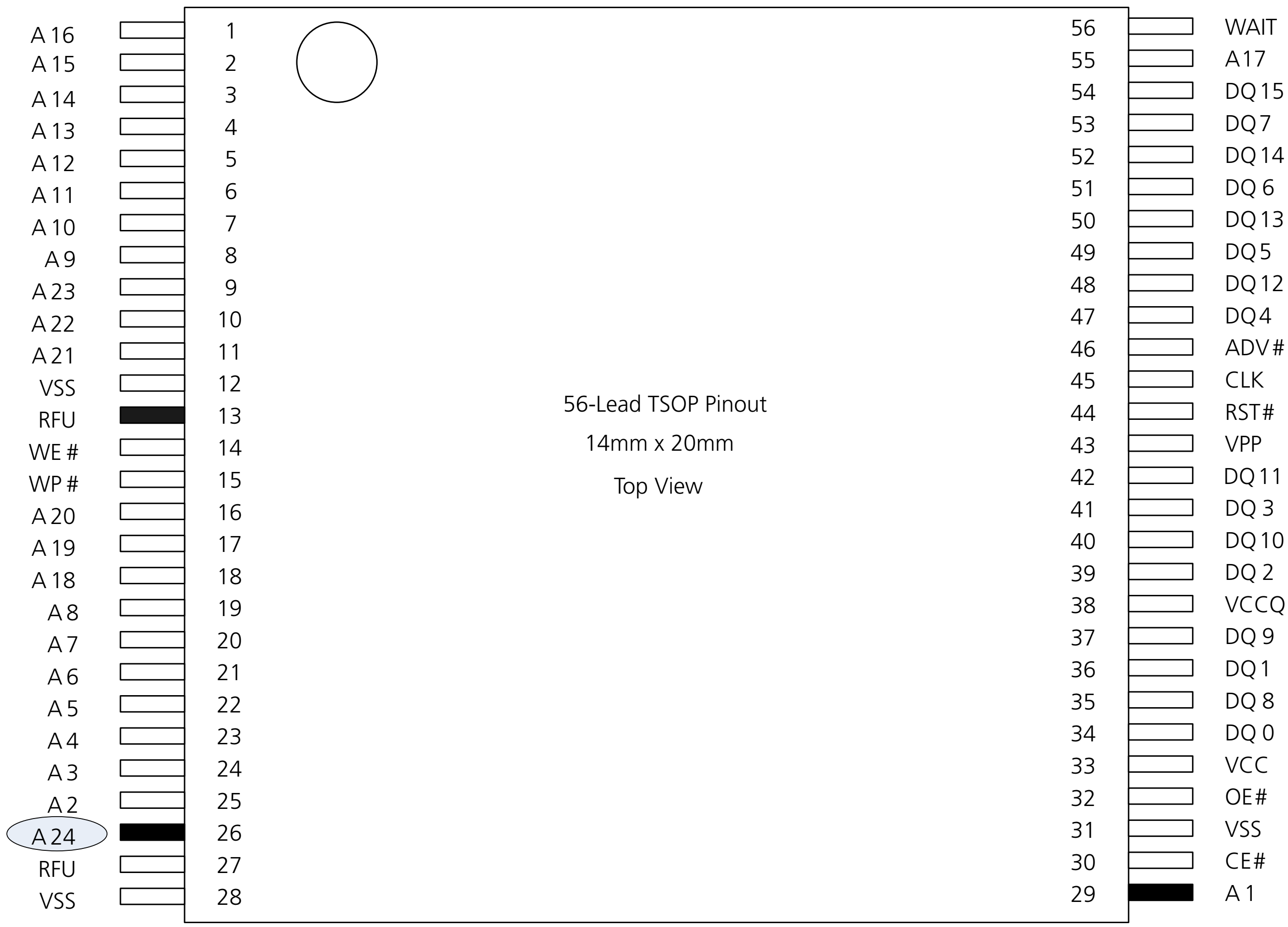
Figure 4: 64-Ball Easy BGA – 10mm x 13mm x 1.2mm



Note: 1. All dimensions are in millimeters. Drawing not to scale.

Pinouts and Ballouts

Figure 5: 56-Lead TSOP Pinout – 256Mb



Notes:
1. A1 is the least significant address bit.
2. A24 is valid for 256Mb densities; otherwise, it is a no connect (NC).
3. No internal connection on Pin 13; it may be driven or floated. For legacy designs, it is a V_{CC} pin and can be tied to V_{CC}.
4. One dimple on package denotes Pin 1 which will always be in the upper left corner of the package, in reference to the product mark.

Figure 6: 64-Ball Easy BGA Ballout – 256Mb, 512Mb

	1	2	3	4	5	6	7	8
A	A1	A6	A8	V_{PP}	A13	V_{CC}	A18	A22
B	A2	V_{SS}	A9	CE #	A14	A25	A19	RFU
C	A3	A7	A10	A12	A15	WP#	A20	A21
D	A4	A5	A11	RST #	V_{CCQ}	V_{CCQ}	A16	A17
E	DQ8	DQ1	DQ9	DQ3	DQ4	CLK	DQ15	RFU
F	RFU	DQ0	DQ10	DQ11	DQ12	ADV#	WAIT	OE#
G	A23	RFU	DQ2	V_{CCQ}	DQ5	DQ6	DQ14	WE#
H	RFU	V_{SS}	V_{CC}	V_{SS}	DQ13	VSS	DQ7	A24

Notes:
1. A1 is the least significant address bit.
2. A24 is valid for 256Mb densities and above; otherwise, it is a no connect (NC).
3. A25 is valid for 512Mb densities; otherwise, it is a no connect.
4. One dimple on package denotes A1 pin, which will always be in the upper-left corner of the package, in reference to the product mark.

Signal Descriptions

Table 6: TSOP and Easy BGA Signal Descriptions

Symbol	Type	Name and Function
A[MAX:1]	Input	**Address inputs:** Device address inputs. **Note:** Unused active address pins should not be left floating; tie them to V_{CCQ} or V_{SS} according to specific design requirements.
ADV#	Input	**Address valid:** Active LOW input. During synchronous READ operations, addresses are latched on the rising edge of ADV#, or on the next valid CLK edge with ADV# LOW, whichever occurs first. In asynchronous mode, the address is latched when ADV# goes HIGH or continuously flows through if ADV# is held LOW. **Note:** Designs not using ADV# must tie it to V_{SS} to allow addresses to flow through.
CE#	Input	**Chip enable:** Active LOW input. CE# LOW selects the associated die. When asserted, internal control logic, input buffers, decoders, and sense amplifiers are active. When de-asserted, the associated die is deselected, power is reduced to standby levels, data and wait outputs are placed in High-Z. **Note:** CE# must be driven HIGH when device is not in use.
CLK	Input	**Clock:** Synchronizes the device with the system bus frequency in synchronous-read mode. During synchronous READs, addresses are latched on the rising edge of ADV#, or on the next valid CLK edge with ADV# LOW, whichever occurs first. **Note:** Designs not using CLK for synchronous read mode must tie it to V_{CCQ} or V_{SS}.
OE#	Input	**Output enable:** Active LOW input. OE# LOW enables the device's output data buffers during READ cycles. OE# HIGH places the data outputs and WAIT in High-Z.
RST#	Input	**Reset:** Active LOW input. RST# resets internal automation and inhibits WRITE operations. This provides data protection during power transitions. RST# HIGH enables normal operation. Exit from reset places the device in asynchronous read array mode.
WP#	Input	**Write protect:** Active LOW input. WP# LOW enables the lock-down mechanism. Blocks in lock-down cannot be unlocked with the Unlock command. WP# HIGH overrides the lock-down function enabling blocks to be erased or programmed using software commands. **Note:** Designs not using WP# for protection could tie it to V_{CCQ} or V_{SS} without additional capacitor.
WE#	Input	**Write enable:** Active LOW input. WE# controls writes to the device. Address and data are latched on the rising edge of WE# or CE#, whichever occurs first.
V_{PP}	Power/Input	**Erase and program power:** A valid voltage on this pin allows erasing or programming. Memory contents cannot be altered when $V_{PP} \le V_{PPLK}$. Block erase and program at invalid V_{PP} voltages should not be attempted. Set $V_{PP} = V_{PPL}$ for in-system PROGRAM and ERASE operations. To accommodate resistor or diode drops from the system supply, the V_{IH} level of V_{PP} can be as low as $V_{PPL,min}$. V_{PP} must remain above $V_{PPL,min}$ to perform in-system modification. V_{PP} may be 0V during READ operations. V_{PP} can be connected to 9V for a cumulative total not to exceed 80 hours. Extended use of this pin at 9V may reduce block cycling capability.
DQ[15:0]	Input/Output	**Data input/output:** Inputs data and commands during WRITE cycles; outputs data during memory, status register, protection register, and read configuration register reads. Data balls float when the CE# or OE# are de-asserted. Data is internally latched during writes.

Table 6: TSOP and Easy BGA Signal Descriptions (Continued)

Symbol	Type	Name and Function
WAIT	Output	**Wait:** Indicates data valid in synchronous array or non-array burst reads. Read configuration register bit 10 (RCR.10, WT) determines its polarity when asserted. This signal's active output is V_{OL} or V_{OH} when CE# and OE# are V_{IL}. WAIT is High-Z if CE# or OE# is V_{IH}. • In synchronous array or non-array read modes, this signal indicates invalid data when asserted and valid data when de-asserted. • In asynchronous page mode, and all write modes, this signal is de-asserted.
V_{CC}	Power	**Device core power supply:** Core (logic) source voltage. Writes to the array are inhibited when $V_{CC} \leq V_{LKO}$. Operations at invalid V_{CC} voltages should not be attempted.
V_{CCQ}	Power	**Output power supply:** Output-driver source voltage.
V_{SS}	Power	**Ground:** Connect to system ground. Do not float any V_{SS} connection.
RFU	—	**Reserved for future use:** Reserved by Micron for future device functionality and enhancement. These should be treated in the same way as a DU signal.
DU	—	**Do not use:** Do not connect to any other signal, or power supply; must be left floating.
NC	—	**No connect:** No internal connection; can be driven or floated.

Bus Operations

CE# LOW and RST# HIGH enable READ operations. The device internally decodes upper address inputs to determine the accessed block. ADV# LOW opens the internal address latches. OE# LOW activates the outputs and gates selected data onto the I/O bus.

Bus cycles to/from the device conform to standard microprocessor bus operations. Bus operations and the logic levels that must be applied to the device control signal inputs are shown here.

Table 7: Bus Operations

Bus Operation		RST#	CLK	ADV#	CE#	OE#	WE#	WAIT	DQ[15:0]	Notes
READ	Asynchronous	H	X	L	L	L	H	De-asserted	Output	-
	Synchronous	H	Running	L	L	L	H	Driven	Output	-
WRITE		H	X	L	L	H	L	High-Z	Input	1
OUTPUT DISABLE		H	X	X	L	H	H	High-Z	High-Z	2
STANDBY		H	X	X	H	X	X	High-Z	High-Z	2
RESET		L	X	X	X	X	X	High-Z	High-Z	2, 3

Notes:
1. Refer to the Device Command Bus Cycles for valid DQ[15:0] during a WRITE operation.
2. X = "Don’t Care" (H or L).
3. RST# must be at V_{SS} ± 0.2V to meet the maximum specified power-down current.

Read

To perform a READ operation, RST# and WE# must be de-asserted while CE# and OE# are asserted. CE# is the device-select control. When asserted, it enables the device. OE# is the data-output control. When asserted, the addressed flash memory data is driven onto the I/O bus.

Write

To perform a WRITE operation, both CE# and WE# are asserted while RST# and OE# are de-asserted. During a WRITE operation, address and data are latched on the rising edge of WE# or CE#, whichever occurs first. The Command Bus Cycles table shows the bus cycle sequence for each of the supported device commands, while the Command Codes and Definitions table describes each command.

Note: WRITE operations with invalid V_{CC} and/or V_{PP} voltages can produce spurious results and should not be attempted.

Output Disable

When OE# is de-asserted, device outputs DQ[15:0] are disabled and placed in High-Z state, WAIT is also placed in High-Z.

Standby

When CE# is de-asserted the device is deselected and placed in standby, substantially reducing power consumption. In standby, the data outputs are placed in High-Z, independent of the level placed on OE#. Standby current (I_{CCS}) is the average current measured over any 5ms time interval, 5µs after CE# is de-asserted. During standby, average current is measured over the same time interval 5µs after CE# is de-asserted.

When the device is deselected (while CE# is de-asserted) during a PROGRAM or ERASE operation, it continues to consume active power until the PROGRAM or ERASE operation is completed.

Reset

As with any automated device, it is important to assert RST# when the system is reset. When the system comes out of reset, the system processor attempts to read from the device if it is the system boot device. If a CPU reset occurs with no device reset, improper CPU initialization may occur because the device may be providing status information rather than array data. Micron devices enable proper CPU initialization following a system reset through the use of the RST# input. RST# should be controlled by the same low-true reset signal that resets the system CPU.

After initial power-up or reset, the device defaults to asynchronous read array mode, and the status register is set to 0x80. Asserting RST# de-energizes all internal circuits, and places the output drivers in High-Z. When RST# is asserted, the device shuts down the operation in progress, a process which takes a minimum amount of time to complete. When RST# has been de-asserted, the device is reset to asynchronous read array state.

When device returns from a reset (RST# de-asserted), a minimum wait is required before the initial read access outputs valid data. Also, a minimum delay is required after a reset before a write cycle can be initiated. After this wake-up interval passes, normal operation is restored.

Note: If RST# is asserted during a PROGRAM or ERASE operation, the operation is terminated and the memory contents at the aborted location (for a program) or block (for an erase) are no longer valid, because the data may have been only partially written or erased.

Device Command Codes

The system CPU provides control of all in-system READ, WRITE, and ERASE operations of the device via the system bus. The device manages all block-erase and word-program algorithms.

Device commands are written to the CUI to control all device operations. The CUI does not occupy an addressable memory location; it is the mechanism through which the device is controlled.

Note: For a dual device, all setup commands should be re-issued to the device when a different die is selected.

Table 8: Command Codes and Definitions

Mode	Device Mode	Code	Description
Read	Read array	0xFF	Places the device in read array mode. Array data is output on DQ[15:0].
	Read status register	0x70	Places the device in read status register mode. The device enters this mode after a PROGRAM or ERASE command is issued. Status register data is output on DQ[7:0].
	Read device ID or read configuration register	0x90	Places device in read device identifier mode. Subsequent reads output manufacturer/device codes, configuration register data, block lock status, or protection register data on DQ[15:0].
	Read CFI	0x98	Places the device in read CFI mode. Subsequent reads output CFI information on DQ[7:0].
	Clear status register	0x50	The device sets status register error bits. The clear status register command is used to clear the SR error bits.
Write	Word program setup	0x40	First cycle of a 2-cycle programming command; prepares the CUI for a WRITE operation. On the next write cycle, the address and data are latched and the device executes the programming algorithm at the addressed location. During PROGRAM operations, the device responds only to READ STATUS REGISTER and PROGRAM SUSPEND commands. CE# or OE# must be toggled to update the status register in asynchronous read. CE# or ADV# must be toggled to update the status register data for synchronous non-array reads. The READ ARRAY command must be issued to read array data after programming has finished.
	Buffered program	0xE8	This command loads a variable number of words up to the buffer size of 512 words onto the program buffer.
	Buffered program confirm	0xD0	The CONFIRM command is issued after the data streaming for writing into the buffer is completed. The device then performs the buffered program algorithm, writing the data from the buffer to the memory array.
	BEFP setup	0x80	First cycle of a two-cycle command; initiates buffered enhanced factory program mode (BEFP). The CUI then waits for the BEFP CONFIRM command, 0xD0, that initiates the BEFP algorithm. All other commands are ignored when BEFP mode begins.
	BEFP confirm	0xD0	If the previous command was BEFP SETUP (0x80), the CUI latches the address and data, and prepares the device for BEFP mode.

Table 8: Command Codes and Definitions (Continued)

Mode	Device Mode	Code	Description
Erase	Block erase setup	0x20	First cycle of a two-cycle command; prepares the CUI for a BLOCK ERASE operation. The device performs the erase algorithm on the block addressed by the ERASE CONFIRM command. If the next command *is not* the ERASE CONFIRM (0xD0) command, the CUI sets status register bits SR4 and SR5, and places the device in read status register mode.
	Block erase confirm	0xD0	If the first command was BLOCK ERASE SETUP (0x20), the CUI latches the address and data, and the device erases the addressed block. During BLOCK ERASE operations, the device responds only to READ STATUS REGISTER and ERASE SUSPEND commands. CE# or OE# must be toggled to update the status register in asynchronous read. CE# or ADV# must be toggled to update the status register data for synchronous non-array reads.
Suspend	Program or erase suspend	0xB0	This command issued to any device address initiates a suspend of the currently-executing program or BLOCK ERASE operation. The status register indicates successful suspend operation by setting either SR2 (program suspended) or SR6 (erase suspended), along with SR7 (ready). The device remains in the suspend mode regardless of control signal states (except for RST# asserted).
	Suspend resume	0xD0	This command issued to any device address resumes the suspended PROGRAM or BLOCK ERASE operation.
Protection	Block lock setup	0x60	First cycle of a two-cycle command; prepares the CUI for block lock configuration changes. If the next command is not BLOCK LOCK (0x01), BLOCK UNLOCK (0xD0), or BLOCK LOCK DOWN (0x2F), the CUI sets status register bits SR5 and SR4, indicating a command sequence error.
	Block lock	0x01	If the previous command was BLOCK LOCK SETUP (0x60), the addressed block is locked.
	Block unlock	0xD0	If the previous command was BLOCK LOCK SETUP (0x60), the addressed block is unlocked. If the addressed block is in a lock down state, the operation has no effect.
	Block lock down	0x2F	If the previous command was BLOCK LOCK SETUP (0x60), the addressed block is locked down.
	OTP register or lock register program setup	0xC0	First cycle of a two-cycle command; prepares the device for a OTP REGISTER or LOCK REGISTER PROGRAM operation. The second cycle latches the register address and data, and starts the programming algorithm to program data the OTP array.
Configuration	Read configuration register setup	0x60	First cycle of a two-cycle command; prepares the CUI for device read configuration. If the SET READ CONFIGURATION REGISTER command (0x03) is not the next command, the CUI sets status register bits SR4 and SR5, indicating a command sequence error.
	Read configuration register	0x03	If the previous command was READ CONFIGURATION REGISTER SETUP (0x60), the CUI latches the address and writes A[16:1] to the read configuration register for Easy BGA and TSOP, A[15:0] for QUAD+. Following a CONFIGURE READ CONFIGURATION REGISTER command, subsequent READ operations access array data.

Table 8: Command Codes and Definitions (Continued)

Mode	Device Mode	Code	Description
Blank Check	Block blank check	0xBC	First cycle of a two-cycle command; initiates the BLANK CHECK operation on a main block.
	Block blank check confirm	0xD0	Second cycle of blank check command sequence; it latches the block address and executes blank check on the main array block.
EFI	Extended function interface	0xEB	First cycle of a multiple-cycle command; initiate operation using extended function interface. The second cycle is a Sub-Op-Code, the data written on third cycle is one less than the word count; the allowable value on this cycle are 0–511. The subsequent cycles load data words into the program buffer at a specified address until word count is achieved.

Device Command Bus Cycles

Device operations are initiated by writing specific device commands to the command user interface (CUI). Several commands are used to modify array data including WORD PROGRAM and BLOCK ERASE commands. Writing either command to the CUI initiates a sequence of internally timed functions that culminate in the completion of the requested task. However, the operation can be aborted by either asserting RST# or by issuing an appropriate suspend command.

Table 9: Command Bus Cycles

Mode	Command	Bus Cycles	First Bus Cycle			Second Bus Cycle		
			Op	Addr[1]	Data[2]	Op	Addr[1]	Data[2]
Read	READ ARRAY	1	WRITE	DnA	0xFF	–	–	–
	READ DEVICE IDENTIFIER	≥2	WRITE	DnA	0x90	READ	DBA + IA	ID
	READ CFI	≥2	WRITE	DnA	0x98	READ	DBA + CFI-A	CFI-D
	READ STATUS REGISTER	2	WRITE	DnA	0x70	READ	DnA	SRD
	CLEAR STATUS REGISTER	1	WRITE	DnA	0x50	–	–	–
Program	WORD PROGRAM	2	WRITE	WA	0x40	WRITE	WA	WD
	BUFFERED PROGRAM[3]	>2	WRITE	WA	0xE8	WRITE	WA	N - 1
	BUFFERED ENHANCED FACTORY PROGRAM (BEFP)[4]	>2	WRITE	WA	0x80	WRITE	WA	0xD0
Erase	BLOCK ERASE	2	WRITE	BA	0x20	WRITE	BA	0xD0
Suspend	PROGRAM/ERASE SUSPEND	1	WRITE	DnA	0xB0	–	–	–
	PROGRAM/ERASE RESUME	1	WRITE	DnA	0xD0	–	–	–
Protection	BLOCK LOCK	2	WRITE	BA	0x60	WRITE	BA	0x01
	BLOCK UNLOCK	2	WRITE	BA	0x60	WRITE	BA	0xD0
	BLOCK LOCK DOWN	2	WRITE	BA	0x60	WRITE	BA	0x2F
	PROGRAM OTP REGISTER	2	WRITE	PRA	0xC0	WRITE	OTP-RA	OTP-D
	PROGRAM LOCK REGISTER	2	WRITE	LRA	0xC0	WRITE	LRA	LRD
Configuration	CONFIGURE READ CONFIGURATION REGISTER	2	WRITE	RCD	0x60	WRITE	RCD	0x03
Blank Check	BLOCK BLANK CHECK	2	WRITE	BA	0xBC	WRITE	BA	D0
EFI	EXTENDED FUNCTION INTERFACE [5]	>2	WRITE	WA	0xEB	Write	WA	Sub-Op code

Notes:
1. First command cycle address should be the same as the operation's target address. DBA = Device base address (needed for dual die 512Mb device); DnA = Address within the device; IA = Identification code address offset; CFI-A = Read CFI address offset; WA = Word address of memory location to be written; BA = Address within the block; OTP-RA = Protection register address; LRA = Lock register address; RCD = Read configuration register data on A[16:1] for Easy BGA and TSOP, A[15:0] for QUAD+ package.
2. ID = Identifier data; CFI-D = CFI data on DQ[15:0]; SRD = Status register data; WD = Word data; N = Word count of data to be loaded into the write buffer; OTP-D = Protection register data; LRD = Lock register data.

3. The second cycle of the BUFFERED PROGRAM command is the word count of the data to be loaded into the write buffer. This is followed by up to 512 words of data. Then the CONFIRM command (0xD0) is issued, triggering the array programming operation.
4. The CONFIRM command (0xD0) is followed by the buffer data.
5. The second cycle is a Sub-Op-Code, the data written on third cycle is N-1; 1≤ N ≤ 512. The subsequent cycles load data words into the program buffer at a specified address until word count is achieved, after the data words are loaded, the final cycle is the confirm cycle 0xD0).

Read Operations

The device supports two read modes: asynchronous page mode and synchronous burst mode. Asynchronous page mode is the default read mode after device power-up or a reset. Under asynchronous page mode, the device can also perform single word read. The read configuration register must be configured to enable synchronous burst reads of the array.

The device can be in any of four read states: read array, read identifier, read status, or read CFI. Upon power-up, or after a reset, the device defaults to read array. To change the read state, the appropriate READ command must be written to the device.

Asynchronous Page Mode Read

Following a device power-up or reset, asynchronous page mode is the default read mode and the device is set to read array. However, to perform array reads after any other device operation (WRITE operation), the READ ARRAY command must be issued in order to read from the array.

Asynchronous page mode reads can only be performed when read configuration register bit RCR15 is set.

To perform an asynchronous page-mode read, an address is driven onto the address bus, and CE# and ADV# are asserted. WE# and RST# must already have been de-asserted. WAIT is de-asserted during asynchronous page mode. ADV# can be driven HIGH to latch the address, or it must be held LOW throughout the READ cycle. CLK is not used for asynchronous page mode reads, and is ignored. If only asynchronous reads are to be performed, CLK should be tied to a valid V_{IH} or V_{SS} level, WAIT signal can be floated, and ADV# must be tied to ground. Array data is driven onto DQ[15:0] after an initial access time ^{t}AVQV delay.

In asynchronous page mode, 16 data words are "sensed" simultaneously from the array and loaded into an internal page buffer. The buffer word corresponding to the initial address on the address bus is driven onto DQ[15:0] after the initial access delay. The lowest four address bits determine which word of the 16-word page is output from the data buffer at any given time.

Note: Asynchronous page read mode is only supported in main array.

Asynchronous Single Word Read

To perform an asynchronous single word read, an address is driven onto the address bus, and CE# is asserted. ADV# can either be driven HIGH to latch the address or be held LOW throughout the READ cycle. WE# and RST# must already have been de-asserted. WAIT is set to a de-asserted state during single word mode, as determined by bit 10 of the read configuration register. CLK is not used for asynchronous single word reads, and is ignored. If asynchronous reads are to be performed only, CLK should be tied to a valid V_{IH} or V_{SS} level, WAIT can be floated, and ADV# must be tied to ground. After OE# is asserted, the data is driven onto DQ[15:0] after an initial access time ^{t}AVQV or ^{t}GLQV delay.

Synchronous Burst Mode Read

Read configuration register bits RCR[15:0] must be set before synchronous burst operation can be performed. Synchronous burst mode can be performed for both array and non-array reads such as read ID, read status, or read query.

To perform a synchronous burst read, an initial address is driven onto the address bus, and CE# and ADV# are asserted. WE# and RST# must already have been de-asserted. ADV# is asserted, and then de-asserted to latch the address. Alternately, ADV# can remain asserted throughout the burst access, in which case the address is latched on the next valid CLK edge while ADV# is asserted.

During synchronous array and non-array read modes, the first word is output from the data buffer on the next valid CLK edge after the initial access latency delay. Subsequent data is output on valid CLK edges following a minimum delay. However, for a synchronous non-array read, the same word of data will be output on successive clock edges until the burst length requirements are satisfied. Refer to the timing diagrams for more detailed information.

Read CFI

The READ CFI command instructs the device to output CFI data when read. See Common Flash Interface for details on issuing the READ CFI command, and for details on addresses and offsets within the CFI database.

Read Device ID

The READ DEVICE IDENTIFIER command instructs the device to output manufacturer code, device identifier code, block lock status, protection register data, or configuration register data.

Table 10: Device ID Information

Item	Address	Data
Manufacturer code	0x00	0x89
Device ID code	0x01	ID (see the Device ID Codes table)
Block lock configuration Block is unlocked Block is locked Block is not locked down Block is locked down	Block base address + 0x02	**Lock bit** DQ_0 = 0b0 DQ_0 = 0b1 DQ_1 = 0b0 DQ_1 = 0b1
Read configuration register	0x05	RCR contents
General purpose register	Device base address + 0x07	General purpose register data
Lock register 0	0x80	PR-LK0 data
64-bit factory-programmed OTP register	0x81–0x84	Factory OTP register data
64-bit user-programmable OTP register	0x85–0x88	User OTP register data
Lock register 1	0x89	PR-LK1 OTP register lock data
128-bit user-programmable protection registers	0x8A–0x109	OTP register data

Device ID Codes

Table 11: Device ID codes

ID Code Type	Device Density	Device Identifier Codes	
		–T (Top Parameter)	–B (Bottom Parameter)
Device Code	256Mb	891F	8922

Note: 1. The 512Mb devices do not have a unique device ID associated with them. Each die within the stack can be identified by device ID codes.

Program Operations

Successful programming requires the addressed block to be unlocked. If the block is locked down, WP# must be de-asserted and the block must be unlocked before attempting to program the block. Attempting to program a locked block causes a program error (SR4 and SR1 set) and termination of the operation. See Security Modes for details on locking and unlocking blocks.

Word Programming (40h)

Word programming operations are initiated by writing the WORD PROGRAM SETUP command to the device (see the Command Codes and Definitions table). This is followed by a second write to the device with the address and data to be programmed. The device outputs status register data when read (see the Word Program Flowchart). V_{PP} must be above V_{PPLK}, and within the specified V_{PPL} MIN/MAX values.

During programming, the device executes a sequence of internally-timed events that program the desired data bits at the addressed location, and verifies that the bits are sufficiently programmed. Programming the array changes 1s to 0s. Memory array bits that are 0s can be changed to 1s only by erasing the block (see Erase Operations).

The status register can be examined for programming progress and errors by reading at any address. The device remains in the read status register state until another command is written to the device.

SR7 indicates the programming status while the sequence executes. Commands that can be issued to the device during programming are PROGRAM SUSPEND, READ STATUS REGISTER, READ DEVICE IDENTIFIER, READ CFI, and READ ARRAY (this returns unknown data).

When programming has finished, SR4 (when set) indicates a programming failure. If SR3 is set, the device could not perform the WORD PROGRAMMING operation because V_{PP} was outside of its acceptable limits. If SR1 is set, the WORD PROGRAMMING operation attempted to program a locked block, causing the operation to abort.

Before issuing a new command, the status register contents should be examined and then cleared using the CLEAR STATUS REGISTER command. Any valid command can follow, when word programming has completed.

Buffered Programming (E8h, D0h)

The device features a 512-word buffer to enable optimum programming performance. For buffered programming, data is first written to an on-chip write buffer. Then the buffer data is programmed into the array in buffer-size increments. This can improve system programming performance significantly over non-buffered programming.

When the BUFFERED PROGRAMMING SETUP command is issued, status register information is updated and reflects the availability of the buffer. SR7 indicates buffer availability: if set, the buffer is available; if cleared, the buffer is not available.

Note: The device default state is to output SR data after the BUFFERED PROGRAMMING SETUP command. CE# and OE# LOW drive device to update status register. It is not allowed to issue 70h to read SR data after E8h command; otherwise, 70h would be counted as word count.

On the next write, a word count is written to the device at the buffer address. This tells the device how many data words will be written to the buffer, up to the maximum size of the buffer.

On the next write, a device start address is given along with the first data to be written to the flash memory array. Subsequent writes provide additional device addresses and data. All data addresses must lie within the start address plus the word count. Optimum programming performance and lower power usage are obtained by aligning the starting address at the beginning of a 512-word boundary (A[9:1] = 0x00 for Easy BGA and TSOP, A[8:0] for QUAD+ package; see Part Numbering Information). The maximum buffer size would be 256-word if the misaligned address range is crossing a 512-word boundary during programming.

After the last data is written to the buffer, the BUFFERED PROGRAMMING CONFIRM command must be issued to the original block address. The device begins to program buffer contents to the array. If a command other than the BUFFERED PROGRAMMING CONFIRM command is written to the device, a command sequence error occurs and SR[7,5,4] are set. If an error occurs while writing to the array, the device stops programming, and SR[7,4] are set, indicating a programming failure.

When buffered programming has completed, additional buffer writes can be initiated by issuing another BUFFERED PROGRAMMING SETUP command and repeating the buffered program sequence. Buffered programming may be performed with $V_{PP} = V_{PPL}$ or V_{PPH} (see Operating Conditions for limitations when operating the device with $V_{PP} = V_{PPH}$).

If an attempt is made to program past an erase-block boundary using the BUFFERED PROGRAM command, the device aborts the operation. This generates a command sequence error, and SR[5,4] are set.

If buffered programming is attempted while V_{PP} is at or below V_{PPLK}, SR[4,3] are set. If any errors are detected that have set status register bits, the status register should be cleared using the CLEAR STATUS REGISTER command.

Buffered Enhanced Factory Programming (80h, D0h)

Buffered enhanced factory programming (BEFP) speeds up multilevel cell (MLC) programming. The enhanced programming algorithm used in BEFP eliminates traditional programming elements that drive up overhead in device programmer systems.

BEFP consists of three phases: setup, program/verify, and exit (see the BEFP Flowchart). It uses a write buffer to spread MLC program performance across 512 data words. Verification occurs in the same phase as programming to accurately program the cell to the correct bit state.

A single two-cycle command sequence programs the entire block of data. This enhancement eliminates three write cycles per buffer: two commands and the word count for each set of 512 data words. Host programmer bus cycles fill the device write buffer followed by a status check. SR0 indicates when data from the buffer has been programmed into sequential array locations.

Following the buffer-to-flash array programming sequence, the device increments internal addressing to automatically select the next 512-word array boundary. This aspect of BEFP saves host programming equipment the address bus setup overhead.

With adequate continuity testing, programming equipment can rely on the device's internal verification to ensure that the device has programmed properly. This eliminates the external post-program verification and its associated overhead.

Table 12: BEFP Requirements

Parameter/Issue	Requirement	Notes
Case temperature	T_C = 30°C ± 10°C	
V_{CC}	Nominal V_{CC}	
V_{PP}	Driven to V_{PPH}	
Setup and confirm	Target block must be unlocked before issuing the BEFP Setup and Confirm commands.	
Programming	The first-word address (WA0) of the block to be programmed must be held constant from the setup phase through all data streaming into the target block, until transition to the exit phase is desired.	
Buffer alignment	WA0 must align with the start of an array buffer boundary.	1

Note: 1. Word buffer boundaries in the array are determined by the lowest 9 address bits (0x000 through 0x1FF). The alignment start point is 0x000.

Table 13: BEFP Considerations

Parameter/Issue	Requirement	Notes
Cycling	For optimum performance, cycling must be limited below 50 ERASE cycles per block.	1
Programming blocks	BEFP programs one block at a time; all buffer data must fall within a single block.	2
Suspend	BEFP cannot be suspended.	
Programming the array	Programming to the array can occur only when the buffer is full.	3

Notes:
1. Some degradation in performance may occur if this limit is exceeded, but the internal algorithm continues to work properly.
2. If the internal address counter increments beyond the block's maximum address, addressing wraps around to the beginning of the block.
3. If the number of words is less than 512, remaining locations must be filled with 0xFFFF.

BEFP Setup Phase: After receiving the BEFP SETUP and CONFIRM command sequence, SR7 (ready) is cleared, indicating that the device is busy with BEFP algorithm startup. A delay before checking SR7 is required to allow the device enough time to perform all of its setups and checks (block lock status, V_{PP} level, etc.). If an error is detected, SR4 is set and BEFP operation terminates. If the block was found to be locked, SR1 is also set. SR3 is set if the error occurred due to an incorrect V_{PP} level.

Note: Reading from the device after the BEFP SETUP and CONFIRM command sequence outputs status register data. Do not issue the READ STATUS REGISTER command; it will be interpreted as data to be loaded into the buffer.

BEFP Program/Verify Phase: After the BEFP setup phase has completed, the host programming system must check SR[7,0] to determine the availability of the write buffer for data streaming. SR7 cleared indicates the device is busy and the BEFP program/verify phase is activated. SR0 indicates the write buffer is available.

Two basic sequences repeat in this phase: loading of the write buffer, followed by buffer data programming to the array. For BEFP, the count value for buffer loading is always the maximum buffer size of 512 words. During the buffer-loading sequence, data is stored to sequential buffer locations starting at address 0x00. Programming of the buffer contents to the array starts as soon as the buffer is full. If the number of words is less than 512, the remaining buffer locations must be filled with 0xFFFF.

Note: The buffer must be completely filled for programming to occur. Supplying an address outside of the current block's range during a buffer-fill sequence causes the algorithm to exit immediately. Any data previously loaded into the buffer during the fill cycle is not programmed into the array.

The starting address for data entry must be buffer size aligned; if not, the BEFP algorithm will be aborted, the program fails, and the (SR4) flag will be set.

Data words from the write buffer are directed to sequential memory locations in the array; programming continues from where the previous buffer sequence ended. The host programming system must poll SR0 to determine when the buffer program sequence completes. SR0 cleared indicates that all buffer data has been transferred to the array; SR0 set indicates that the buffer is not available yet for the next fill cycle. The host system may check full status for errors at any time, but it is only necessary on a block basis after BEFP exit. After the buffer fill cycle, no WRITE cycles should be issued to the device until SR0 = 0 and the device is ready for the next buffer fill.

Note: Any spurious writes are ignored after a BUFFER FILL operation and when internal program is proceeding.

The host programming system continues the BEFP algorithm by providing the next group of data words to be written to the buffer. Alternatively, it can terminate this phase by changing the block address to one outside of the current block's range.

The program/verify phase concludes when the programmer writes to a different block address; data supplied must be 0xFFFF. Upon program/verify phase completion, the device enters the BEFP exit phase.

Program Suspend

Issuing the PROGRAM SUSPEND command while programming suspends the programming operation. This allows data to be accessed from the device other than the one being programmed. The PROGRAM SUSPEND command can be issued to any device address. A PROGRAM operation can be suspended to perform reads only. Additionally, a PROGRAM operation that is running during an erase suspend can be suspended to perform a READ operation.

When a programming operation is executing, issuing the PROGRAM SUSPEND command requests the device to suspend the programming algorithm at predetermined points. The device continues to output status register data after the PROGRAM SUSPEND command is issued. Programming is suspended when SR[7,2] are set.

To read data from the device, the READ ARRAY command must be issued. READ ARRAY, READ STATUS REGISTER, READ DEVICE IDENTIFIER, READ CFI, and PROGRAM RESUME valid commands during a program suspend.

During a program suspend, de-asserting CE# places the device in standby, reducing active current. V_{PP} must remain at its programming level, and WP# must remain unchanged while in program suspend. If RST# is asserted, the device is reset.

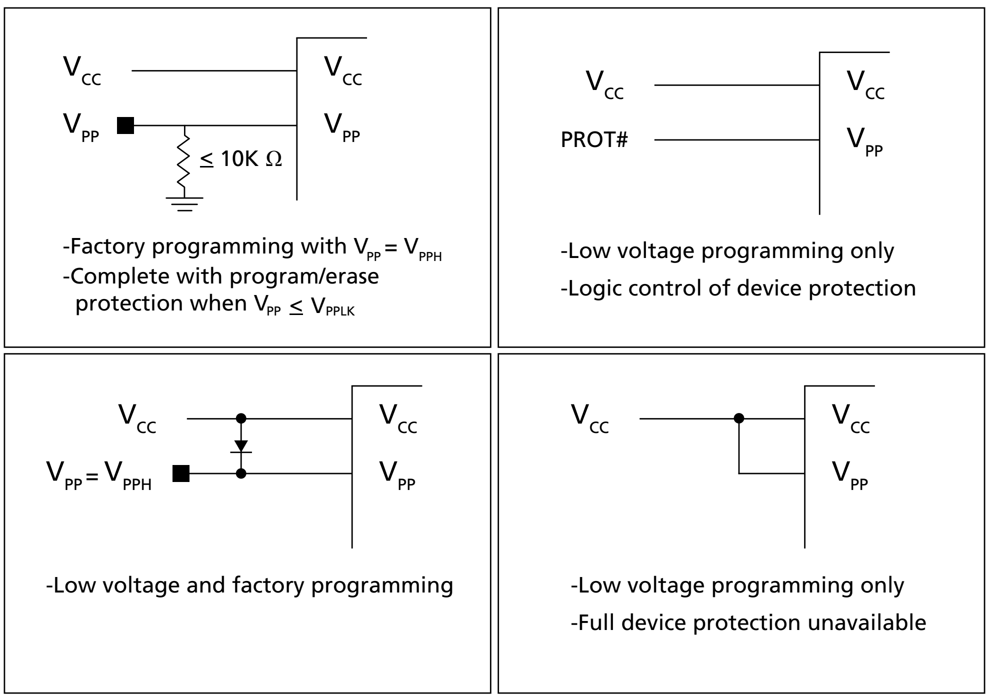
Program Resume

The RESUME command instructs the device to continue programming, and automatically clears SR[7,2]. This command can be written to any address. If error bits are set, the status register should be cleared before issuing the next command. RST# must remain de-asserted.

Program Protection

When $V_{PP} = V_{IL}$, absolute hardware write protection is provided for all device blocks. If V_{PP} is at or below V_{PPLK}, programming operations halt and SR3 is set, indicating a V_{PP}-level error. Block lock registers are not affected by the voltage level on V_{PP}; they may still be programmed and read, even if V_{PP} is less than V_{PPLK}.

Figure 7: Example V_{PP} Supply Connections



Erase Operations

BLOCK ERASE Command

ERASE operations are performed on a block basis. An entire block is erased each time a BLOCK ERASE command sequence is issued, and only one block is erased at a time. When a block is erased, each bit within that block reads as a logical 1.

A BLOCK ERASE operation is initiated by writing the BLOCK ERASE SETUP command to the address of the block to be erased, followed by the BLOCK ERASE CONFIRM command. If the device is placed in standby (CE# de-asserted) during a BLOCK ERASE operation, the device completes the operation before entering standby. The V_{PP} value must be above V_{PPLK} and the block must be unlocked.

During a BLOCK ERASE operation, the device executes a sequence of internally-timed events that conditions, erases, and verifies all bits within the block. Erasing the array changes the value in each cell from a 1 to a 0. Memory block array cells that with a value of 1 can be changed to 0 only by programming the block.

The status register can be examined for block erase progress and errors by reading any address. The device remains in the read status register state until another command is written. SR0 indicates whether the addressed block is erasing. SR7 is set upon erase completion.

SR7 indicates block erase status while the sequence executes. When the BLOCK ERASE operation has completed, SR5 = 1 (set) indicates an erase failure. SR3 = 1 indicates that the device could not perform the BLOCK ERASE operation because V_{PP} was outside of its acceptable limits. SR1 = 1 indicates that the BLOCK ERASE operation attempted to erase a locked block, causing the operation to abort.

Before issuing a new command, the status register contents should be examined and then cleared using the CLEAR STATUS REGISTER command. Any valid command can follow after the BLOCK ERASE operation has completed.

The BLOCK ERASE operation is aborted by performing a reset or powering down the device. In either case, data integrity cannot be ensured, and it is recommended to erase again the blocks aborted.

BLANK CHECK Command

The BLANK CHECK operation determines whether a specified main block is blank; that is, completely erased. Other than a BLANK CHECK operation, only a BLOCK ERASE operation can ensure a block is completely erased. BLANK CHECK is especially useful when a BLOCK ERASE operation is interrupted by a power loss event.

A BLANK CHECK operation can apply to only one block at a time. The only operation allowed simultaneously is a READ STATUS REGISTER operation. SUSPEND and RESUME operations and a BLANK CHECK operation are mutually exclusive.

A BLANK CHECK operation is initiated by writing the BLANK CHECK SETUP command to the block address, followed by the CHECK CONFIRM command. When a successful command sequence is entered, the device automatically enters the read status state. The device then reads the entire specified block and determines whether any bit in the block is programmed or over-erased.

BLANK CHECK operation progress and errors are determined by reading the status register at any address within the block being accessed. SR7 = 0 is a BLANK CHECK busy status. SR7 = 1 is a BLANK CHECK operation complete status. The status register should be checked for any errors and then cleared. If the BLANK CHECK operation fails, meaning the block is not completely erased, SR5 = 1. CE# or OE# toggle (during polling) updates the status register.

The READ STATUS REGISTER command must always be followed by a CLEAR STATUS REGISTER command. The device remains in status register mode until another command is written to the device. Any command can follow once the BLANK CHECK command is complete.

ERASE SUSPEND Command

The ERASE SUSPEND command suspends a BLOCK ERASE operation that is in progress, enabling access to data in memory locations other than the one being erased. The ERASE SUSPEND command can be issued to any device address. A BLOCK ERASE operation can be suspended to perform a WORD or BUFFER PROGRAM operation, or a READ operation within any block except the block that is erase suspended.

When a BLOCK ERASE operation is executing, issuing the ERASE SUSPEND command requests the device to suspend the erase algorithm at predetermined points. The device continues to output status register data after the ERASE SUSPEND command is issued. Block erase is suspended when SR[7,6] are set.

To read data from the device (other than an erase-suspended block), the READ ARRAY command must be issued. During erase suspend, a PROGRAM command can be issued to any block other than the erase-suspended block. Block erase cannot resume until program operations initiated during erase suspend complete. READ ARRAY, READ STATUS REGISTER, READ DEVICE IDENTIFIER, READ CFI, and ERASE RESUME are valid commands during erase suspend. Additionally, CLEAR STATUS REGISTER, PROGRAM, PROGRAM SUSPEND, BLOCK LOCK, BLOCK UNLOCK, and BLOCK LOCK DOWN are valid commands during an ERASE SUSPEND operation.

During an erase suspend, de-asserting CE# places the device in standby, reducing active current. V_{PP} must remain at a valid level, and WP# must remain unchanged while in erase suspend. If RST# is asserted, the device is reset.

ERASE RESUME Command

The ERASE RESUME command instructs the device to continue erasing, and automatically clears SR[7,6]. This command can be written to any address. If status register error bits are set, the status register should be cleared before issuing the next instruction. RST# must remain de-asserted.

Erase Protection

When $V_{PP} = V_{IL}$, absolute hardware erase protection is provided for all device blocks. If V_{PP} is at or below V_{PPLK}, ERASE operations halt and SR3 is set indicating a V_{PP}-level error.

Security Operations

Block Locking

Individual instant block locking is used to protect user code and/or data within the flash memory array. All blocks power-up in a locked state to protect array data from being altered during power transitions. Any block can be locked or unlocked with no latency. Locked blocks cannot be programmed or erased; they can only be read.

Software-controlled security is implemented using the BLOCK LOCK and BLOCK UNLOCK commands. Hardware-controlled security can be implemented using the BLOCK LOCK DOWN command along with asserting WP#. Also, V_{PP} data security can be used to inhibit PROGRAM and ERASE operations.

BLOCK LOCK Command

To lock a block, issue the BLOCK LOCK SETUP command, followed by the BLOCK LOCK command issued to the desired block's address. If the SET READ CONFIGURATION REGISTER command is issued after the BLOCK LOCK SETUP command, the device configures the RCR instead.

BLOCK LOCK and UNLOCK operations are not affected by the voltage level on V_{PP}. The block lock bits may be modified and/or read even if V_{PP} is at or below V_{PPLK}.

BLOCK UNLOCK Command

The BLOCK UNLOCK command is used to unlock blocks. Unlocked blocks can be read, programmed, and erased. Unlocked blocks return to a locked state when the device is reset or powered down. If a block is in a lock-down state, WP# must be de-asserted before it can be unlocked.

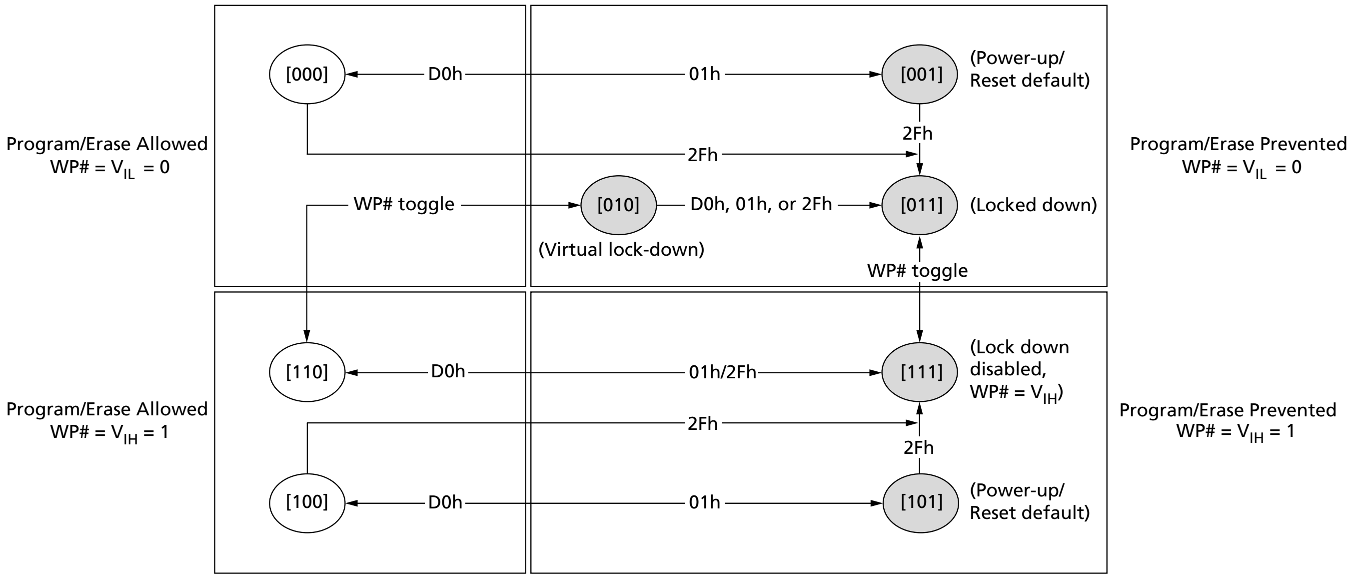
BLOCK LOCK DOWN Command

A locked or unlocked block can be locked-down by writing the BLOCK LOCK DOWN command sequence. Blocks in a lock-down state cannot be programmed or erased; they can only be read. However, unlike locked blocks, their locked state cannot be changed by software commands alone. A locked-down block can only be unlocked by issuing the BLOCK UNLOCK command with WP# de-asserted. To return an unlocked block to locked-down state, a BLOCK LOCK DOWN command must be issued prior to changing WP# to V_{IL}. Locked-down blocks revert to the locked state upon reset or power up the device.

Block Lock Status

The READ DEVICE IDENTIFIER command is used to determine a block's lock status. DQ[1:0] display the addressed block's lock status; DQ0 is the addressed block's lock bit, while DQ1 is the addressed block's lock-down bit.

Figure 8: Block Locking State Diagram



Note: 1. D0h = UNLOCK command; 01h = LOCK command; 60h (not shown) LOCK SETUP command; 2Fh = LOCK DOWN command.

Block Locking During Suspend

Block lock and unlock changes can be performed during an erase suspend. To change block locking during an ERASE operation, first issue the ERASE SUSPEND command. Monitor the status register until SR7 and SR6 are set, indicating the device is suspended and ready to accept another command.

Next, write the desired lock command sequence to a block, which changes the lock state of that block. After completing BLOCK LOCK or BLOCK UNLOCK operations, resume the ERASE operation using the ERASE RESUME command.

Note:

A BLOCK LOCK SETUP command followed by any command other than BLOCK LOCK, BLOCK UNLOCK, or BLOCK LOCK DOWN produces a command sequence error and set SR4 and SR5. If a command sequence error occurs during an erase suspend, SR4 and SR5 remains set, even after the erase operation is resumed. Unless the Status Register is cleared using the CLEAR STATUS REGISTER command before resuming the ERASE operation, possible erase errors may be masked by the command sequence error.

If a block is locked or locked-down during an erase suspend of the *same* block, the lock status bits change immediately. However, the ERASE operation completes when it is resumed. BLOCK LOCK operations cannot occur during a program suspend.

Selectable OTP Blocks

The OTP security feature on the device is backward-compatible to the earlier generation devices. Contact your local Micron representative for details about its implementation.

Password Access

The password access is a security enhancement offered on the device. This feature protects information stored in array blocks by preventing content alteration or reads until a valid 64-bit password is received. The password access may be combined with nonvolatile protection and/or volatile protection to create a multi-tiered solution.

Contact your Micron sales office for further details concerning password access.

Status Register

Read Status Register

To read the status register, issue the READ STATUS REGISTER command at any address. Status register information is available at the address that the READ STATUS REGISTER, WORD PROGRAM, or BLOCK ERASE command is issued to. Status register data is automatically made available following a word program, block erase, or block lock command sequence. Reads from the device after any of these command sequences will output the devices status until another valid command is written (e.g. READ ARRAY command).

The status register is read using single asynchronous mode or synchronous burst mode reads. Status register data is output on DQ[7:0], while 0x00 is output on DQ[15:8]. In asynchronous mode, the falling edge of OE# or CE# (whichever occurs first) updates and latches the status register contents. However, when reading the status register in synchronous burst mode, CE# or ADV# must be toggled to update status data.

The device write status bit (SR7) provides the overall status of the device. SR[6:1] present status and error information about the PROGRAM, ERASE, SUSPEND, V_{PP}, and BLOCK LOCK operations.

Note: Reading the status register is a nonarray READ operation. When the operation occurs in asynchronous page mode, only the first data is valid and all subsequent data are undefined. When the operation occurs in synchronous burst mode, the same data word requested will be output on successive clock edges until the burst length requirements are satisfied.

Table 14: Status Register Description

Notes apply to entire table

Bits	Name	Bit Settings	Description
7	Device write status (DWS)	0 = Busy 1 = Ready	**Status bit:** Indicates whether a PROGRAM or ERASE command cycle is in progress.
6	Erase Suspend Status (ESS)	0 = Not in effect 1 = In effect	**Status bit:** Indicates whether an ERASE operation has been or is going to be suspended.
5:4	Erase/Blank check status (ES) Program status (PS)	00 = PROGRAM/ERASE successful 01 = PROGRAM error 10 = ERASE/BLANK CHECK error 11 = Command sequence error	**Status/Error bit:** Indicates whether an ERASE/ BLANK CHECK or PROGRAM operation was successful. When an error is returned, the operation is aborted.
3	V_{PP} status (VPPS)	0 = Within limits 1 = Exceeded limits ($V_{PP} \le V_{PPLK}$)	**Status bit:** Indicates whether a PROGRAM/ERASE operation is within acceptable voltage range limits.
2	Program suspend status (PSS)	0 = Not in effect 1 = In effect	**Status bit:** Indicates whether a PROGRAM operation has been or is going to be suspended.
1	Block lock status (BLS)	0 = Not locked 1 = Locked (operation aborted)	**Status bit:** Indicates whether a block is locked when a PROGRAM or ERASE operation is initiated.
0	BEFP status (BWS)	0 = BEFP complete 1 = BEFP in progress	**Status bit:** Indicates whether BEFP data has completed loading into the buffer.

Notes: 1. Default value = 0x80.

2. Always clear the status register prior to resuming ERASE operations. This eliminates status register ambiguity when issuing commands during ERASE SUSPEND. If a command sequence error occurs during an ERASE SUSPEND, the status register contains the command sequence error status (SR[7,5,4] set). When the ERASE operation resumes and finishes, possible errors during the operation cannot be detected via the status register because it contains the previous error status.
3. When bits 5:4 indicate a PROGRAM/ERASE operation error, either a CLEAR STATUS REGISTER 50h) or a RESET command must be issued with a 15µs delay.

Clear Status Register

The CLEAR STATUS REGISTER command clears the status register. It functions independently of V_{PP}. The device sets and clears SR[7,6,2], but it sets bits SR[5:3,1] without clearing them. The status register should be cleared before starting a command sequence to avoid any ambiguity. A device reset also clears the status register.

Configuration Register

Read Configuration Register

The read configuration register (RCR) is a 16-bit read/write register used to select bus read mode (synchronous or asynchronous) and to configure device synchronous burst read characteristics. To modify RCR settings, use the CONFIGURE READ CONFIGURATION REGISTER command. RCR contents can be examined using the READ DEVICE IDENTIFIER command and then reading from offset 0x05. On power-up or exit from reset, the RCR defaults to asynchronous mode. RCR bits are described in more detail below.

Note: Reading the configuration register is a nonarray READ operation. When the operation occurs in asynchronous page mode, only the first data is valid, and all subsequent data are undefined. When the operation occurs in synchronous burst mode, the same word of data requested will be output on successive clock edges until the burst length requirements are satisfied.

Table 15: Read Configuration Register

Bits	Name	Settings/Description
15	Read mode (RM)	0 = Synchronous burst mode read 1 = Asynchronous page mode read (default)
14:11	Latency count (LC[3:0])	0000 = Code 0 (reserved) 0001 = Code 1 (reserved) 0010 = Code 2 0011 = Code 3 0100 = Code 4 0101 = Code 5 0110 = Code 6 0111 = Code 7 1000 = Code 8 1001 = Code 9 1010 = Code 10 1011 = Code11 1100 = Code 12 1101 = Code 13 1110 = Code 14 1111 = Code 15 (default)
10	WAIT polarity (WP)	0 = WAIT signal is active LOW (default) 1 = WAIT signal is active HIGH
9	Reserved (R)	Default 0, Nonchangeable
8	WAIT delay (WD)	0 = WAIT de-asserted with valid data 1 = WAIT de-asserted one data cycle before valid data (default)
7	Burst sequence (BS)	Default 0, Nonchangeable
6	Clock edge (CE)	0 = Falling edge 1 = Rising edge (default)
5:4	Reserved (R)	Default 0, Nonchangeable
3	Burst wrap (BW)	0 = Wrap; Burst accesses wrap within burst length set by BL[2:0] 1 = No Wrap; Burst accesses do not wrap within burst length (default)
2:0	Burst length (BL[2:0])	001 = 4-word burst 010 = 8-word burst 011 = 16-word burst 111 = Continuous burst (default) (Other bit settings are reserved)

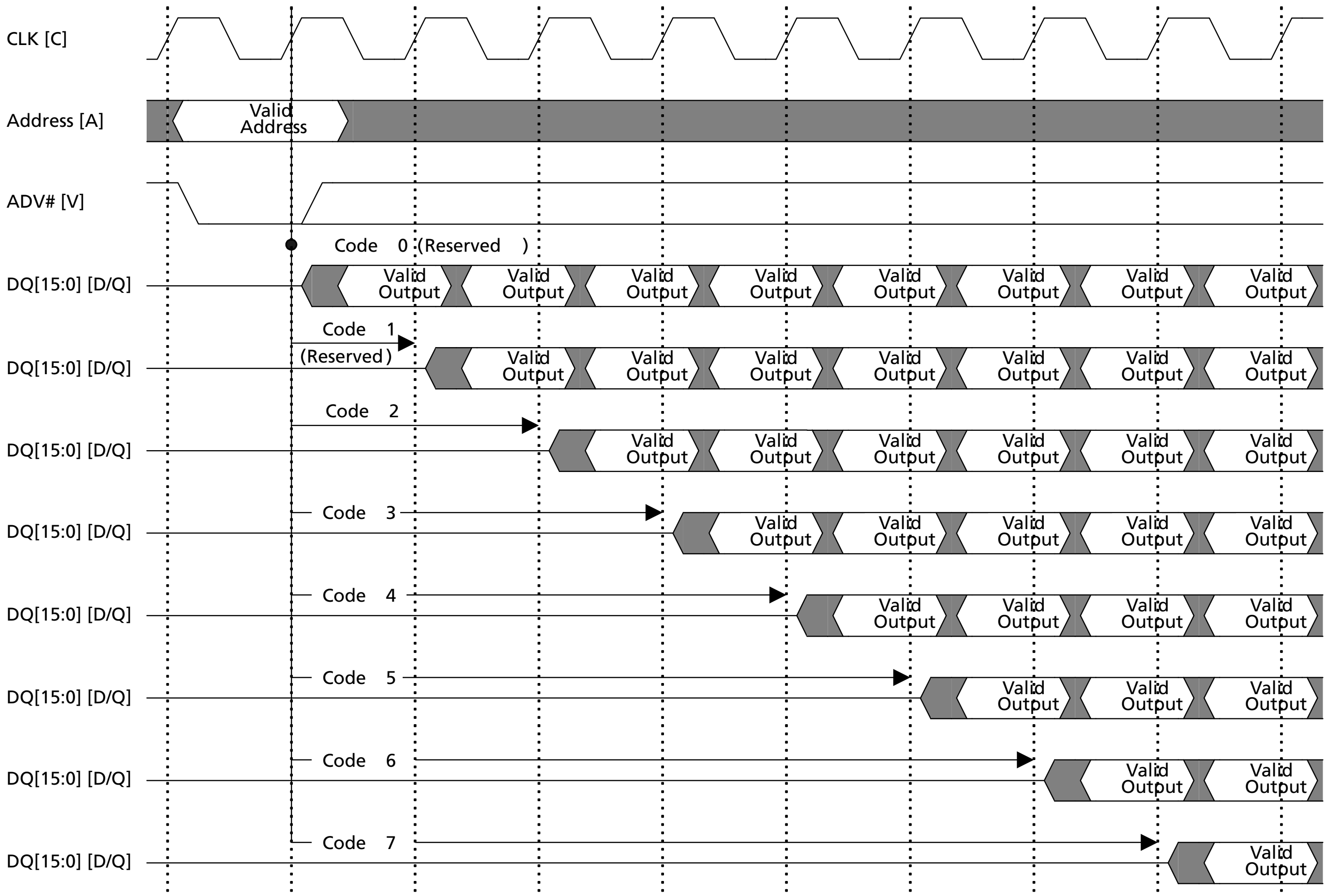
Read Mode

The read mode (RM) bit selects synchronous burst mode or asynchronous page mode operation for the device. When the RM bit is set, asynchronous page mode is selected (default). When RM is cleared, synchronous burst mode is selected.

Latency Count

The latency count (LC) bits tell the device how many clock cycles must elapse from the rising edge of ADV# (or from the first valid clock edge after ADV# is asserted) until the first valid data word is driven to DQ[15:0]. The input clock frequency is used to determine this value. The First Access Latency Count figure shows the data output latency for different LC settings.

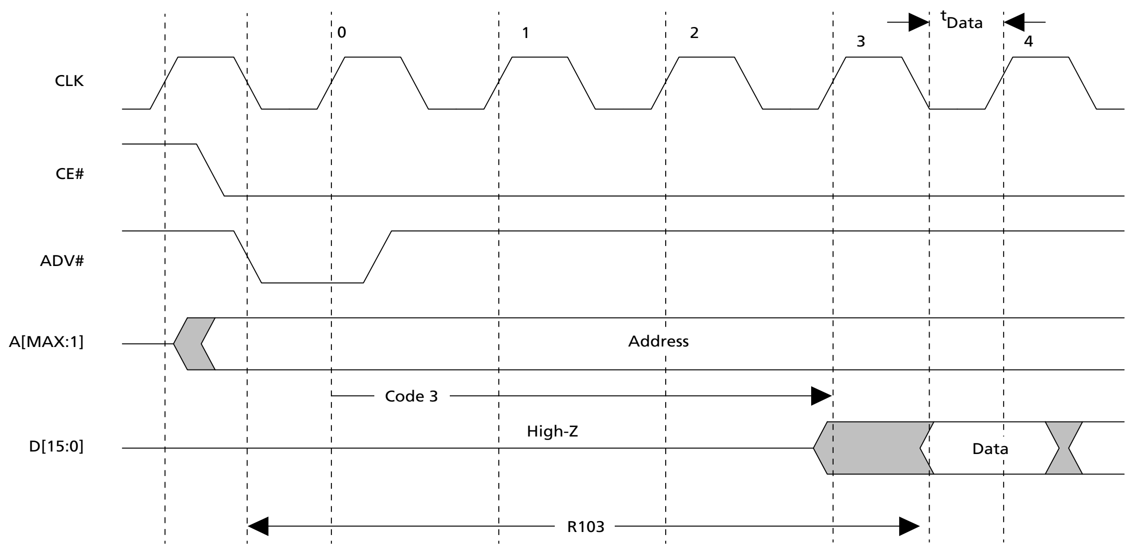
Figure 9: First Access Latency Count



Note: 1. First Access Latency Count Calculation:

- 1 / CLK frequency = CLK period (ns)
- n x (CLK period) ≥ ^{t}AVQV (ns) – ^{t}CHQV (ns)
- Latency Count = n

Figure 10: Example Latency Count Setting Using Code 3



End of Wordline Considerations

End of wordline (EOWL) wait states can result when the starting address of the burst operation is not aligned to a 16-word boundary; that is, A[4:1] of the start address does not equal 0x0. The figure below illustrates the end of wordline wait state(s) that occur after the first 16-word boundary is reached. The number of data words and wait states is summarized in the table below.

Figure 11: End of Wordline Timing Diagram

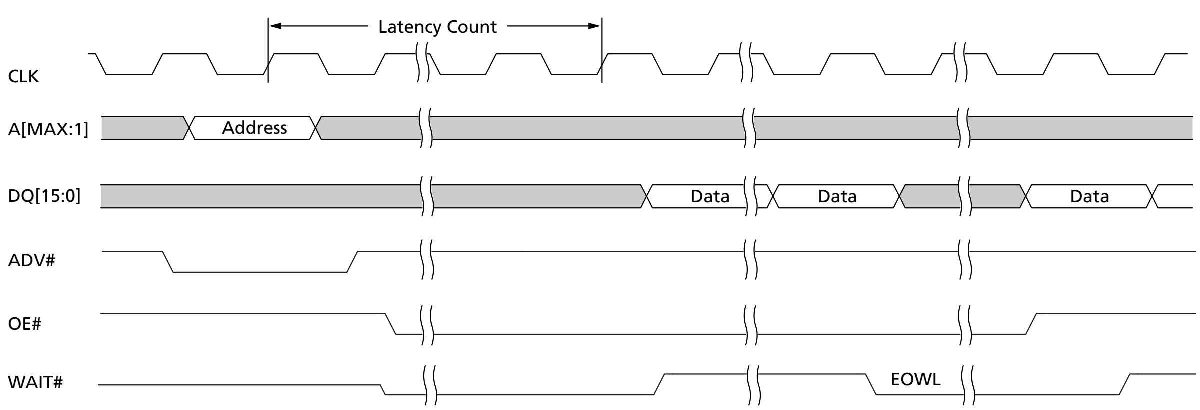


Table 16: End of Wordline Data and WAIT State Comparison

Latency Count	130nm		65nm	
	Data Words	WAIT States	Data Words	WAIT States
1	Not Supported	Not Supported	Not Supported	Not Supported
2	4	0 to 1	16	0 to 1
3	4	0 to 2	16	0 to 2
4	4	0 to 3	16	0 to 3
5	4	0 to 4	16	0 to 4
6	4	0 to 5	16	0 to 5
7	4	0 to 6	16	0 to 6
8	Not Supported	Not Supported	16	0 to 7
9			16	0 to 8
10			16	0 to 9
11			16	0 to 10
12			16	0 to 11
13			16	0 to 12
14			16	0 to 13
15			16	0 to 14

WAIT Signal Polarity and Functionality

The WAIT polarity (WP) bit, RCR10 determines the asserted level (V_{OH} or V_{OL}) of WAIT. When WP is set, WAIT is asserted HIGH (default). When WP is cleared, WAIT is asserted LOW. The WAIT signal changes state on valid clock edges during active bus cycles (CE# asserted, OE# asserted, RST# de-asserted).

The WAIT signal indicates data valid when the device is operating in synchronous mode (RCR15 = 0). The WAIT signal is only de-asserted when data is valid on the bus. When the device is operating in synchronous nonarray read mode, such as read status, read ID, or read CFI, the WAIT signal is also de-asserted when data is valid on the bus. WAIT behavior during synchronous nonarray reads at the end of wordline works correctly only on the first data access. When the device is operating in asynchronous page mode, asynchronous single word read mode, and all write operations, WAIT is set to a de-asserted state as determined by RCR10.

Table 17: WAIT Functionality Table

Condition	WAIT	Notes
CE# = 1, OE# = X or CE# = 0, OE# = 1	High-Z	1
CE# = 0, OE# = 0	Active	1
Synchronous Array Reads	Active	1
Synchronous Nonarray Reads	Active	1
All Asynchronous Reads	De-asserted	1

Table 17: WAIT Functionality Table (Continued)

Condition	WAIT	Notes
All Writes	High-Z	1, 2

Notes:
1. Active means that WAIT is asserted until data becomes valid, then deasserts.
2. When OE# = V_{IH} during writes, WAIT = High-Z.

WAIT Delay

The WAIT delay (WD) bit controls the WAIT assertion delay behavior during synchronous burst reads. WAIT can be asserted either during or one data cycle before valid data is output on DQ[15:0]. When WD is set, WAIT is de-asserted one data cycle *before* valid data (default). When WD is cleared, WAIT is de-asserted *during* valid data.

Burst Sequence

The burst sequence (BS) bit selects linear burst sequence (default). Only linear burst sequence is supported. The synchronous burst sequence for all burst lengths, as well as the effect of the burst wrap (BW) setting are shown below.

Table 18: Burst Sequence Word Ordering

Start Address (DEC)	Burst Wrap (RCR3)	Burst Addressing Sequence (DEC)			
		4-Word Burst (BL[2:0] = 0b001)	8-Word Burst (BL[2:0] = 0b010)	16-Word Burst (BL[2:0] = 0b011)	Continuous Burst (BL[2:0] = 0b111)
0	0	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4…14-15	0-1-2-3-4-5-6-…
1	0	1-2-3-0	1-2-3-4-5-6-7-0	1-2-3-4-5…15-0	1-2-3-4-5-6-7-…
2	0	2-3-0-1	2-3-4-5-6-7-0-1	2-3-4-5-6…15-0-1	2-3-4-5-6-7-8-…
3	0	3-0-1-2	3-4-5-6-7-0-1-2	3-4-5-6-7…15-0-1-2	3-4-5-6-7-8-9-…
4	0		4-5-6-7-0-1-2-3	4-5-6-7-8…15-0-1-2-3	4-5-6-7-8-9-10…
5	0		5-6-7-0-1-2-3-4	5-6-7-8-9…15-0-1-2-3-4	5-6-7-8-9-10-11…
6	0		6-7-0-1-2-3-4-5	6-7-8-9-10…15-0-1-2-3-4-5	6-7-8-9-10-11-12-…
7	0		7-0-1-2-3-4-5-6	7-8-9-10…15-0-1-2-3-4-5-6	7-8-9-10-11-12-13…
⋮	⋮	⋮	⋮	⋮	⋮
14	0			14-15-0-1-2…12-13	14-15-16-17-18-19-20-…
15	0			15-0-1-2-3…13-14	15-16-17-18-19-20-21-…
⋮	⋮	⋮	⋮	⋮	⋮
0	1	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4…14-15	0-1-2-3-4-5-6-…
1	1	1-2-3-4	1-2-3-4-5-6-7-8	1-2-3-4-5…15-16	1-2-3-4-5-6-7-…
2	1	2-3-4-5	2-3-4-5-6-7-8-9	2-3-4-5-6…16-17	2-3-4-5-6-7-8-…
3	1	3-4-5-6	3-4-5-6-7-8-9-10	3-4-5-6-7…17-18	3-4-5-6-7-8-9-…

Table 18: Burst Sequence Word Ordering (Continued)

Start Address (DEC)	Burst Wrap (RCR3)	Burst Addressing Sequence (DEC)			
		4-Word Burst (BL[2:0] = 0b001)	8-Word Burst (BL[2:0] = 0b010)	16-Word Burst (BL[2:0] = 0b011)	Continuous Burst (BL[2:0] = 0b111)
4	1		4-5-6-7-8-9-10-11	4-5-6-7-8…18-19	4-5-6-7-8-9-10…
5	1		5-6-7-8-9-10-11-12	5-6-7-8-9…19-20	5-6-7-8-9-10-11…
6	1		6-7-8-9-10-11-12-13	6-7-8-9-10…20-21	6-7-8-9-10-11-12-…
7	1		7-8-9-10-11-12-13-14	7-8-9-10-11…21-22	7-8-9-10-11-12-13…
⋮	⋮	⋮	⋮	⋮	⋮
14	1			14-15-16-17-18…28-29	14-15-16-17-18-19-20-…
15	1			15-16-17-18-19…29-30	15-16-17-18-19-20-21-…

Clock Edge

The clock edge (CE) bit selects either a rising (default) or falling clock edge for CLK. This clock edge is used at the start of a burst cycle to output synchronous data and to assert/de-assert WAIT.

Burst Wrap

The burst wrap (BW) bit determines whether 4-word, 8-word, or 16-word burst length accesses wrap within the selected word length boundaries or cross word length boundaries. When BW is set, burst wrapping does not occur (default). When BW is cleared, burst wrapping occurs.

When performing synchronous burst reads with BW set (no wrap), an output delay may occur when the burst sequence crosses its first device row (16-word) boundary. If the burst sequence's start address is 4-word aligned, then no delay occurs. If the start address is at the end of a 4-word boundary, the worst-case output delay is one clock cycle less than the first access latency count. This delay can take place only once and doesn't occur if the burst sequence does not cross a device row boundary. WAIT informs the system of this delay when it occurs.

Burst Length

The burst length bits (BL[2:0]) select the linear burst length for all synchronous burst reads of the flash memory array. The burst lengths are 4-word, 8-word, 16-word, or continuous.

Continuous burst accesses are linear only and do not wrap within any word length boundaries. When a burst cycle begins, the device outputs synchronous burst data until it reaches the end of the "burstable" address space.

One-Time Programmable Registers

Read OTP Registers

The device contains 17 OTP registers that can be used to implement system security measures and/or device identification. Each OTP register can be individually locked.

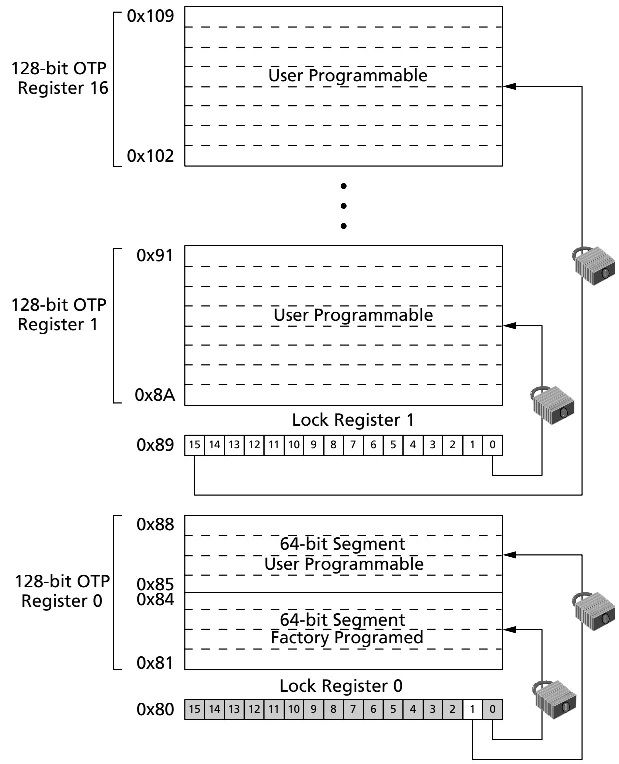
The first 128-bit OTP register is comprised of two 64-bit (8-word) segments. The lower 64-bit segment is preprogrammed at the Micron factory with a unique 64-bit number. The upper 64-bit segment, as well as the other sixteen 128-bit OTP registers, are blank. Users can program them as needed. Once programmed, users can also lock the OTP register(s) to prevent additional bit programming (see the OTP Register Map figure below).

The OTP registers contain OTP bits; when programmed, PR bits cannot be erased. Each OTP register can be accessed multiple times to program individual bits, as long as the register remains unlocked.

Each OTP register has an associated lock register bit. When a lock register bit is programmed, the associated OTP register can only be read; it can no longer be programmed. Additionally, because the lock register bits themselves are OTP, when programmed, they cannot be erased. Therefore, when an OTP register is locked, it cannot be unlocked.

The OTP registers can be read from an OTP-RA address. To read the OTP register, a READ DEVICE IDENTIFIER command is issued at an OTP-RA address to place the device in the read device identifier state. Next, a READ operation is performed using the address offset corresponding to the register to be read. The Device Identifier Information table shows the address offsets of the OTP registers and lock registers. PR data is read 16 bits at a time.

Figure 12: OTP Register Map



Program OTP Registers

To program an OTP register, a PROGRAM OTP REGISTER command is issued at the parameter's base address plus the offset of the desired OTP register location. Next, the desired OTP register data is written to the same OTP register address.

The device programs the 64-bit and 128-bit user-programmable OTP register data 16 bits at a time. Issuing the PROGRAM OTP REGISTER command outside of the OTP register's address space causes a program error (SR4 set). Attempting to program a locked OTP register causes a program error (SR4 set) and a lock error (SR1 set).

Lock OTP Registers

Each OTP register can be locked by programming its respective lock bit in the lock register. The corresponding bit in the lock register is programmed by issuing the PROGRAM LOCK REGISTER command, followed by the desired lock register data. The physical addresses of the lock registers are 0x80 for register 0 and 0x89 for register 1; these addresses are used when programming the lock registers.

Bit 0 of lock register 0 is programmed during the manufacturing process, locking the lower-half segment of the first 128-bit OTP register. Bit 1 of lock register 0, which corresponds to the upper-half segment of the first 128-bit OTP register, can be programmed by the user . When programming bit 1 of lock register 0, all other bits need to be left as 1 such that the data programmed is 0xFFFD.

Lock register 1 controls the the upper sixteen 128-bit OTP registers. Each bit of lock register 1 corresponds to a specific 128-bit OTP register. Programming a bit in lock register 1 locks the corresponding 128-bit OTP register; e.g., programming LR1.0 locks the corresponding OTP register 1.

Note: Once locked, the OTP registers cannot be unlocked.

Common Flash Interface

The CFI is part of an overall specification for multiple command-set and control-interface descriptions. System software can parse the CFI database structure to obtain information about the device, such as block size, density, bus width, and electrical specifications. The system software determines which command set to use to properly perform a WRITE command, a BLOCK ERASE or READ command, and to otherwise control the device. Information in the CFI database can be viewed by issuing the READ CFI command.

READ CFI Structure Output

The READ CFI command obtains CFI database structure information and always outputs it on the lower byte, DQ[7:0], for a word-wide (x16) device. This CFI-compliant device always outputs 00h data on the upper byte (DQ[15:8]).

The numerical offset value is the address relative to the maximum bus width the device supports. For this device family, the starting address is a 10h, which is a word address for x16 devices. For example, at this starting address of 10h, a READ CFI command outputs an ASCII Q in the lower byte and 00h in the higher byte as shown here.

In all the CFI tables shown here, address and data are represented in hexadecimal notation. In addition, because the upper byte of word-wide devices is always 00h, as shown in the example here, the leading 00 has been dropped and only the lower byte value is shown. Following is a table showing the CFI output for a x16 device, beginning at address 10h and a table showing an overview of the CFI database sections with their addresses.

Table 19: Example of CFI Output (x16 device) as a Function of Device and Mode

Device	Hex Offset	Hex Code	ASCII Value (DQ[15:8])	ASCII Value (DQ[7:0])
Address	00010:	51	00	Q
	00011:	52	00	R
	00012:	59	00	Y
	00013:	P_ID_{LO}	00	Primary vendor ID
	00014:	P_ID_{HI}	00	
	00015:	P_{LO}	00	Primary vendor table address
	00016:	P_{HI}	00	
	00017:	A_ID_{LO}	00	Alternate vendor ID
	00018:	A_ID_{HI}	00	
	: :	: :	: :	: :

Table 20: CFI Database: Addresses and Sections

Address	Section Name	Description
00001:Fh	Reserved	Reserved for vendor-specific information
00010h	CFI ID string	Flash device command set ID (identification) and vendor data offset
0001Bh	System interface information	Flash device timing and voltage
00027h	Device geometry definition	Flash device layout
P	Primary Micron-specific extended query	Vendor-defined informaton specific to the primary vendor algorithm (offset 15 defines *P* which points to the primary Micron-specific extended query table.)

Table 21: CFI ID String

Hex Offset	Length	Description	Address	Hex Code	ASCII Value (DQ[7:0])
10h	3	Query unique ASCII string “QRY”	10:	- -51	Q
			11:	- -52	R
			12:	- -59	Y
13h	2	Primary vendor command set and control interface ID code. 16-bit ID code for vendor-specified algorithms.	13:	- -01	Primary vendor ID number
			14:	- -00	
15h	2	Extended query table primary algorithm address.	15:	- -0A	Primary vendor table address, primary algorithm
			16:	- -01	
17h	2	Alternate vendor command set and control interface ID code. 0000h means no second vendor-specified algorithm exists.	17:	- -00	Alternate vendor ID number
			18:	- -00	
19h	2	Secondary algorithm extended query table address. 0000h means none exists.	19:	- -00	Primary vendor table address, secondary algorithm
			1A:	- -00	

Note: 1. The CFI ID string provides verification that the device supports the CFI specification. It also indicates the specification version and supported vendor-specific command sets.

Table 22: System Interface Information

Hex Offset	Length	Description	Address	Hex Code	ASCII Value (DQ[7:0])
1Bh	1	V_{CC} logic supply minimum program/erase voltage. bits 0 - 3 BCD 100 mV bits 4 - 7 BCD volts	1Bh	- -23	2.3V
1Ch	1	V_{CC} logic supply maximum program/erase voltage. bits 0 - 3 BCD 100 mV bits 4 - 7 BCD volts	1Ch	- -36	3.6V
1Dh	1	V_{PP} [programming] supply minimum program/ erase voltage. bits 0 - 3 BCD 100 mV bits 4 - 7 hex volts	1Dh	- -85	8.5V
1Eh	1	V_{PP} [programming] supply maximum program/ erase voltage. bits 0 - 3 BCD 100 mV bits 4 - 7 hex volts	1Eh	- -95	9.5V
1Fh	1	"n" such that typical single word program timeout = 2^n µs.	1Fh	- -09	512µs
20h	1	"n" such that typical full buffer write timeout = 2^n µs.	20h	- -0A	1024µs
21h	1	"n" such that typical block erase timeout = 2^n ms.	21h	- -0A	1s
22h	1	"n" such that typical full chip erase timeout = 2^n ms.	22h	- -00	NA
23h	1	"n" such that maximum word program timeout = 2^n times typical.	23h	- -01	1024µs
24h	1	"n" such that maximum buffer write timeout = 2^n times typical.	24h	- -02	4096µs
25h	1	"n" such that maximum block erase timeout = 2^n times typical.	25h	- -02	4s
26h	1	"n" such that maximum chip erase timeout = 2^n times typical.	26h	- -00	NA

Table 23: Device Geometry

Hex Offset	Length	Description	Address	Hex Code	ASCII Value (DQ[7:0])
27h	1	n such that device size in bytes = 2^n.	27:		See Note 1
28h	2	Flash device interface code assignment: n such that n + 1 specifies the bit field that represents the flash device width capabilities as described here: bit 0: x8 bit 1: x16 bit 2: x32 bit 3: x64 bits 4 - 7: – bits 8 - 15: –	28:	- -01	x16
			29:	- -00	
2Ah	2	n such that maximum number of bytes in write buffer = 2^n.	2Ah	- -0A	1024
			2Bh	- -00	
2Ch	1	Number of erase block regions (x) within the device: 1) x = 0 means no erase blocking; the device erases in bulk. 2) x specifies the number of device regions with one or more contiguous, same-size erase blocks. 3) Symmetrically blocked partitions have one blocking region.	2Ch		See Note 1
2Dh	4	Erase block region 1 information: bits 0 - 15 = y, y + 1 = number of identical-size erase blocks. bits 16 - 31 = z, region erase block(s) size are z x 256 bytes.	2D: 2E: 2F: 30:		See Note 1
31h	4	Erase block region 2 information: bits 0 - 15 = y, y + 1 = number of identical-size erase blocks. bits 16 - 31 = z, region erase block(s) size are z x 256 bytes.	31: 32: 33: 34:		See Note 1
35h	4	Reserved for future erase block region information.	35: 36: 37: 38:		See Note 1

Note: 1. See Block Region Map Information table.

Table 24: Block Region Map Information

Address	256Mb		Address	256Mb	
	Bottom	Top		Bottom	Top
27:	--19	--19	30:	--00	--02
28:	--01	--01	31:	--FE	--03
29:	--00	--00	32:	--00	--00
2A:	--0A	--0A	33:	--00	--80
2B:	--00	--00	34:	--02	--00
2C:	--02	--02	35:	--00	--00

Table 24: Block Region Map Information (Continued)

Address	256Mb		Address	256Mb	
	Bottom	Top		Bottom	Top
2D:	--03	--FE	36:	--00	--00
2E:	--00	--00	37:	--00	--00
2F:	--80	--00	38:	--00	--00

Table 25: Primary Vendor-Specific Extended Query

Hex Offset P = 10Ah	Length	Description	Address	Hex Code	ASCII Value (DQ[7:0])
(P+0)h (P+1)h (P+2)h	3	Primary extended query table, unique ASCII string: PRI	10A:	- -50	P
			10B:	- -52	R
			10C:	- -49	I
(P+3)h	1	Major version number, ASCII	10D:	- -31	1
(P+4)h	1	Minor version number, ASCII	10E:	- -35	5
(P+5)h (P+6)h (P+7)h (P+8)h	4	Optional feature and command support (1 = yes; 0 = no) Bits 11 - 29 are reserved; undefined bits are 0 If bit 31 = 1, then another 31-bit field of optional features follows at the end of the bit 30 field.	10F:	- -E6	–
			110:	- -01	–
			111:	- -00	–
			112:	See Note 1	–
		Bit 0: Chip erase supported.	bit 0 = 0		No
		Bit 1: Suspend erase supported.	bit 1 = 1		Yes
		Bit 2: Suspend program supported.	bit 2 = 1		Yes
		Bit 3: Legacy lock/unlock supported.	bit 3 = 0		No
		Bit 4: Queued erase supported.	bit 4 = 0		No
		Bit 5: Instant individual block locking supported.	bit 5 = 1		Yes
		Bit 6: OTP bits supported.	bit 6 = 1		Yes
		Bit 7: Page mode read supported.	bit 7 = 1		Yes
		Bit 8: Synchronous read supported.	bit 8 = 1		Yes
		Bit 9: Simultaneous operations supported.	bit 9 = 0		No
		Bit 10: Extended Flash array block supported	bit 10 = 0		No
		Bit 11: Permanent block locking of up to full main array supported	bit 11 = 0		No
		Bit 12: Permanent block locking of up to partial main array supported	bit 12 = 0		No
		Bit 30: CFI links to follow:	bit 30 = 0		See Note 1
		Bit 31: Another optional features field to follow.	bit 31 = 0		

Table 25: Primary Vendor-Specific Extended Query (Continued)

Hex Offset P = 10Ah	Length	Description	Address	Hex Code	ASCII Value (DQ[7:0])
(P+9)h	1	Supported functions after SUSPEND: READ ARRAY, STATUS, QUERY. Other supported options include: Bits 1 - 7: Reserved; undefined bits are 0.	113:	- -01	–
		Bit 0: Program supported after ERASE SUSPEND.	bit 0 = 1		Yes
(P+A)h (P+B)h	2	Block Status Register mask: Bits 2 - 15 are reserved; undefined bits are 0.	114:	- -03	–
			115:	- -00	–
		Bit 0: Block lock-bit status register active.	bit 0 = 1		Yes
		Bit 1: Block lock-down bit status active.	bit 1 = 1		Yes
		Bit 4: EFA block lock-bit status register active.	bit 4 = 0		No
		Bit 5: EFA block lock-bit status active.	bit 5 = 0		No
(P+C)h	1	V_{CC} logic supply highest performance program/erase voltage. bits 0 - 3 BCD 100 mV bits 4 - 7 hex value in volts	116:	- -30	3.0V
(P+D)h	1	V_{PP} optimum program/erase voltage. bits 0 - 3 BCD 100mV bits 4 - 7 hex value in volts	117:	- -90	9.0V

Note: 1. See Optional Features Fields table.

Table 26: Optional Features Field

Address	Discrete		512Mb			
	Bottom	Top	Bottom		Top	
	–	–	die 1 (B)	die 2 (T)	die 1 (T)	die 2 (B)
112:	--00	--00	40:	--00	--40	--00

Table 27: One Time Programmable (OTP) Space Information

Hex Offset P = 10Ah	Length	Description	Address	Hex Code	ASCII Value (DQ[7:0])
(P+E)h	1	Number of OTP block fields in JEDEC ID space. 00h indicates that 256 OTP fields are available.	118:	- -02	2

Table 27: One Time Programmable (OTP) Space Information (Continued)

Hex Offset P = 10Ah	Length	Description	Address	Hex Code	ASCII Value (DQ[7:0])
(P+F)h (P+10)h (P+11)h (P+12)h	4	OTP Field 1: OTP Description: This field describes user-available OTP bytes. Some are preprogrammed with device-unique serial numbers. Others are user-programmable. Bits 0-15 point to the OTP Lock byte (the first byte). The following bytes are factory preprogrammed and user-programmable: Bits 0 - 7 = Lock/bytes JEDEC plane physical low address. Bits 8 - 15 = Lock/bytes JEDEC plane physical high address. Bits 16 - 23 = n where 2^n equals factory preprogrammed bytes. Bits 24 - 31 = n where 2^n equals user-programmable bytes.	119: 11A: 1B: 11C:	- -80 - -00 - -03 - -03	80h 00h 8 byte 8 byte
(P+13)h (P+14)h (P+15)h (P+16)h	10	Protection field 2: protection description Bits 0 - 31 point to the protection register physical lock word address in the JEDEC plane. The bytes that follow are factory or user-progammable.	11D: 11E: 11F: 120:	- -89 - -00 - -00 - -00	89h 00h 00h 00h
(P+17)h (P+18)h (P+19)h		Bits 32 - 39 = n where n equals factory programmed groups (low byte). Bits 40 - 47 = n where n equals factory programmed groups (high byte). Bits 48 - 55 = n where 2n equals factory programmed bytes/groups.	121: 122: 123:	- -00 - -00 - -00	0 0 0
(P+1A)h (P+1B)h (P+1C)h		Bits 56 - 63 = n where n equals user programmed groups (low byte). Bits 64 - 71 = n where n equals user programmed groups (high byte). Bits 72 - 79 = n where 2^n equals user programmable bytes/groups.	124: 125: 126:	- -10 - -00 - -04	16 0 16

Table 28: Burst Read Information

Hex Offset P = 10Ah	Length	Description	Address	Hex Code	ASCII Value (DQ[7:0])
(P+1D)h	1	Page Mode Read capability: Bits 7 - 0 = n where 2^n hex value represents the number of read-page bytes. See offset 28h for device word width to determine page-mode data output width. 00h indicates no read page buffer.	127:	- -05	32 byte

Table 28: Burst Read Information (Continued)

Hex Offset P = 10Ah	Length	Description	Address	Hex Code	ASCII Value (DQ[7:0])
(P+1E)h	1	Number of synchronous mode read configuration fields that follow. 00h indicates no burst capability.	128:	- -04	4
(P+1F)h	1	Synchronous mode read capability configuration 1: Bits 3 - 7 = Reserved. Bits 0 - 2 = n where 2^{n+1} hex value represents the maximum number of continuous synchronous reads when the device is configured for its maximum word width. A value of 07h indicates that the device is capable of continuous linear bursts that will output data until the internal burst counter reaches the end of the device's burstable address space. This fields's 3-bit value can be written directly to the Read Configuration Register bits 0 - 2 if the device is configured for its maximum word width. See offset 28h for word width to determine the burst data output width.	129:	- -01	4
(P+20)h	1	Synchronous mode read capability configuration 2.	12A:	- -02	8
(P+21)h	1	Synchronous mode read capability configuration 3.	12B:	- -03	16
(P+22)	1	Synchronous mode read capability configuration 4.	12C:	- -07	Continued

Table 29: Partition and Block Erase Region Information

Hex Offset P = 10Ah		Description Optional Flash features and commands	Length	Address	
Bottom	Top			Bottom	Top
(P+23)h	(P+23)h	Number of device hardware-partition regions within the device: x = 0: a single hardware partition device (no fields follow). x specifies the number of device partition regions containing one or more contiguous erase block regions	1	12D:	12D:

Table 30: Partition Region 1 Information: Top and Bottom Offset/Address

Hex Offset P = 10Ah		Description	Length	Address	
Bottom	Top	Optional Flash features and commands		Bottom	Top
(P+24)h (P+25)h	(P+24)h (P+25)h	Data size of this Partition Region information field (number of addressable locations, including this field.	2	12E: 12F:	12E: 12F:
(P+26)h (P+27)h	(P+26)h (P+27)h	Number of identical partitions within the partition region.	2	130: 131:	130: 131:
(P+28)h	(P+28)h	Number of program or erase operations allowed in a partition: Bits 0 - 3 = Number of simultaneous program operations. Bits 4 - 7 = Number of simultaneous erase operations.	1	132:	132:
(P+29)h	(P+29)h	Simultaneous program or erase operations allowed in other partitions while a partition in this region is in program mode: Bits 0 - 3 = Number of simultaneous program operations. Bits 4 - 7 = Number of simultaneous erase operations.	1	133:	133:
(P+2A)h	(P+2A)h	Simultaneous program or erase operations allowed in other partitions while a partition in this region is in erase mode: Bits 0 - 3 = Number of simultaneous program operations. Bits 4 - 7 = Number of simultaneous erase operations.	1	134:	134:
(P+2B)h	(P+2B)h	Types of erase block regions in this partition region: x=0: No erase blocking; the partition region erases in bulk. x = Number of erase block regions with contiguous, same-size erase blocks. Symmetrically blocked partitions have one blocking region. Partition size = (Type 1 blocks) x (Type 1 block sizes) + (Type 2 blocks) x (Type 2 block sizes) +...+ (Type n blocks) x (Type n block sizes).	1	135:	135:

Table 31: Partition Region 1 Information

Hex Offset P = 10Ah Bottom/Top	Description Optional Flash features and commands	Length	Address Bottom/Top
(P+2C)h (P+2D)h (P+2E)h (P+2F)h	Partition region 1 erase block type 1 information: Bits 0-15 = y, y+1 = Number of identical-sized erase blocks in a partition. Bits 16-31 = z, where region erase block(s) size is z x 256 bytes.	4	136: 137: 138: 139:

Table 31: Partition Region 1 Information (Continued)

Hex Offset P = 10Ah Bottom/Top	Description Optional Flash features and commands	Length	Address Bottom/Top
(P+30)h (P+31)h	Partition 1 (erase block type 1): Minimum block erase cycles x 1000	2	13A: 13B:
(P+32)h	Partition 1 (erase block type 1) bits per cell; internal ECC: Bits 0 - 3 = bits per cell in erase region Bit 4 = reserved for "internal ECC used" (1=yes, 0=no) Bit 5 - 7 = reserved for future use	1	13C:
(P+33)h	Partition 1 (erase block type 1) page mode and synchronous mode capabilities: Bits 0 = page-mode host reads permitted (1=yes, 0=no) Bit 1 = synchronous host reads permitted (1=yes, 0=no) Bit 2 = synchronous host writes permitted (1=yes, 0=no) Bit 3 - 7 = reserved for future use	1	13D:
(P+34)h (P+35)h (P+36)h (P+37)h (P+38)h (P+39)h	Partition 1 (erase block type 1) programming region information: Bits 0 - 7 = x, 2^x: programming region aligned size (bytes) Bit 8-14 = reserved for future use Bit 15 = legacy flash operation; ignore 0:7 Bit 16 - 23 = y: control mode valid size (bytes) Bit 24 - 31 = reserved for future use Bit 32 - 39 = z: control mode invalid size (bytes) Bit 40 - 46 = reserved for future use Bit 47 = legacy flash operation (ignore 23:16 and 39:32)	6	13E: 13F: 140: 141: 142: 143:
(P+3A)h (P+3B)h (P+3C)h (P+3D)h	Partition 1 erase block type 2 information: Bits 0-15 = y, y+1 = Number of identical-size erase blocks in a partition. Bits 16 - 31 = z, where region erase block(s) size is z x 256 bytes. (bottom parameter device only)	4	144: 145: 146: 147:
(P+3E)h (P+3F)h	Partition 1 (erase block type 2) Minimum block erase cycles x 1000	2	148: 149:
(P+40)h	Partition 1 (erase block type 2) bits per cell, internal EDAC: Bits 0 - 3 = bits per cell in erase region Bit 4 = reserved for "internal ECC used" (1=yes, 0=no) Bits 5 - 7 = reserved for future use	1	14A:
(P+41)h	Partition 1 (erase block type 2) page mode and synchronous mode capabilities: Bit 0 = page-mode host reads permitted (1=yes, 0=no) Bit 1 = synchronous host reads permitted (1=yes, 0=no) Bit 2 = synchronous host writes permitted (1=yes, 0=no) Bits 3-7 = reserved for future use	1	14B:

Table 31: Partition Region 1 Information (Continued)

Hex Offset P = 10Ah Bottom/Top	Description Optional Flash features and commands	Length	Address Bottom/Top
(P+42)h (P+43)h (P+44)h (P+45)h (P+46)h (P+47)h	Partition 1 (erase block type 2) programming region information: Bits 0-7 = x, 2^nx = Programming region aligned size (bytes) Bits 8-14 = reserved for future use Bit 15 = legacy flash operation (ignore 0:7) Bits 16 - 23 = y = Control mode valid size in bytes Bits 24 - 31 = reserved Bits 32 - 39 = z = Control mode invalid size in bytes Bits 40 - 46 = reserved Bit 47 = legacy flash operation (ignore 23:16 and 39:32)	6	14C: 14D: 14E: 14F: 150: 151:

Table 32: Partition Region 1: Partition and Erase Block Map Information

Address	256Mb	
	Bottom	Top
12D:	- -01	- -01
12E:	- -24	- -24
12F:	- -00	- -00
130:	- -01	- -01
131:	- -00	- -00
132:	- -11	- -11
133:	- -00	- -00
134:	- -00	- -00
135:	- -02	- -02
136:	- -03	- -FE
137:	- -00	- -00
138:	- -80	- -00
139:	- -00	- -02
13A:	- -64	- -64
13B:	- -00	- -00
13C:	- -02	- -02
13D:	- -03	- -03
13E:	- -00	- -00
13F:	- -80	- -80
140:	- -00	- -00
141:	- -00	- -00
142:	- -00	- -00
143:	- -80	- -80
144:	- -FE	- -03
145:	- -00	- -00
146:	- -00	- -80
147:	- -02	- -00
148:	- -64	- -64
149:	- -00	- -00
14A:	- -02	- -02
14B:	- -03	- -03
14C:	- -00	- -00
14D:	- -80	- -80
14E:	- -00	- -00
14F:	- -00	- -00
150:	- -00	- -00
151:	- -80	- -80

Table 33: CFI Link Information

Offset P = 10Ah	Length	Description	Address	ASCII Value (DQ[7:0])
		CFI Link field bit definitions:		
(P+48)h	4	Bits 0 - 9 = Address offset (within 32Mbit segment of referenced CFI table)	152:	See Note 1
(P+49)h		Bits 10 - 27 = nth 32Mbit segment of referenced CFI table	153:	
(P+4A)h		Bits 28 - 30 = Memory Type	154:	
(P+4B)h		Bit 31 = Another CFI link field immediately follows	155:	
(P+4C)h	1	CFI Link field quantity subfield definitions: Bits 0 - 3 = Quantity field (n such that n+1 equals quantity) Bit 4 = Table and die relative location Bit 5 = Link field and table relative location Bits 6 - 7 = Reserved	156:	

Note: 1. See Additional CFI Link Field table.

Table 34: Additional CFI Link Field

Address	Discrete		512Mb			
	Bottom	Top	Bottom		Top	
	–	–	die 1 (B)	die 2 (T)	die 1 (T)	die 2 (B)
152:	--FF	--FF	--10	--FF	--10	--FF
153:	--FF	--FF	--20	--FF	--20	--FF
154:	--FF	--FF	--00	--FF	--00	--FF
155:	--FF	--FF	--00	--FF	--00	--FF
156:	--FF	--FF	--10	--FF	--10	--FF

Flowcharts

Figure 13: Word Program Procedure

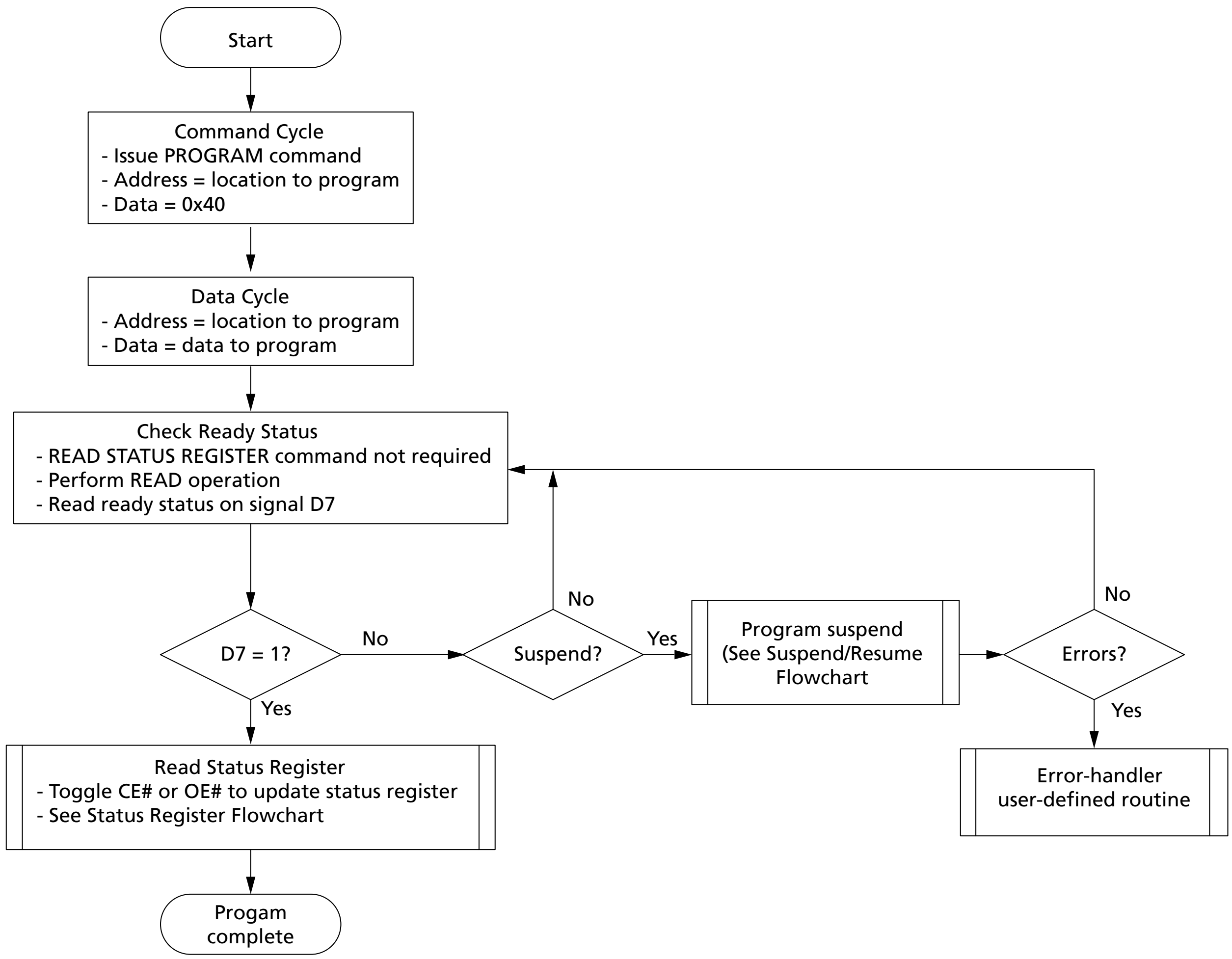
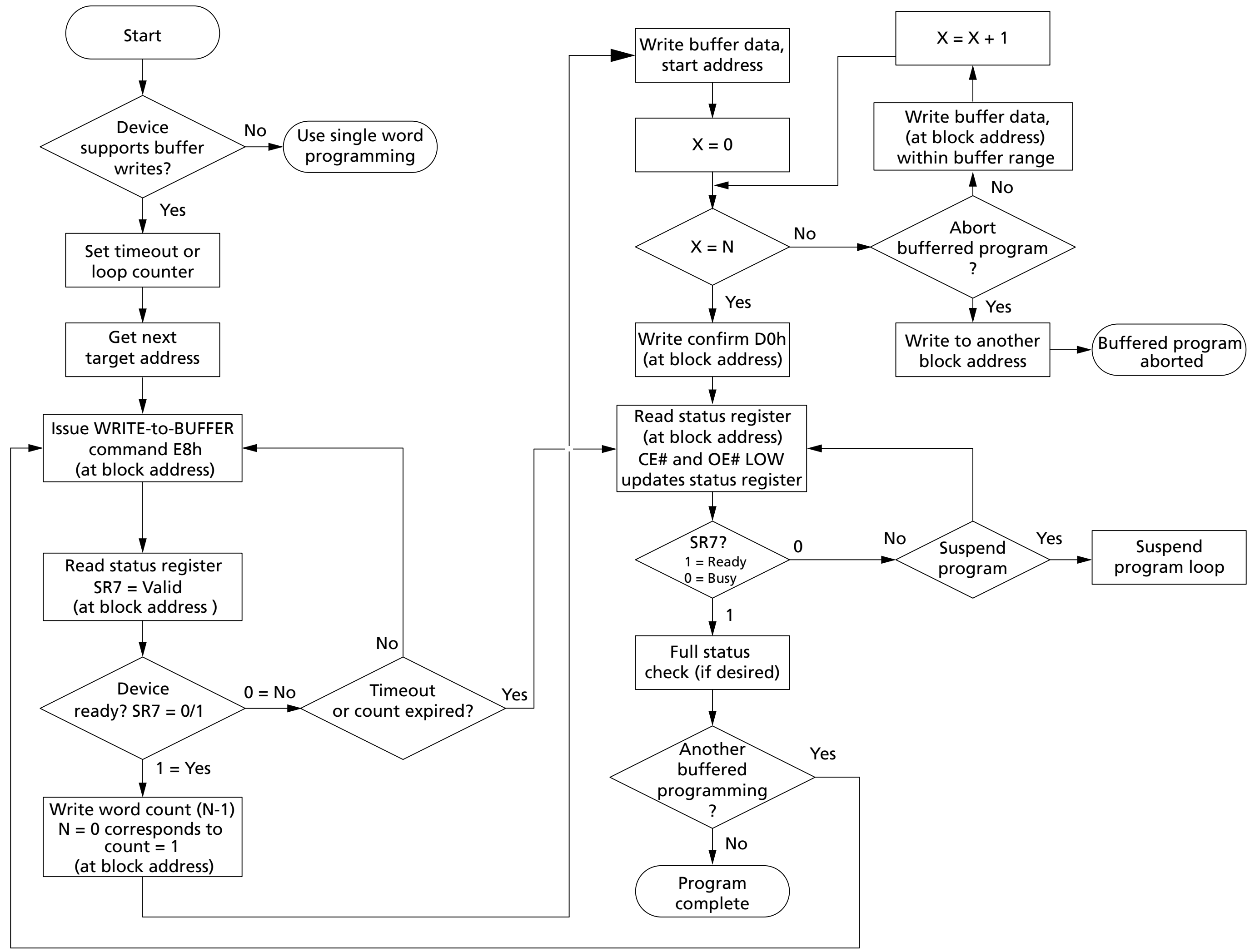


Figure 14: Buffer Program Procedure



Notes:
1. Word count values on DQ0:DQ15 are loaded into the count register. Count ranges for this device are N = 0000h to 01FFh.
2. Device outputs the status register when read.
3. Write buffer contents will be programmed at the device start or destination address.
4. Align the start address on a write buffer boundary for maximum programming performance; that is, A[9:1] of the start address = 0).
5. Device aborts the BUFFERED PROGRAM command if the current address is outside the original block address.
6. Status register indicates an improper command sequence if the BUFFERED PROGRAM command is aborted. Follow this with a CLEAR STATUS REGISTER command.
7. Device defaults to SR output data after BUFFERED PROGRAMMING SETUP command (E8h) is issued . CE# or OE# must be toggled to update the status register . Don't issue the READ SR command (70h); it is interpreted by the device as buffer word count.
8. Full status check can be done after erase and write sequences complete. Write FFh after the last operation to reset the device to read array mode.

Figure 15: Buffered Enhanced Factory Programming (BEFP) Procedure

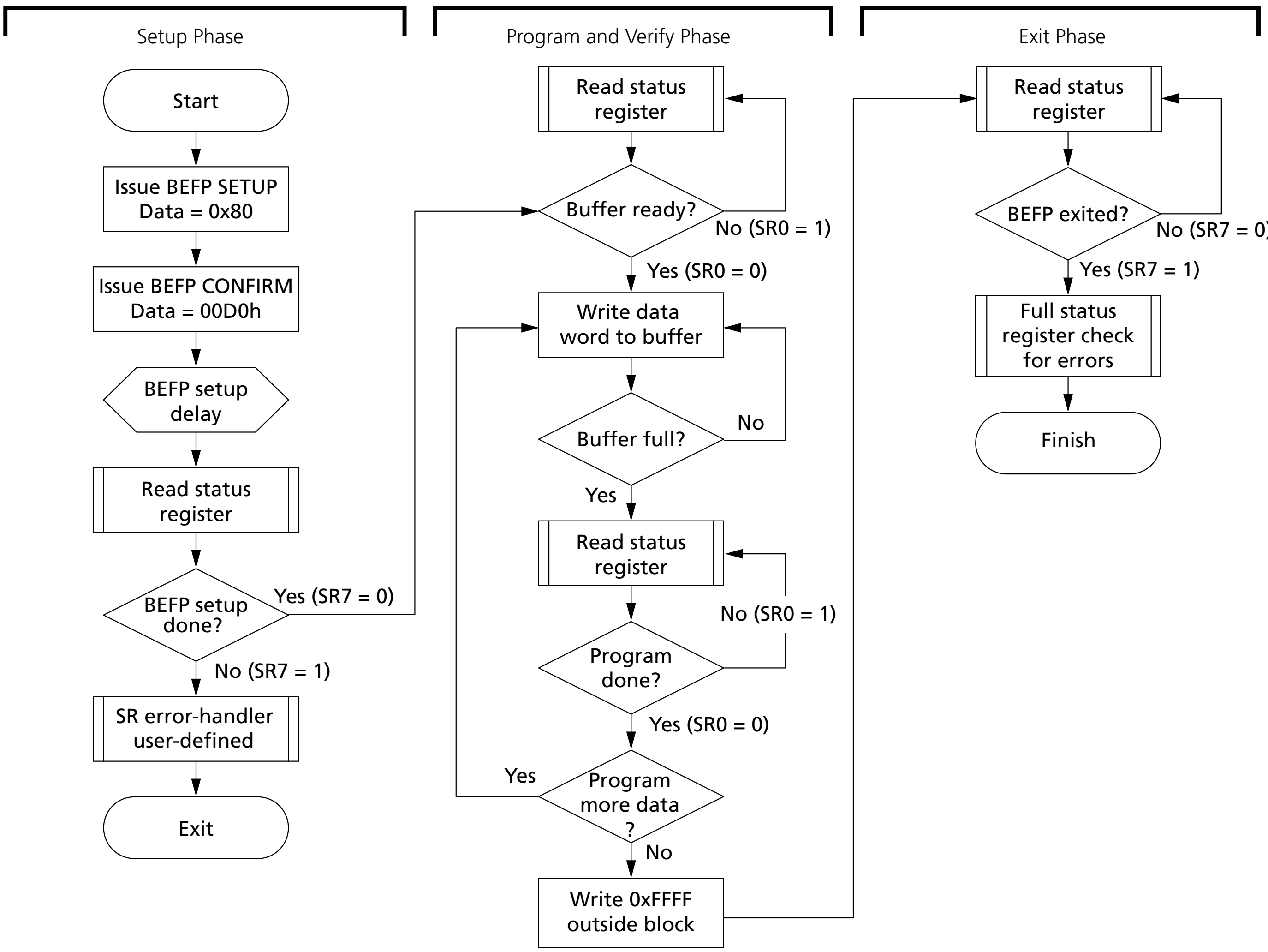


Figure 16: Block Erase Procedure

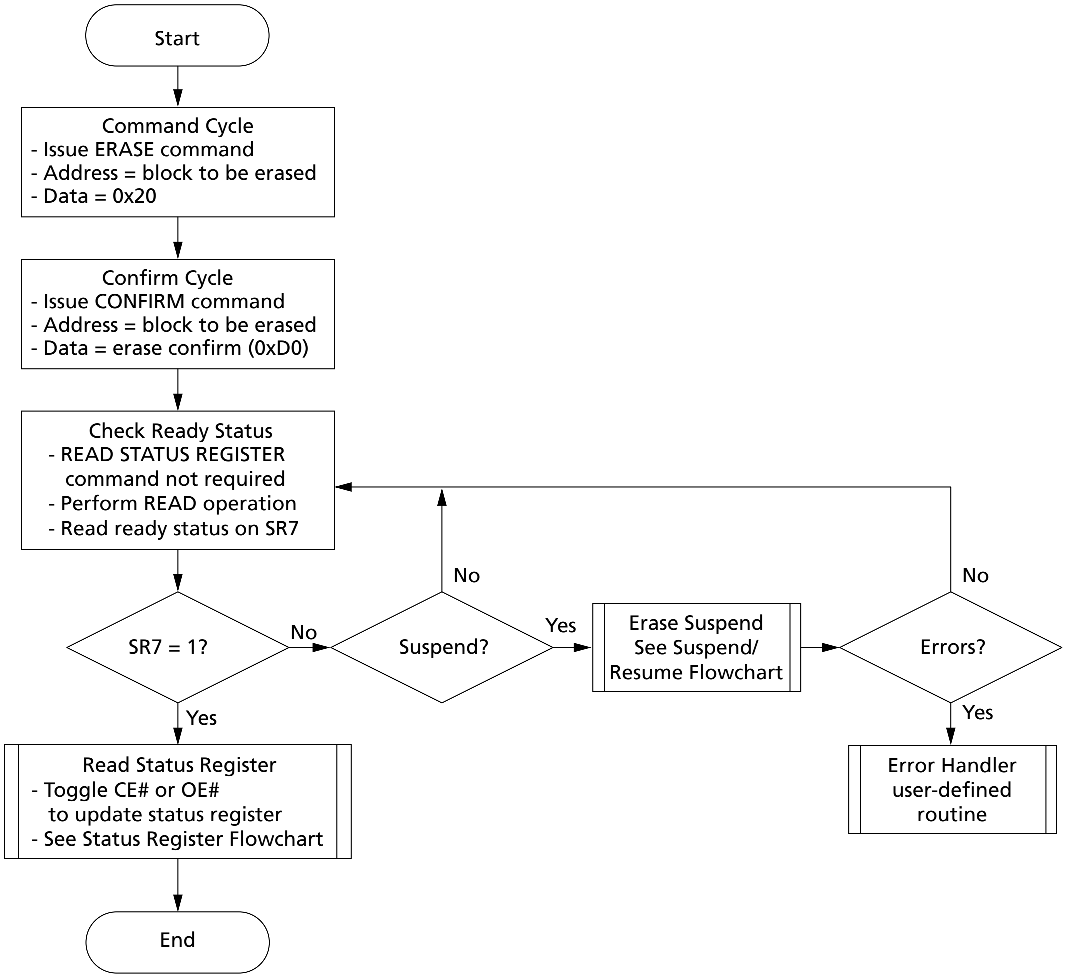


Figure 17: Program Suspend/Resume Procedure

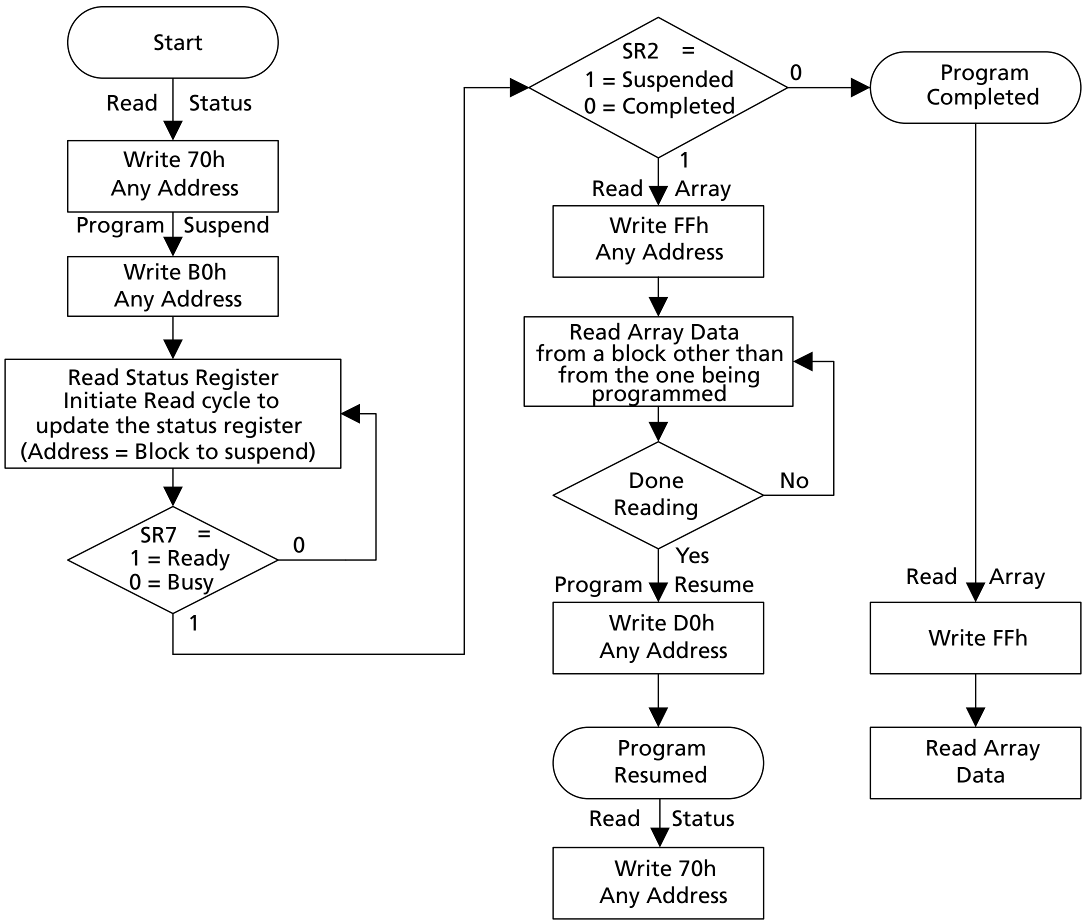
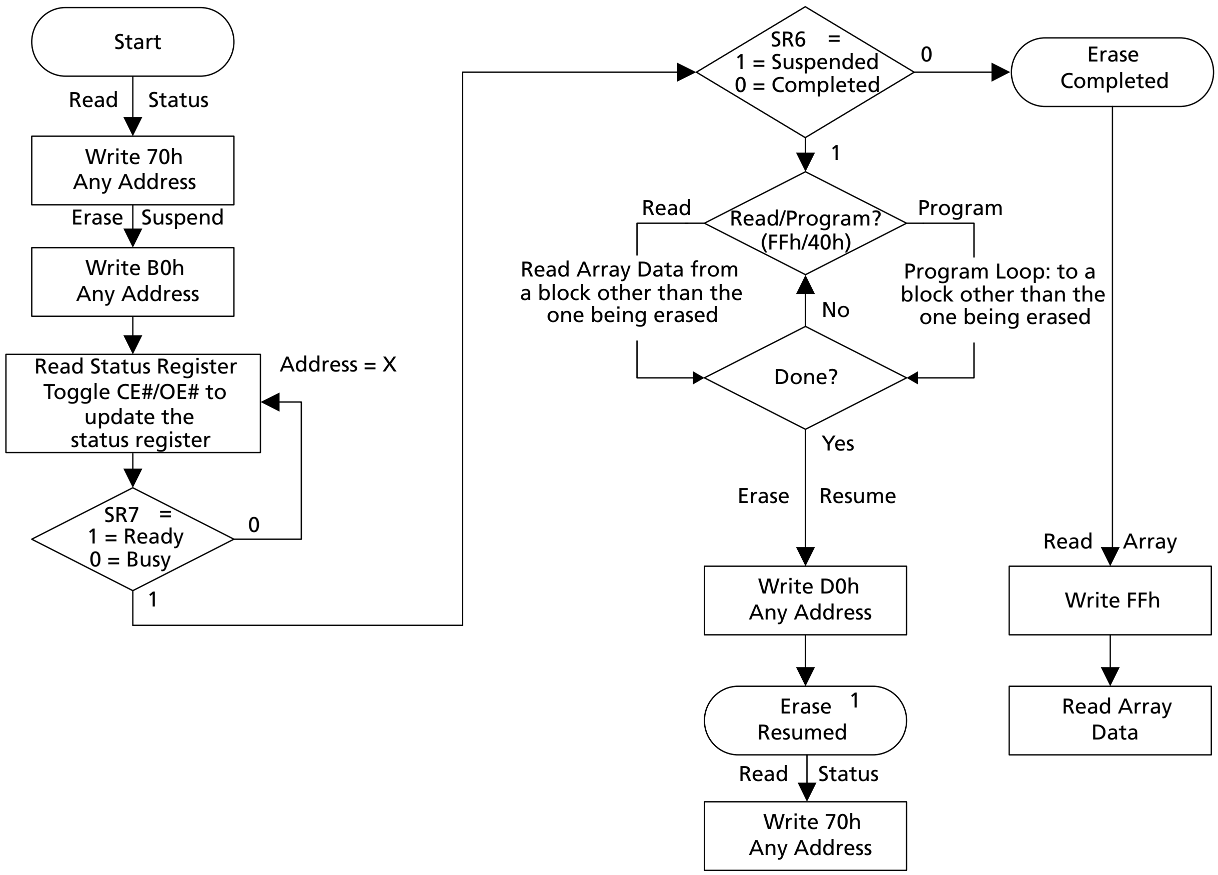


Figure 18: Erase Suspend/Resume Procedure



Note: 1. The tERS/SUSP timing between the initial BLOCK ERASE or ERASE RESUME command and a subsequent ERASE SUSPEND command should be followed.

Figure 19: Block Lock Operations Procedure

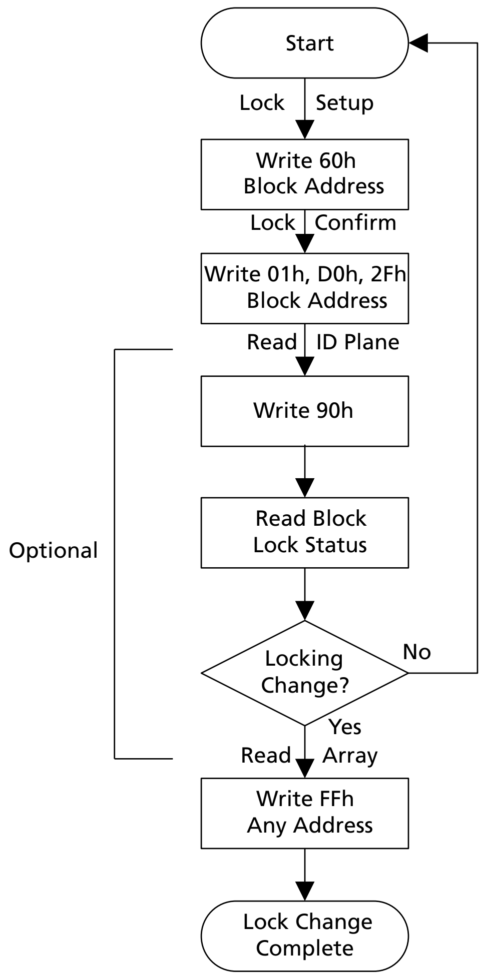


Figure 20: OTP Register Programming Procedure

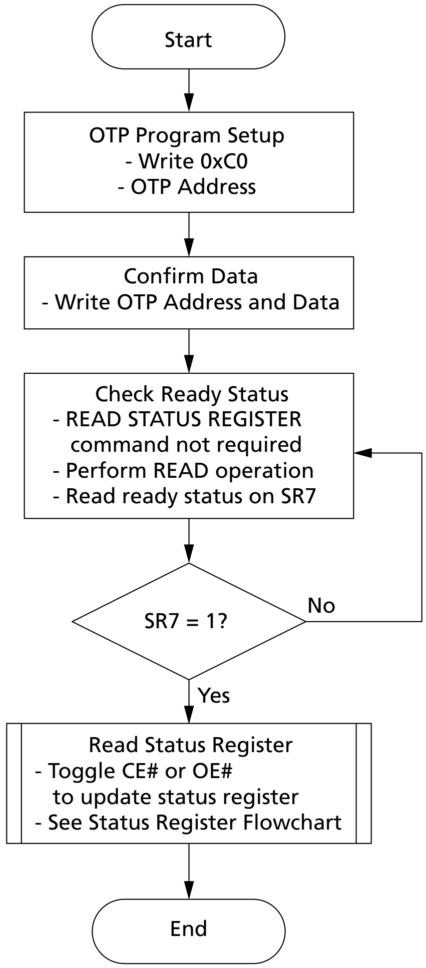
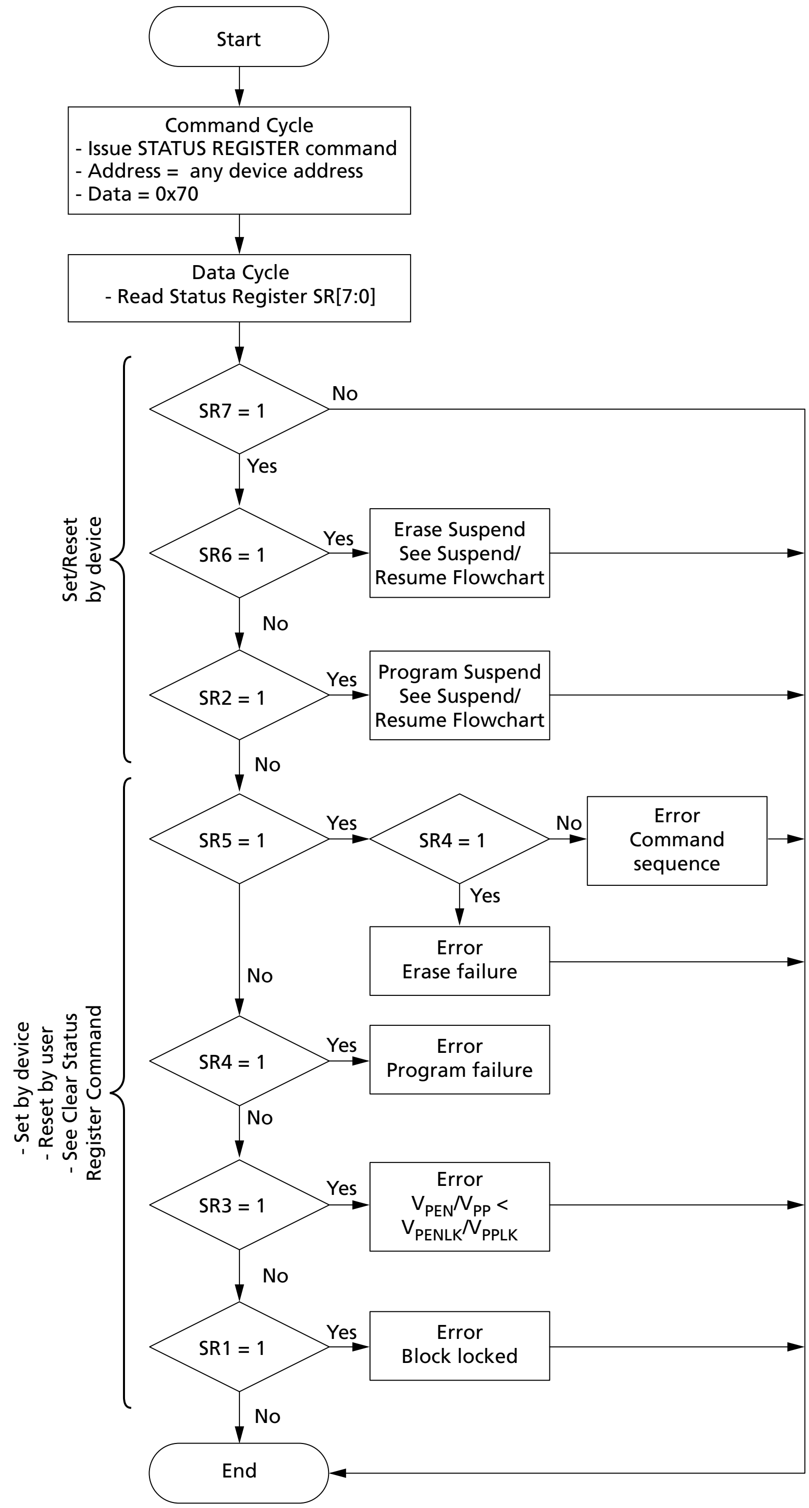


Figure 21: Status Register Procedure



Power and Reset Specifications

V_{CC} should attain V_{CCmin} from V_{SS} simultaneously with or before applying V_{CCQ}, V_{PP} during power up. V_{CC} should attain V_{SS} during power down. Device inputs should not be driven before supply voltage = V_{CCmin}.

Power supply transitions should only occur when RST# is LOW. This protects the device from accidental programming or erasure during power transitions.

Asserting RST# during a system reset is important with automated program/erase devices because systems typically expect to read from the device when coming out of reset. If a CPU reset occurs without a device reset, proper CPU initialization may not occur. This is because the device may be providing status information, instead of array data as expected. Connect RST# to the same active LOW reset signal used for CPU initialization.

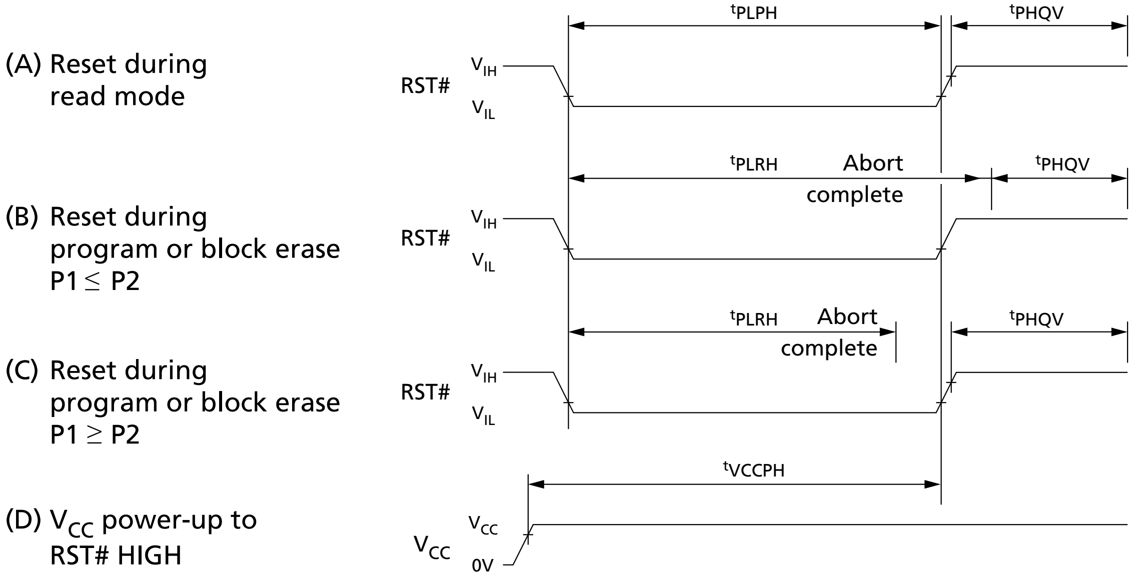
Because the device is disabled when RST# is asserted, it ignores its control inputs during power-up/down. Invalid bus conditions are masked, providing a level of memory protection.

Table 35: Power and Reset

Parameter	Symbol	Min	Max	Unit	Notes
RST# pulse width LOW	^tPLPH	100	–	ns	1, 2, 3, 4
RST# LOW to device reset during erase	^tPLPH	–	25	us	1, 3, 4, 7
RST# LOW to device reset during program		–	25		1, 3, 4, 7
V_{CC} Power valid to RST# de-assertion (HIGH)	^tVCCPH	300	–		1, 4, 5, 6

Notes:
1. These specifications are valid for all device versions (packages and speeds).
2. The device may reset if ^tPLPH is < ^tPLPH MIN, but this is not guaranteed.
3. Not applicable if RST# is tied to V_{CC}.
4. Sampled, but not 100% tested.
5. When RST# is tied to the V_{CC} supply, device will not be ready until ^tVCCPH after $V_{CC} \geq V_{CCMIN}$.
6. When RST# is tied to the V_{CCQ} supply, device will not be ready until ^tVCCPH after $V_{CC} \geq V_{CCMIN}$.
7. Reset completes within ^tPLPH if RST# is asserted while no ERASE or PROGRAM operation is executing.

Figure 22: Reset Operation Waveforms



Power Supply Decoupling

The device requires careful power supply de-coupling. Three basic power supply current considerations are 1) standby current levels, 2) active current levels, and 3) transient peaks produced when CE# and OE# are asserted and de-asserted.

When the device is accessed, internal conditions change. Circuits within the device enable charge pumps, and internal logic states change at high speed. These internal activities produce transient signals. Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and correct de-coupling capacitor selection suppress transient voltage peaks.

Because the devices draw their power from V_{CC}, V_{PP}, and V_{CCQ}, each power connection should have a 0.1µF and a 0.01µF ceramic capacitor to ground. High-frequency, inherently low-inductance capacitors should be placed as close as possible to package leads.

Additionally, for every eight devices used in the system, a 4.7µF electrolytic capacitor should be placed between power and ground close to the devices. The bulk capacitor is meant to overcome voltage droop caused by PCB trace inductance.

Maximum Ratings and Operating Conditions

Stresses greater than those listed can cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated is not guaranteed.

Table 36: Maximum Ratings

Parameter	Maximum Rating	Notes
Temperature under bias	–40°C to + 85 °C	
Storage temperature	–65°C to + 125 °C	
Voltage on any signal (except V_{CC}, V_{PP}, and V_{CCQ})	–2V to +5.6V	1
V_{PP} voltage	–2V to +11.5V	1, 2
V_{CC} voltage	–2V to +5.6V	1
V_{CCQ} voltage	–2V to +5.6V	1
Output short circuit current	100mA	3

Notes:
1. Voltages shown are specified with respect to V_{SS}. During infrequent nonperiodic transitions, the level may undershoot to –2V for periods less than 20ns or overshoot to V_{CC} + 2V or V_{CCQ} + 2V or V_{PP} + 2V for periods less than 20ns.
2. Program/erase voltage is typically 1.7–2V; 9V can be applied for 80 hours maximum total, however, 9V program/erase voltage may reduce block cycling capability.
3. Output is shorted for no more than one second, and more than one output is not shorted at one time.

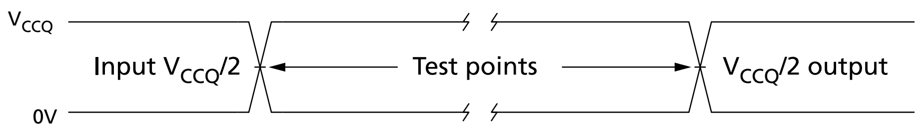
Table 37: Operating Conditions

Symbol	Parameter		Min	Max	Unit	Notes
T_A	Operating temperature		–40	+85	°C	1
V_{CC}	V_{CC} supply voltage		2.3	3.6	V	
V_{CCQ}	I/O supply voltage	CMOS inputs	2.3	3.6		
		TTL inputs	2.4	3.6		
V_{PPL}	V_{PP} voltage supply (logic level)		1.5	3.6		2
V_{PPH}	Buffered enhanced factory programming V_{PP}		8.5	9.5		
^{t}PPH	Maximum V_{PP} hours	$V_{PP} = V_{PPH}$	–	80	Hours	
BLOCK ERASE cycles	Main and parameter blocks	$V_{PP} = V_{PPL}$	100,000	–	Cycles	
	Main blocks	$V_{PP} = V_{PPH}$	–	1000		
	Parameter blocks	$V_{PP} = V_{PPH}$	–	2500		

Notes:
1. T_A = ambient temperature.
2. In typical operation, V_{PP} program voltage is V_{PPL}.

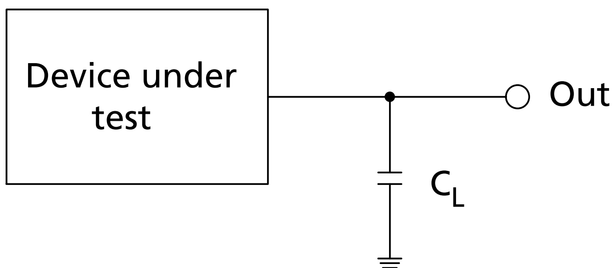
AC Test Conditions and Capacitance

Figure 23: AC Input/Output Reference Timing



Note: 1. AC test inputs are driven at V_{CCQ} for logic 1 and at 0V for logic 0. Input/output timing begins/ends at $V_{CCQ}/2$. Input rise and fall times (10% to 90%) <5ns. Worst-case speed occurs at $V_{CC} = V_{CC}$ (MIN).

Figure 24: Transient Equivalent Load Circuit



Notes: 1. See the Test Configuration for Worst-Case Speed Conditions table for component values.
2. CL includes jig capacitance.

Table 38: Test Configuration: Worst-Case Speed Condition

Test Configuration	C_L (pF)
V_{CCQ}(MIN) standard test	30

Figure 25: Clock Input AC Waveform

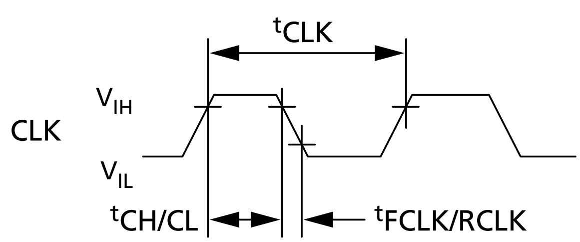


Table 39: Capacitance

Parameter	Signal	Density	Min	Typ	Max	Unit	Condition	Notes
Input Capacitance	Address, Data, CE#, WE#, OE#, RST#, CLK, ADV#, WP#	256Mb	3	7	8	pF	TYP temp = 25°C; MAX temp = 85°C V_{CC} = 0–2.0V, V_{CCQ} = 0– 3.6V Discrete silicon die	1
		256Mb/ 256Mb	6	14	16			
Output Capacitance	Data, WAIT	256Mb	3	5	7			
		256Mb/ 256Mb	6	10	14			

Note: 1. Sampled, but not 100% tested.

DC Electrical Specifications

Table 40: DC Current Characteristics

Parameter		Symbol	CMOS Inputs (V_{CCQ} = 2.3–3.6V)		TTL Inputs (V_{CCQ} = 2.4–3.6V)		Unit	Test Conditions		Notes
			Typ	Max	Typ	Max				
Input load current		I_{LI}	–	±1	–	±2	µA	$V_{CC} = V_{CC}$ (MAX) $V_{CCQ} = V_{CCQ}$ (MAX) $V_{IN} = V_{CCQ}$ or V_{SS}		1, 6
Output leakage current	DQ[15:0], WAIT	I_{LO}	–	±1	–	±10	µA	$V_{CC} = V_{CC}$ (MAX) $V_{CCQ} = V_{CCQ}$ (MAX) $V_{IN} = V_{CCQ}$ or V_{SS}		
V_{CC} standby, Power-down	256Mb	I_{CCS}, I_{CCD}	65	210	65	210	µA	$V_{CC} = V_{CC}$ (MAX) $V_{CCQ} = V_{CCQ}$ (MAX) CE# = V_{CCQ} RST# = V_{CCQ} (for I_{CCS}) RST# = V_{SS} (for I_{CCD}) WP# = V_{IH}		1. 2
	512Mb		130	420	130	420				
Average V_{CC} read current	Asynchronous single-word f = 5 MHz (1 CLK)	I_{CCR}	26	31	26	31	mA	16-word read	$V_{CC} = V_{CC}$ (MAX) CE# = V_{IL} OE# = V_{IH} Inputs: V_{IL} or V_{IH}	1
	Page mode read *f* = 13 MHz (17 CLK)		12	16	12	16	mA	16-word read		
	Synchronous burst *f* = 52 MHz, LC = 4		19	22	19	22	mA	8-word read		
			16	18	16	18	mA	16-word read		
			21	24	21	24	mA	Continuous read		
V_{CC} program current, V_{CC} erase current		I_{CCW}, I_{CCE}	35	50	35	50	mA	$V_{PP} = V_{PPL}$, program/erase in progress		1, 3, 5
			35	50	35	50		$V_{PP} = V_{PPH}$, program/erase in progress		1, 3, 5
V_{CC} program suspend current, V_{CC} erase suspend current	256Mb	I_{CCWS}, I_{CCES}	65	210	65	210	µA	CE# = V_{CCQ}, suspend in progress		1, 3, 4
	512Mb		70	225	70	225				
V_{PP} standby current, V_{PP} program suspend current, V_{PP} erase suspend current		I_{PPS}, I_{PPWS}, I_{PPES}	0.2	5	0.2	5	µA	$V_{PP} = V_{PPL}$, suspend in progress		1, 3, 7
V_{PP} read		I_{PPR}	2	15	2	15	µA	$V_{PP} = V_{PPL}$		1, 3

Table 40: DC Current Characteristics (Continued)

Parameter	Symbol	CMOS Inputs (V_{CCQ} = 2.3–3.6V) Typ	CMOS Inputs Max	TTL Inputs (V_{CCQ} = 2.4–3.6V) Typ	TTL Inputs Max	Unit	Test Conditions	Notes
V_{PP} program current	I_{PPW}	0.05	0.1	0.05	0.1	mA	$V_{PP} = V_{PPL}$, program in progress	3
		0.05	0.1	0.05	0.1		$V_{PP} = V_{PPH}$, program in progress	
V_{PP} erase current	I_{PPE}	0.05	0.1	0.05	0.1	mA	$V_{PP} = V_{PPL}$, erase in progress	3
		0.05	0.1	0.05	0.1		$V_{PP} = V_{PPH}$, erase in progress	
V_{PP} blank check	I_{PPBC}	0.05	0.1	0.05	0.1	mA	$V_{PP} = V_{PPL}$	3
		0.05	0.1	0.05	0.1		$V_{PP} = V_{PPH}$	

Notes:
1. All currents are RMS unless noted. Typical values at TYP V_{CC}, T_C = +25°C.
2. I_{CCS} is the average current measured over any 5ms time interval 5μs after CE# is de-asserted.
3. Sampled, not 100% tested.
4. I_{CCES} is specified with the device deselected. If device is read while in erase suspend, current is I_{CCES} plus I_{CCR}.
5. I_{CCW}, I_{CCE} measured over TYP or MAX times specified in Program and Erase Characteristics (page 90).
6. if $V_{IN} > V_{CC}$, the input load current increases to 10μA MAX.
7. the I_{PPS}, I_{PPWS}, I_{PPES} will increase to 200μA when V_{PP}/WP# is at V_{PPH}.

Table 41: DC Voltage Characteristics

Parameter	Symbol	CMOS Inputs (V_{CCQ} = 2.3–3.6V) Min	CMOS Inputs Max	TTL Inputs[1] (V_{CCQ} = 2.4–3.6V) Min	TTL Inputs Max	Unit	Test Conditions	Notes
Input low voltage	V_{IL}	–0.5	0.4	–0.5	0.6	V		2
Input high voltage	V_{IH}	V_{CCQ} - 0.4	V_{CCQ} + 0.5	2	V_{CCQ} + 0.5	V		
Output low voltage	V_{OL}	–	0.2	–	0.2	V	$V_{CC} = V_{CC}$ (MIN) $V_{CCQ} = V_{CCQ}$ (MIN) I_{OL} = 100μA	
Output high voltage	V_{OH}	V_{CCQ} - 0.2	–	V_{CCQ} – 0.2	–	V	$V_{CC} = V_{CC}$ (MIN) $V_{CCQ} = V_{CCQ}$ (MIN) I_{OH} = –100μA	
V_{PP} lock out voltage	V_{PPLK}	–	0.4	–	0.4	V		3
V_{CC} lock voltage	V_{LKO}	1.5	–	1.5	–	V		
V_{CCQ} lock voltage	V_{LKOQ}	0.9	–	0.9	–	V		

Notes:
1. Synchronous read mode is not supported with TTL inputs.
2. V_{IL} can undershoot to –1.0V for durations of 2ns or less and V_{IH} can overshoot to V_{CCQ} + 1.0V for durations of 2ns or less.
3. $V_{PP} \leq V_{PPLK}$ inhibits ERASE and PROGRAM operations. Do not use V_{PPL} and V_{PPH} outside their valid ranges.

AC Read Specifications

Table 42: AC Read Specifications

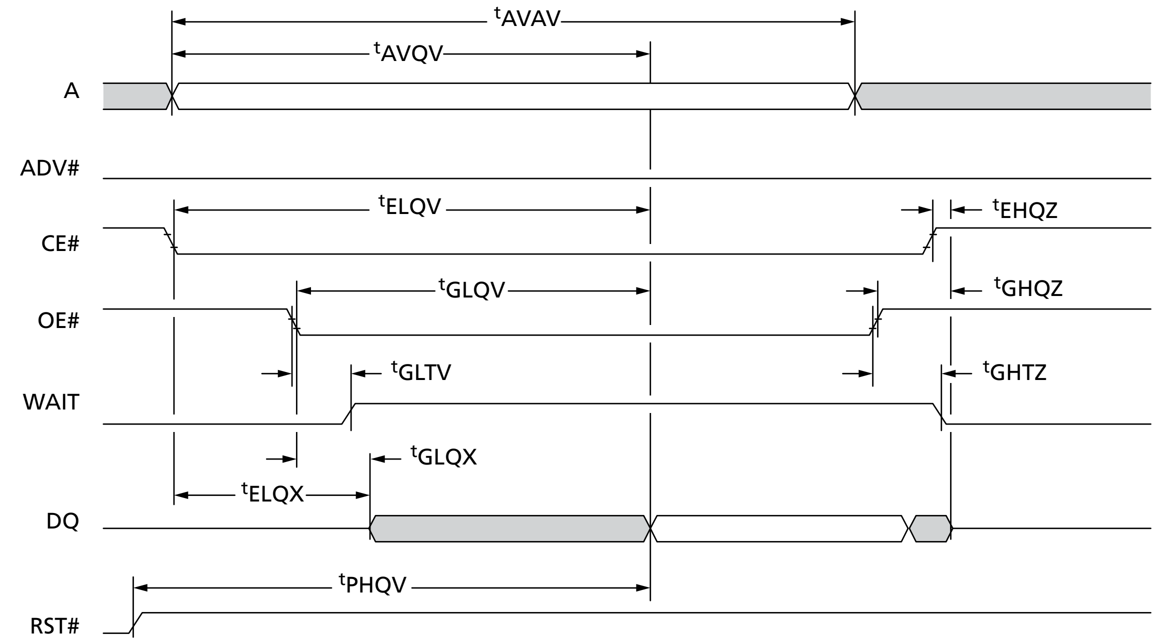
Parameter	Symbol		Min	Max	Unit	Note
Asynchronous Specifications						
READ cycle time	^{t}AVAV	Easy BGA	95	-	ns	-
		TSOP	105		ns	-
Address to output valid	^{t}AVQV	Easy BGA	-	95	ns	-
		TSOP		105	ns	-
CE# LOW to output valid	^{t}ELQV	Easy BGA	-	95	ns	-
		TSOP		105	ns	-
OE# LOW to output valid	^{t}GLQV		-	25	ns	1
RST# HIGH to output valid	^{t}PHQV		-	150	ns	
CE# LOW to output in Low-Z	^{t}ELQX		0	-	ns	2
OE# LOW to output in Low-Z	^{t}GLQX		0	-	ns	1, 2
CE# HIGH to output in High-Z	^{t}EHQZ		-	20	ns	2
OE# HIGH to output in High-Z	^{t}GHQZ		-	15	ns	
Output hold from first occurring address, CE#, or OE# change	^{t}OH		0	-	ns	
CE# pulse width HIGH	^{t}EHEL		17	-	ns	
CE# LOW to WAIT valid	^{t}ELTV		-	17	ns	
CE# HIGH to WAIT High-Z	^{t}EHTZ		-	20	ns	2
OE# LOW to WAIT valid	^{t}GLTV		-	17	ns	
OE# LOW to WAIT in Low-Z	^{t}GLTX		0	-	ns	2
OE# HIGH to WAIT in High-Z	^{t}GHTZ		-	20	ns	
Latching Specifications						
Address setup to ADV# HIGH	^{t}AVVH		10	-	ns	
CE# LOW to ADV# HIGH	^{t}ELVH		10	-	ns	
ADV# LOW to output valid	^{t}VLQV	Easy BGA	-	95	ns	
		TSOP	-	105	ns	
ADV# pulse width LOW	^{t}VLVH		10	-	ns	
ADV# pulse width HIGH	^{t}VHVL		10	-	ns	
Address hold from ADV# HIGH	^{t}VHAX		9	-	ns	3
Page address access	^{t}APA		-	25	ns	
RST# HIGH to ADV# HIGH	^{t}PHVH		30	-	ns	
Clock Specifications						

Table 42: AC Read Specifications (Continued)

Parameter	Symbol		Min	Max	Unit	Note
CLK frequency	^{t}CLK	Easy BGA	-	52	MHz	2, 4, 5
		TSOP	-	40	MHz	
CLK period	^{t}CLK	Easy BGA	19.2	-	ns	
		TSOP	25	-	ns	
CLK HIGH/LOW time	^{t}CH/CL	Easy BGA	5	-	ns	
		TSOP	9			
CLK fall/rise time	^{t}FCLK/RCLK		0.3	3	ns	
Synchronous Specifications[5]						
Address setup to CLK	^{t}AVCH/L		9	-	ns	5
ADV# LOW setup to CLK	^{t}VLCH/L		9	-	ns	
CE# LOW setup to CLK	^{t}ELCH/L		9	-	ns	
CLK to output valid	^{t}CHQV / ^{t}CLQV	Easy BGA	-	17	ns	
		TSOP	-	20	ns	5
Output hold from CLK	^{t}CHQX		3	-	ns	5
Address hold from CLK	^{t}CHAX		10	-	ns	3, 5
CLK to WAIT valid	^{t}CHTV	Easy BGA	-	17	ns	5
		TSOP	-	20		
CLK valid to ADV# setup	^{t}CHVL		3	-	ns	
WAIT hold from CLK	^{t}CHTX		3	-	ns	5

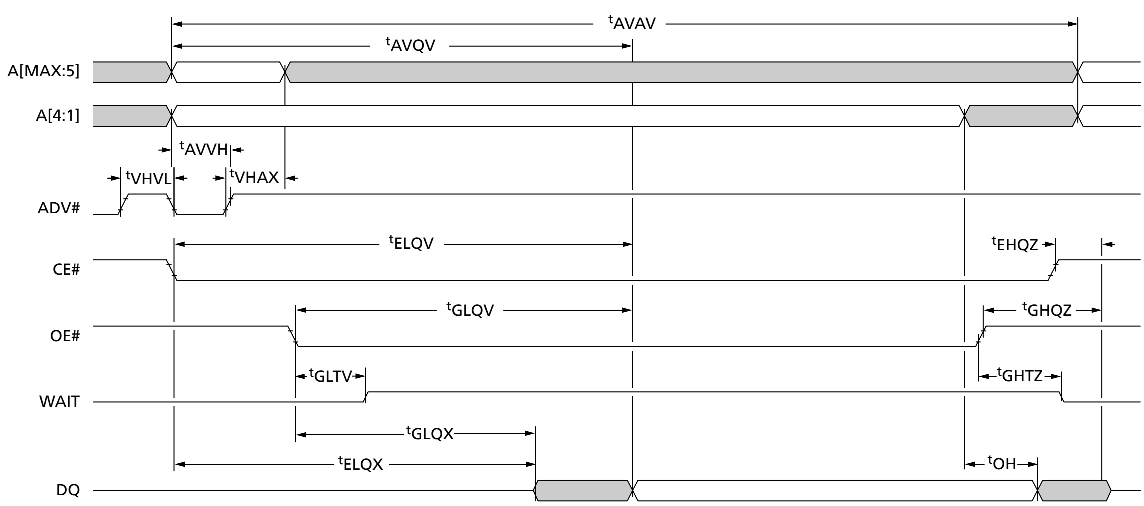
Notes:
1. OE# may be delayed by up to ^{t}ELQV – ^{t}GLQV after CE#'s falling edge without impact to ^{t}ELQV.
2. Sampled, not 100% tested.
3. Address hold in synchronous burst mode is ^{t}CHAX or ^{t}VHAX, whichever timing specification is satisfied first.
4. Synchronous read mode is not supported with TTL level inputs.
5. Applies only to subsequent synchronous reads.

Figure 26: Asynchronous Single-Word Read (ADV# LOW)



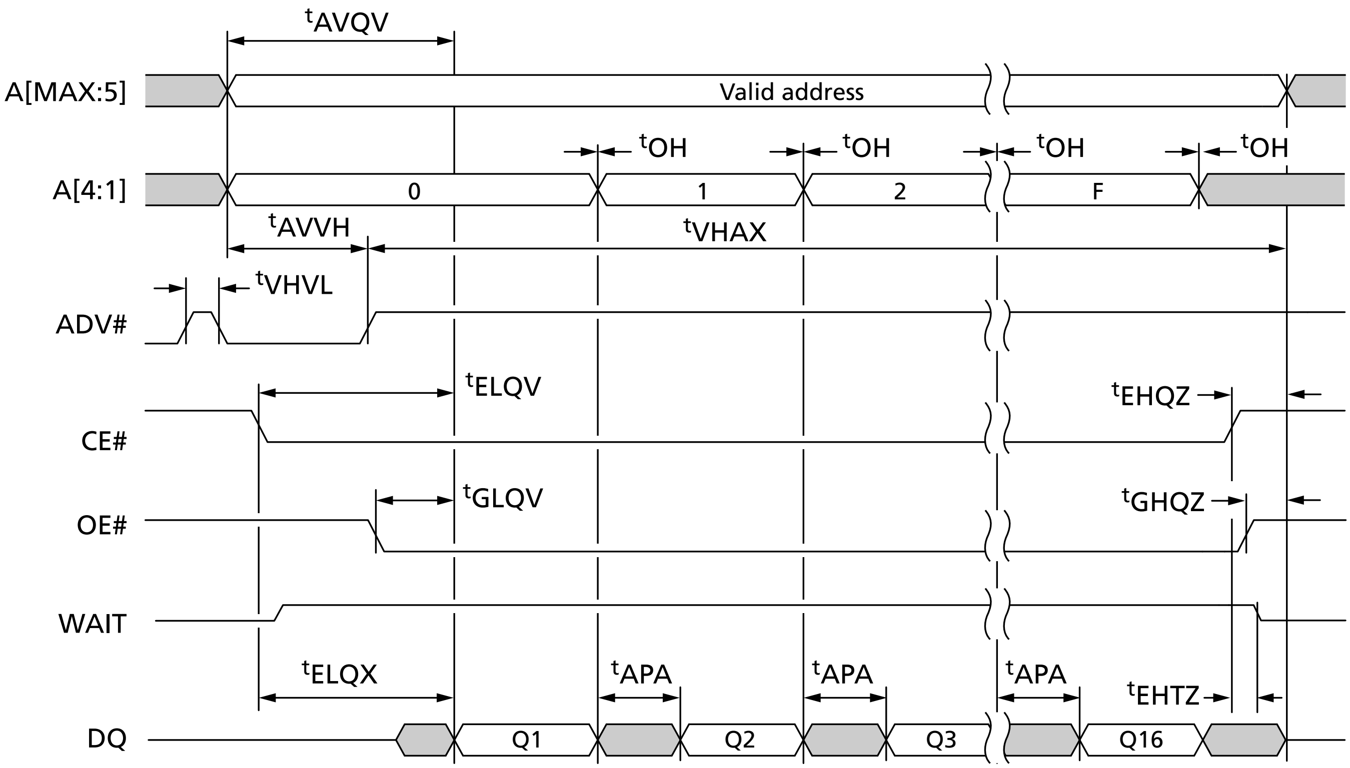
Note: 1. WAIT shown deasserted during asynchronous read mode (RCR10 = 0, WAIT asserted LOW).

Figure 27: Asynchronous Single-Word Read (ADV# Latch)



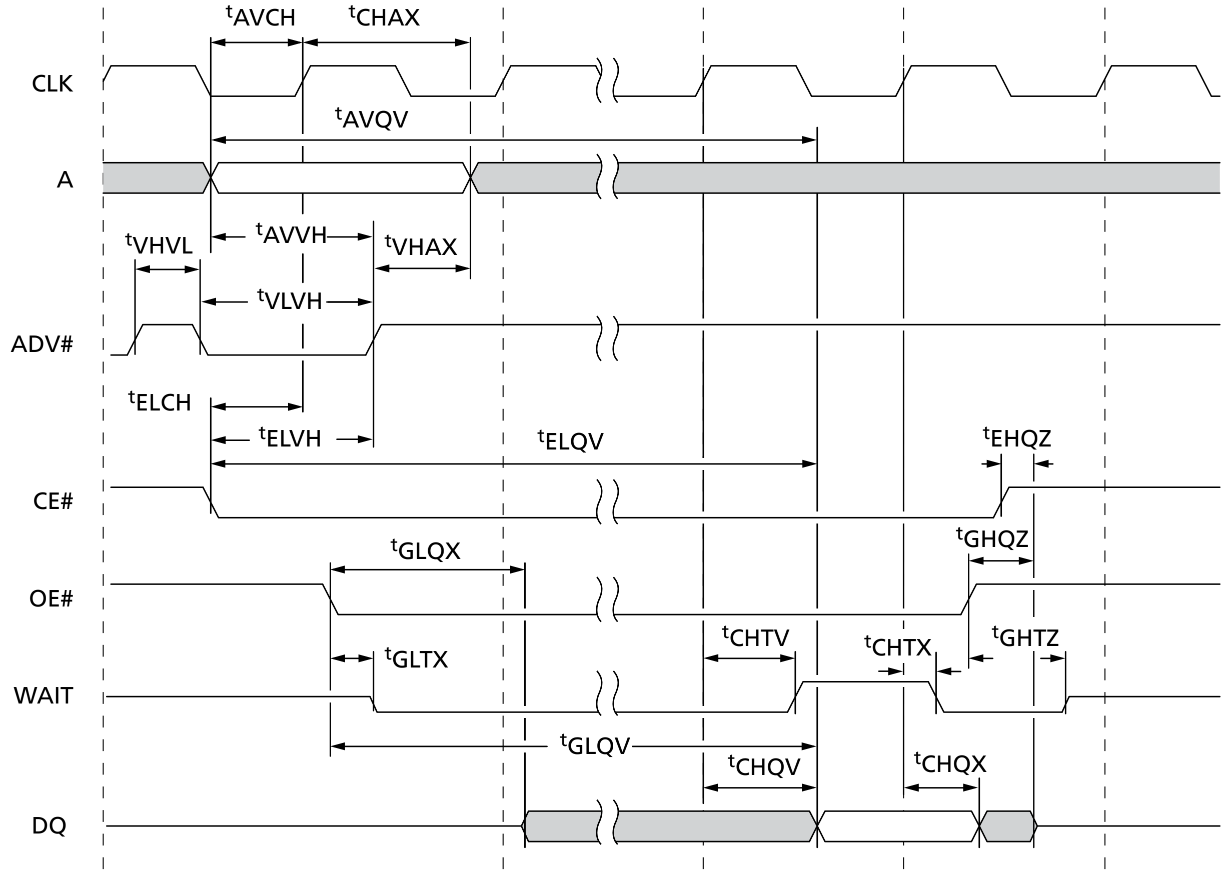
Note: 1. WAIT shown deasserted during asynchronous read mode (RCR10 = 0, WAIT asserted LOW).

Figure 28: Asynchronous Page Mode Read



Note: 1. WAIT shown deasserted during asynchronous read mode (RCR10 = 0, WAIT asserted LOW).

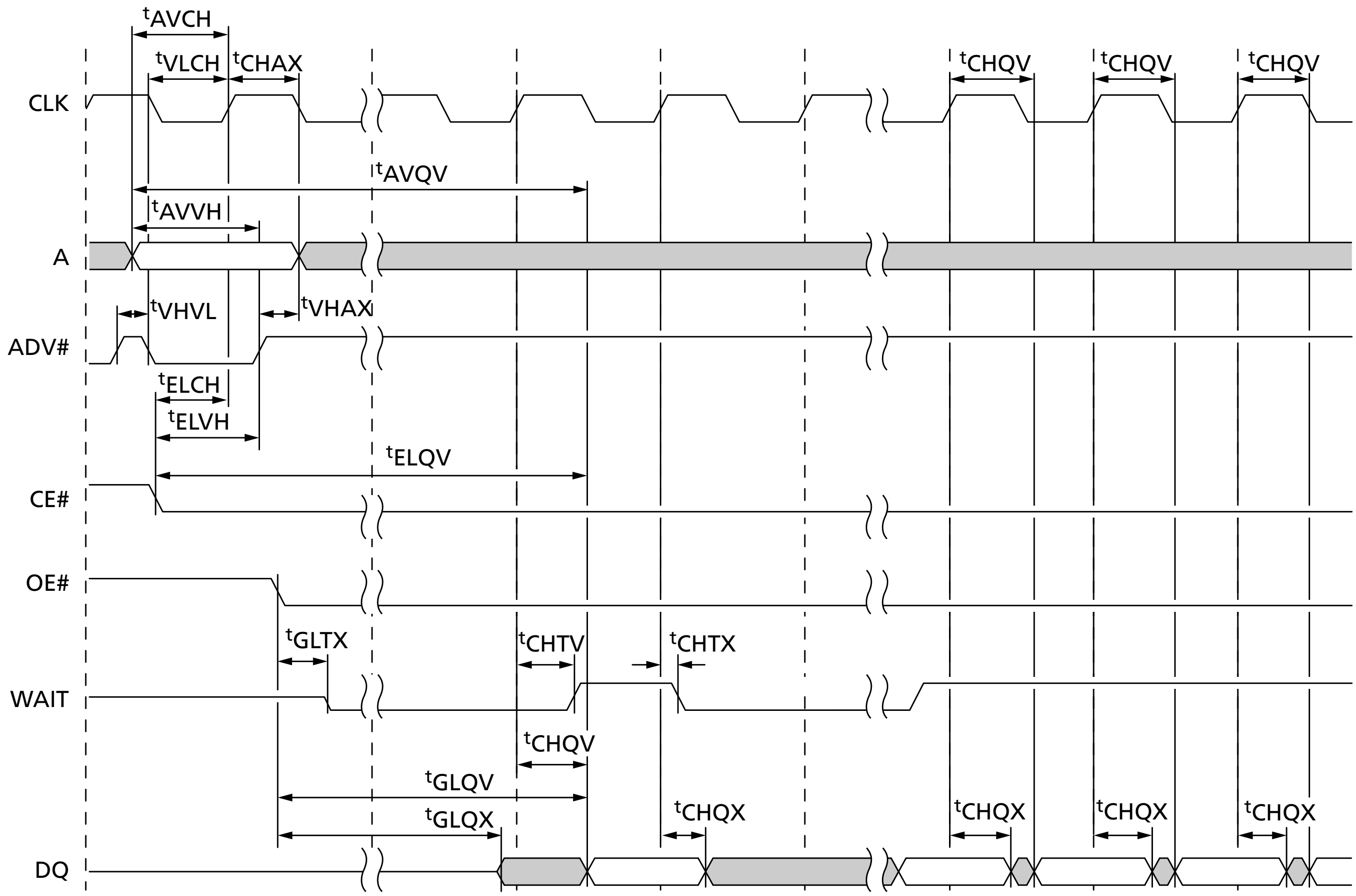
Figure 29: Synchronous Single-Word Array or Nonarray Read



Notes: 1. WAIT is driven per OE# assertion during synchronous array or nonarray read and can be configured to assert either during or one data cycle before valid data.

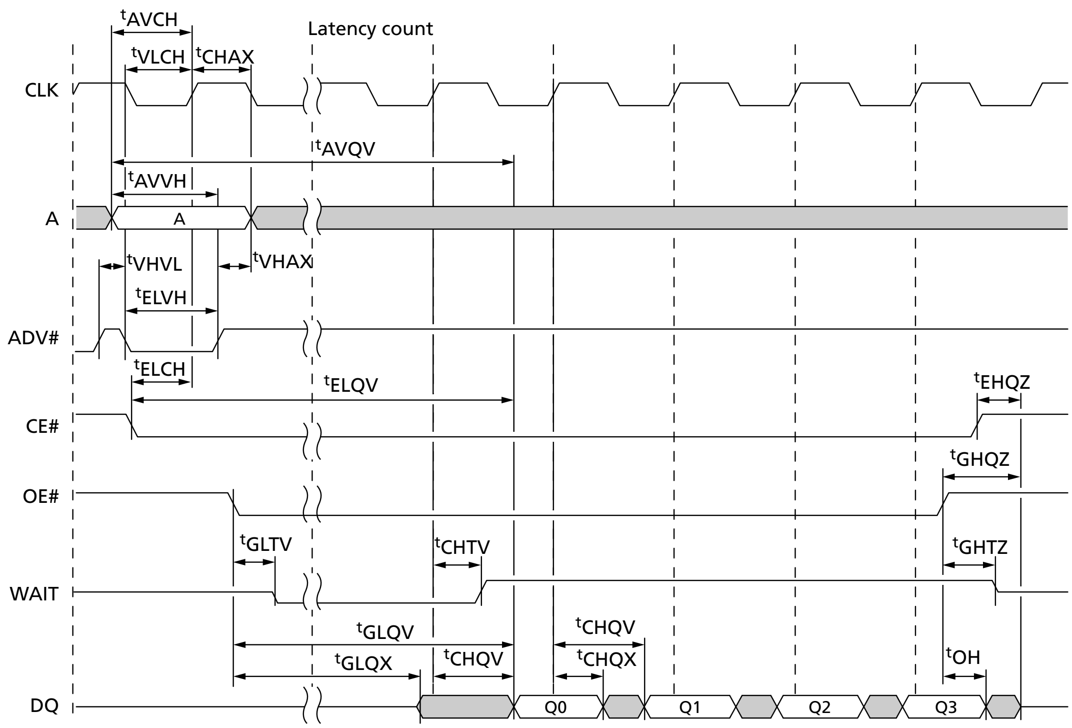
2. In this example, an *n*-word burst is initiated to the flash memory array and is terminated by CE# deassertion after the first word in the burst.

Figure 30: Continuous Burst Read with Output Delay



Notes:
1. WAIT is driven per OE# assertion during synchronous array or nonarray read and can be configured to assert either during or one data cycle before valid data.
2. At the end of a wordline; the delay incurred when a burst access crosses a 16-word boundary and the starting address is not 4-word boundary aligned.

Figure 31: Synchronous Burst Mode 4-Word Read



Note: 1. WAIT is driven per OE# assertion during synchronous array or nonarray read. WAIT asserted during initial latency and deasserted during valid data (RCR10 = 0, WAIT asserted LOW).

AC Write Specifications

Table 43: AC Write Specifications

Parameter	Symbol	Min	Max	Unit	Notes
RST# HIGH recovery to WE# LOW	^tPHWL	150	-	ns	1, 2, 3
CE# setup to WE# LOW	^tELWL	0	-	ns	1, 2, 3
WE# write pulse width LOW	^tWLWH	50	-	ns	1, 2, 4
Data setup to WE# HIGH	^tDVWH	50	-	ns	1, 2, 12
Address setup to WE# HIGH	^tAVWH	50	-	ns	1, 2
CE# hold from WE# HIGH	^tWHEH	0	-	ns	
Data hold from WE# HIGH	^tWHDX	0	-	ns	
Address hold from WE# HIGH	^tWHAX	0	-	ns	
WE# pulse width HIGH	^tWHWL	20	-	ns	1, 2, 5
V_{PP} setup to WE# HIGH	^tVPWH	200	-	ns	1, 2, 3, 7
V_{PP} hold from status read	^tQVVL	0	-	ns	
WP# hold from status read	^tQVBL	0	-	ns	1, 2, 3, 7
WP# setup to WE# HIGH	^tBHWH	200	-	ns	
WE# HIGH to OE# LOW	^tWHGL	0	-	ns	1, 2, 9
WE# HIGH to read valid	^tWHQV	t_{AVQV} + 35	-	ns	1, 2, 3, 6, 10
Write to Asynchronous Read Specifications					
WE# HIGH to address valid	^tWHAV	0	-	ns	1, 2, 3, 6, 8
Write to Synchronous Read Specifications					
WE# HIGH to clock valid	$^tWHCH/L$	19	-	ns	1, 2, 3, 6, 10
WE# HIGH to ADV# HIGH	^tWHVH	19	-	ns	
WE# HIGH to ADV# LOW	^tWHVL	7	-	ns	
Write Specification with Clock Active					
ADV# HIGH to WE# LOW	^tVHWL	-	20	ns	1, 2, 3, 11
Clock HIGH to WE# LOW	^tCHWL	-	20	ns	

Notes:
1. Write timing characteristics during erase suspend are the same as WRITE-only operations.
2. A WRITE operation can be terminated with either CE# or WE#.
3. Sampled, not 100% tested.
4. Write pulse width LOW (^tWLWH or ^tELEH) is defined from CE# or WE# LOW (whichever occurs last) to CE# or WE# HIGH (whichever occurs first). Thus, ^tWLWH = ^tELEH = ^tWLEH = ^tELWH.
5. Write pulse width HIGH ^tWHWL or ^tEHEL) is defined from CE# or WE# HIGH whichever occurs first) to CE# or WE# LOW whichever occurs last). Thus, ^tWHWL = ^tEHEL = t_{WHEL} = ^tEHWL).
6. ^tWHVH or $^tWHCH/L$ must be met when transitioning from a WRITE cycle to a synchronous BURST read.
7. V_{PP} and WP# should be at a valid level until erase or program success is determined.
8. This specification is only applicable when transitioning from a WRITE cycle to an asynchronous read. See spec $^tWHCH/L$ and ^tWHVH for synchronous read.

9. When doing a READ STATUS operation following any command that alters the status register, ^{t}WHGL is 20ns.
10. Add 10ns if the WRITE operation results in an RCR or block lock status change, for the subsequent READ operation to reflect this change.
11. These specs are required only when the device is in a synchronous mode and the clock is active during an address setup phase.
12. This specification must be complied with customer's writing timing. The result would be unpredictable if there is any violation to this timing specification.

Figure 32: Write to Write Timing

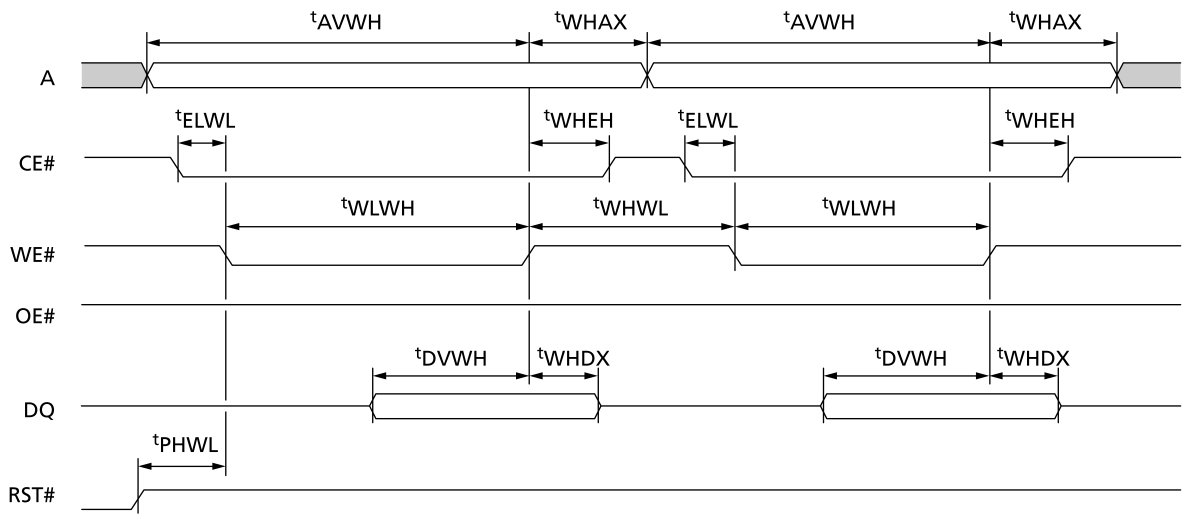
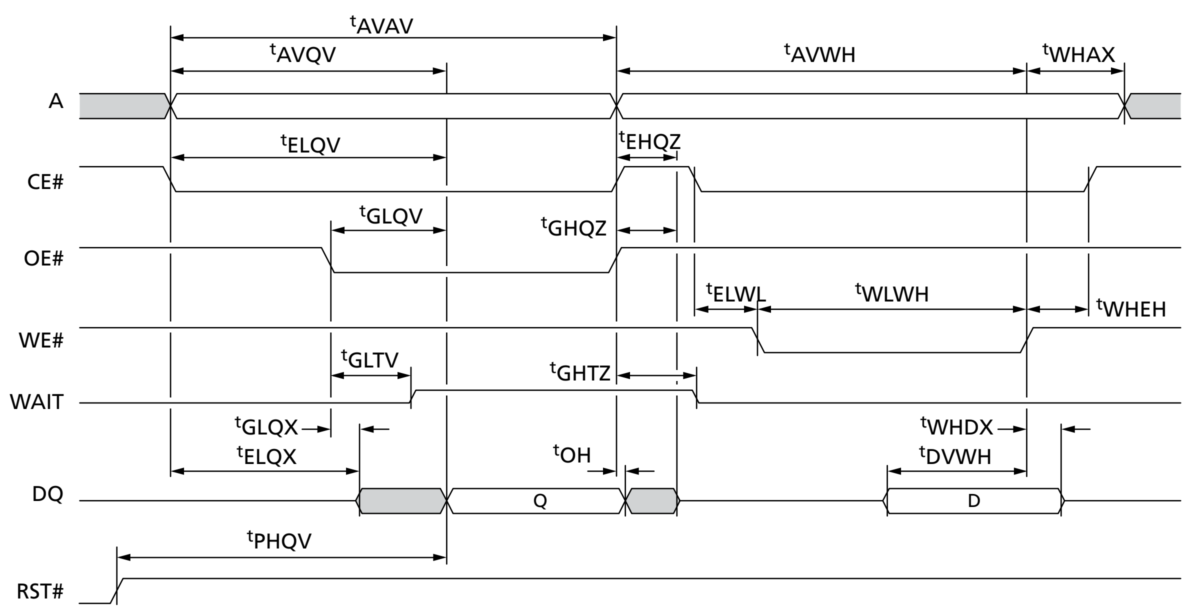


Figure 33: Asynchronous Read to Write Timing



Note: 1. WAIT de-asserted during asynchronous read and during write. WAIT High-Z during write per OE# deasserted.

Figure 34: Write to Asynchronous Read Timing

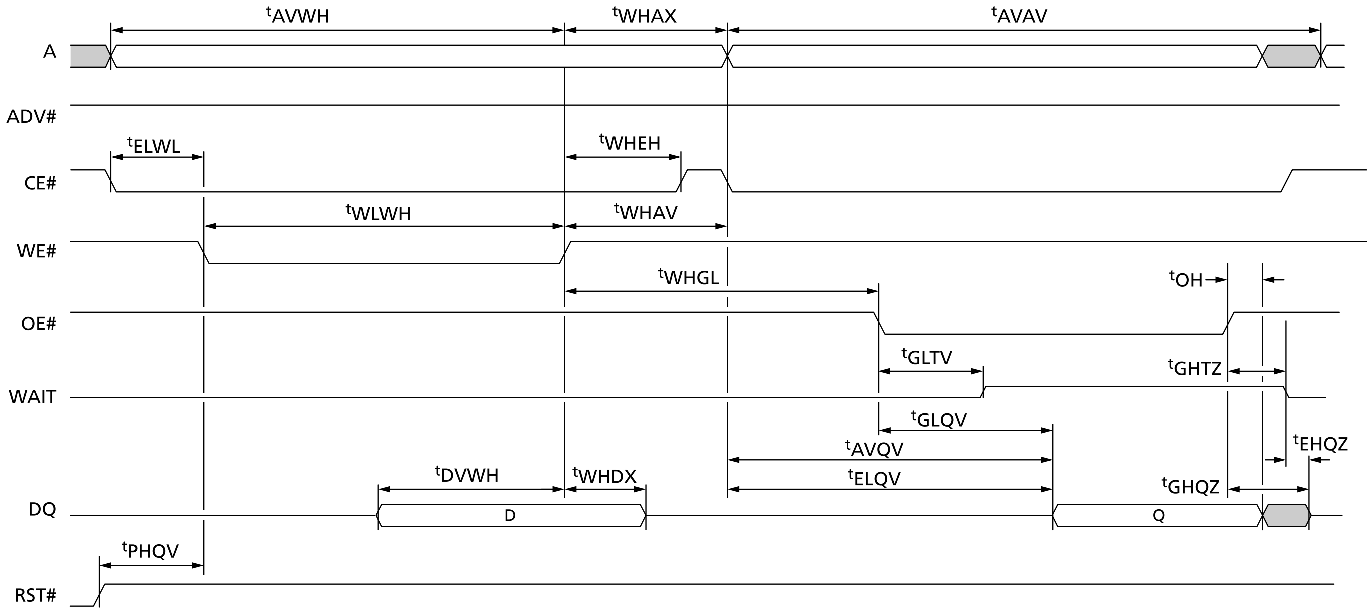
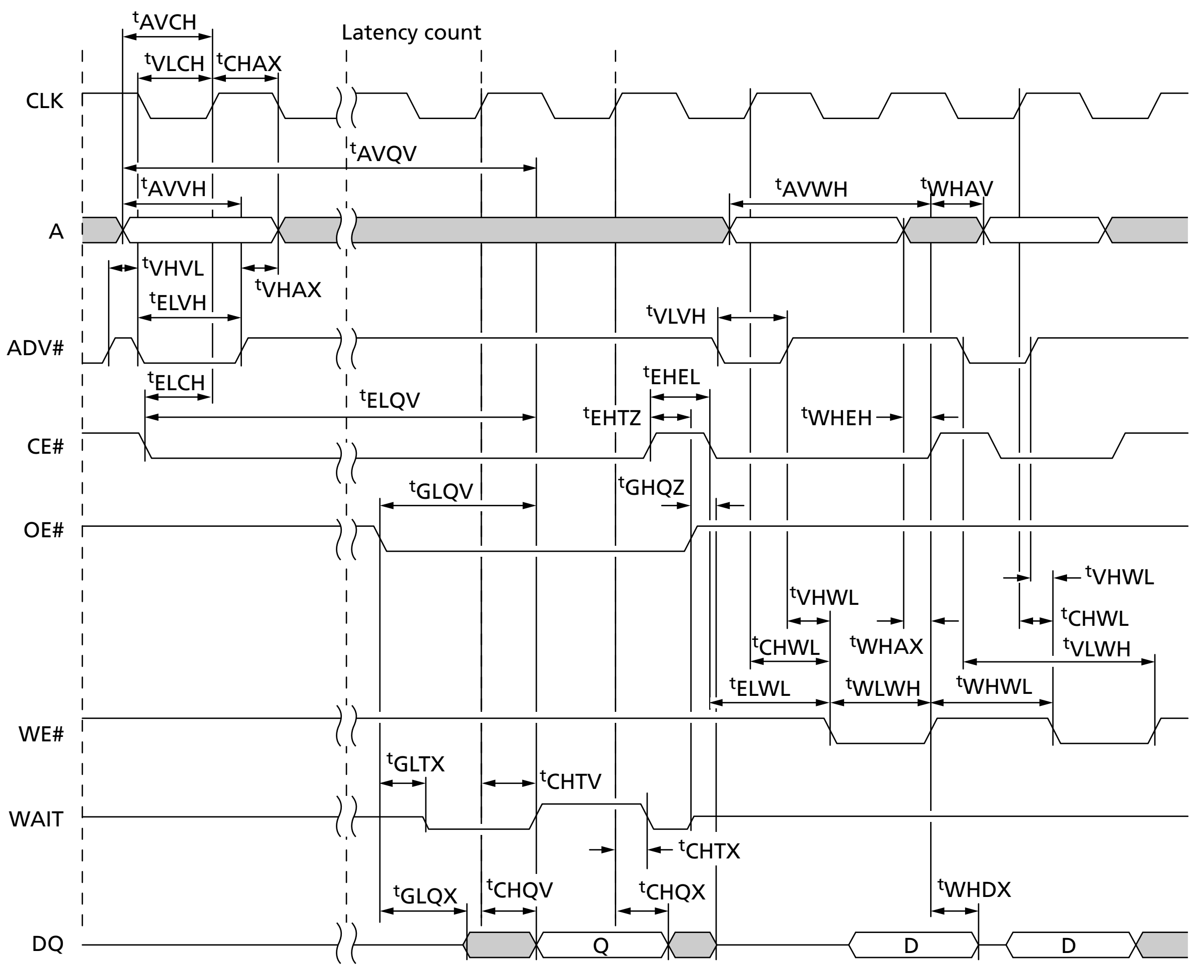
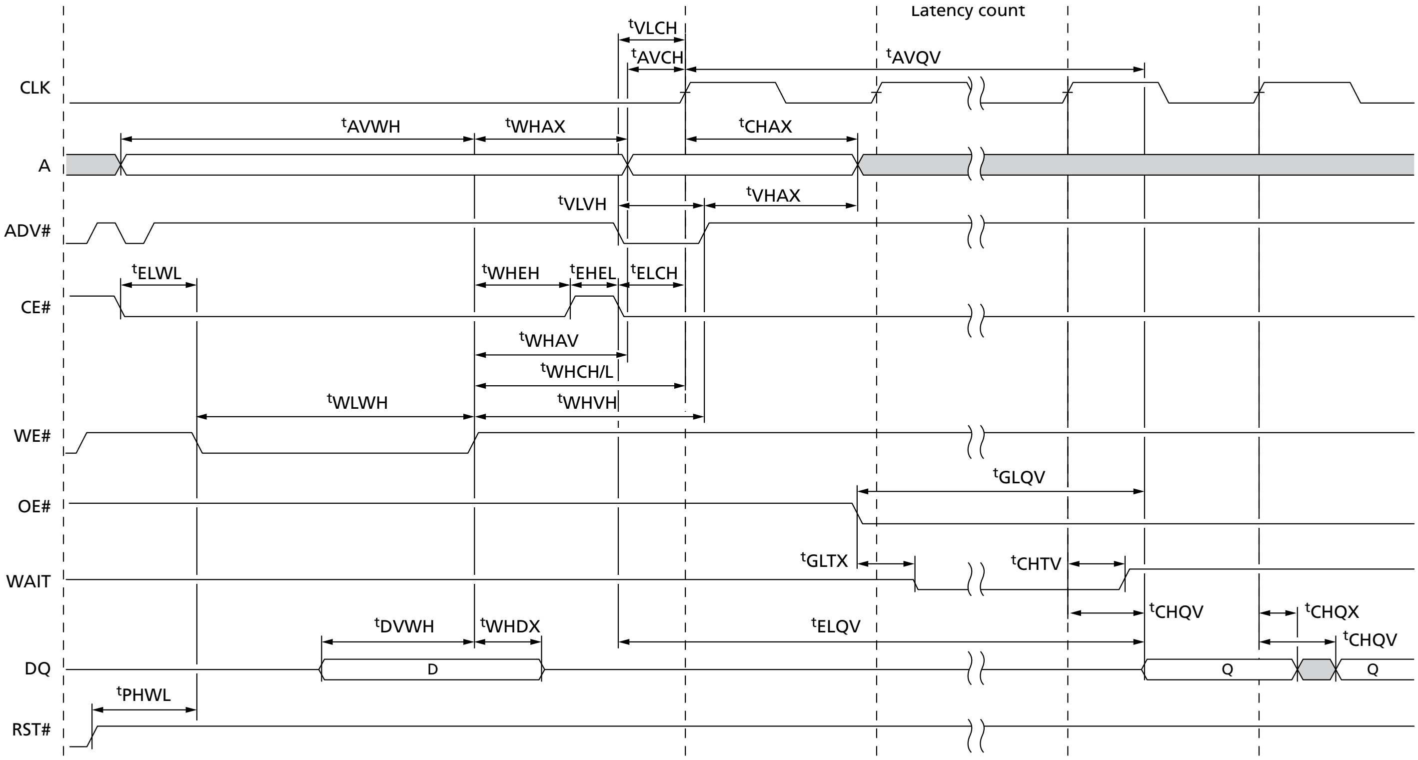


Figure 35: Synchronous Read to Write Timing



Note: 1. WAIT shown de-asserted and High-Z per OE# de-assertion during WRITE operation (RCR10 = 0, WAIT asserted LOW). Clock is ignored during WRITE operation.

Figure 36: Write to Synchronous Read Timing



Note: 1. WAIT shown de-asserted and High-Z per OE# de-assertion during WRITE operation (RCR10 = 0, WAIT asserted LOW).

Program and Erase Characteristics

Table 44: Program and Erase Specifications

Parameter		Symbol	V_{PPL}			V_{PPH}			Unit	Notes
			Min	Typ	Max	Min	Typ	Max		
Conventional Word Programming										
Program time	Single word	tPROG/W	–	270	456	–	270	456	µs	1
Buffered Programming										
Program time	Aligned, BP time (32 words)	tPROG	–	310	716	–	310	716	µs	1
	Aligned, BP time (64 words)		–	310	900	–	310	900		
	Aligned, BP time (128 words)		–	375	1140	–	375	1140		
	Aligned, BP time (256 words)		–	505	1690	–	505	1690		
	One full buffer, BP time (512 words)		–	900	3016	–	900	3016		
Buffered Enhanced Factory Programming										
Program	Single byte	tBEFP/B	N/A	N/A	N/A	–	0.5	–	µs	1, 2
	BEFP Setup	tBEFP/SETUP	N/A	N/A	N/A	5	–	–		1
Erase and Suspend										
Erase time	32KB parameter	tERS/PB	–	0.8	4.0	–	0.8	4.0	s	1
	128KB main	tERS/MB	–	0.8	4.0	–	0.8	4.0		
Suspend latency	Program suspend	tSUSP/P	–	25	30	–	25	30	µs	
	Erase suspend	tSUSP/E	–	25	30	–	25	30		
	Erase-to-suspend	tERS/SUSP	–	500	–	–	500	–		1, 3
Blank Check										
Blank check	Main array block	tBC/MB	–	3.2	–	–	3.2	–	ms	

Notes:
1. Typical values measured at T_C = +25°C and nominal voltages. Performance numbers are valid for all speed versions. Excludes system overhead. Sampled, but not 100% tested.
2. Averaged over entire device.
3. tERS/SUSP is the typical time between an initial BLOCK ERASE or ERASE RESUME command and the a subsequent ERASE SUSPEND command. Violating the specification repeatedly during any particular block erase may cause erase failures.

Revision History

Rev. C – 9/15

- Correct the tCHTX spec.

Rev. B – 12/13

- On cover page, corrected erase suspend (TYP) from 30µs to 25µs.
- Updated part numbers
- Added the following part number disclaimer: "Not all part numbers listed here are available for ordering."
- Revised timings

Rev. A – 8/13

- Initial Micron brand release

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