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MM74HC595 8-Bit Shift Register with Output Latches

Features

- Low Quiescent current: 80µA Maximum (74HC Series)
- Low Input Current: 1µA Maximum
- 8-Bit Serial-In, Parallel-Out Shift Register with Storage
- Wide Operating Voltage Range: 2V–6V
- Cascadable
- Shift Register has Direct Clear
- Guaranteed Shift Frequency: DC to 30MHz

Description

The MM74HC595 high-speed shift register utilizes advanced silicon-gate CMOS technology. This device possesses the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads.

This device contains an eight-bit serial-in, parallel-out, shift register that feeds an eight-bit D-type storage register. The storage register has eight 3-state outputs. Separate clocks are provided for both the shift register and the storage register. The shift register has a direct-overriding clear, serial input, and serial output (standard) pins for cascading. Both the shift register and storage register use positive-edge triggered clocks. If both clocks are connected together, the shift register state is one clock pulse ahead of the storage register.

The 74HC logic family is speed, function, and pin-out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Ordering Information

Part Number	Operating Temperature Range	 Eco Status	Package	Packing Method
MM74HC595M	-40 to +85°C	RoHS	16-Lead, Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Inch Narrow	Tubes
MM74HC595MX	-40 to +85°C	RoHS		Tape and Reel
MM74HC595SJ	-40 to +85°C	RoHS	16-Lead, Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide	Tubes
MM74HC595SJX	-40 to +85°C	RoHS		Tape and Reel
MM74HC595MTC	-40 to +85°C	RoHS	16-Lead, Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide	Tubes
MM74HC595MTCX	-40 to +85°C	RoHS		Tape and Reel
MM74HC595N	-40 to +85°C	RoHS	16-Lead, Plastic Dual In-Line Package (PDIP), JEDEC MS-001, 0.300 Inch Wide	Tubes

 For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Block Diagram

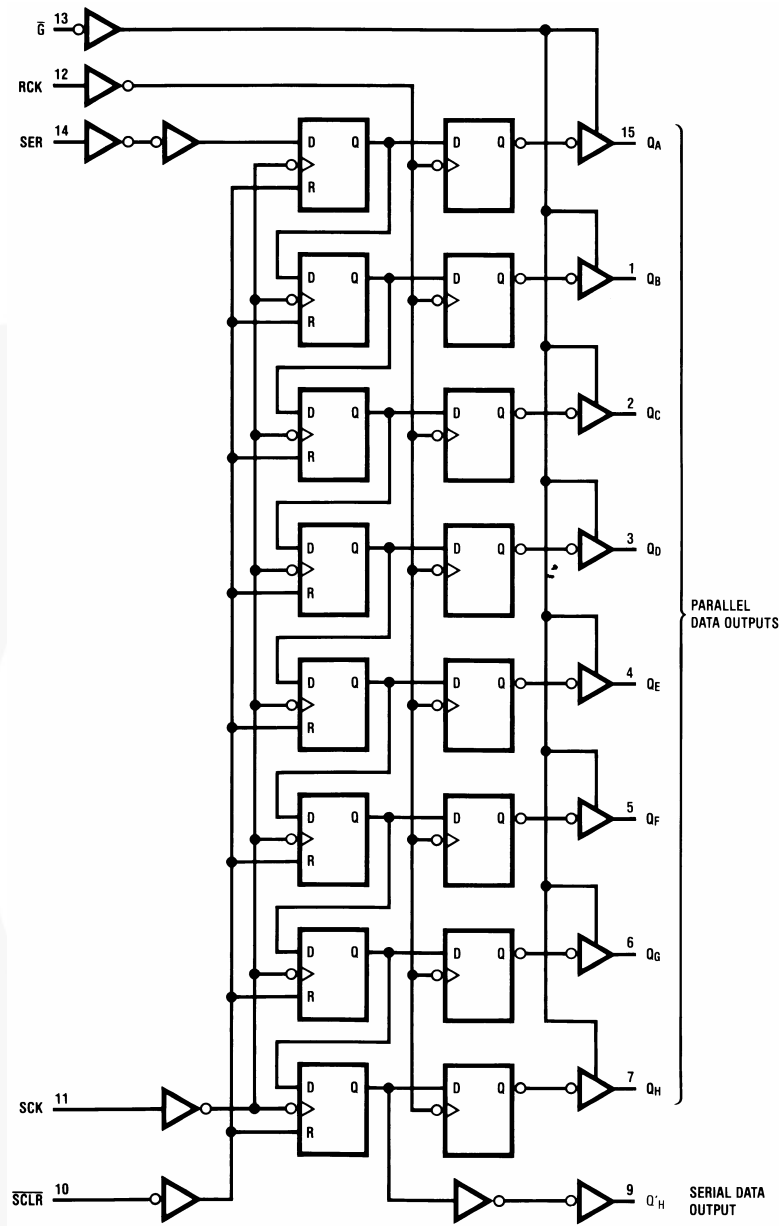


Figure 1. Logic Diagram (Positive Logic)

Pin Configuration



Figure 2. Pin Configuration

Pin Definitions

Pin #	Name	Description
1	Q _B	Output Bit B
2	Q _C	Output Bit C
3	Q _D	Output Bit D
4	Q _E	Output Bit E
5	Q _F	Output Bit F
6	Q _G	Output Bit G
7	Q _H	Output Bit H
8	GND	Ground
9	Q' _H	Serial Data Output
10	SCLR	Shift Register Clear
11	SCK	Shift Register Clock Input
12	RCK	Storage Register Clock Input
13	\overline{G}	Output Enable
14	SER	Serial Data Input
15	QA	Output Bit A
16	V _{CC}	Supply Voltage

Truth Table

RCK	SCK	SCLR	G	Function
X	X	X	H	QA through Q _H = 3-state
X	X	L	L	Shift register clocked; Q' _H = 0
X	↑	H	L	Shift register clocked; Q _N = Q _{N-1} , Q ₀ = SER
↑	X	H	L	Contents of shift; register transferred to output latches

L = Logic Level LOW

H = Logic Level HIGH

X = Don't Care

↑ = Transition from LOW to HIGH level

Absolute Maximum Ratings⁽¹⁾

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V _{CC}	Supply Voltage		-0.5	7.0	V
V _{IN}	DC Input Voltage		-1.5 to V _{CC+}	1.5	V
V _{OUT}	DC Output Voltage		-0.5 to V _{CC+}	0.5	V
I _{IK} , I _{OK}	Clamp Diode Current			±20	mA
I _{OUT}	DC Output Current, per Pin			±35	mA
I _{CC}	DC VCC or GND Current, per Pin			±70	mA
T _{STG}	Storage Temperature Range		-65	+150	°C
P _D	Power Dissipation	PDIP ⁽²⁾		600	mW
		SOIC Package Only		500	
T _L	Lead Temperature			+260	°C
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114		4000	V

Notes:

1. Unless otherwise specified all voltages are referenced to ground.
2. Power dissipation temperature derating, plastic package (PDIP); 12mW/°C from -65 to +85°C.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter		Min.	Max.	Unit
V _{CC}	Supply Voltage		2	6	V
V _{IN} , V _{OUT}	DC Input or Output Voltage		0	V _{CC}	V
T _A	Operating Temperature Range		-40	+85	°C
t _R , t _F	Input Rise and Fall Times	V _{CC} =2.0V		1000	ns
		V _{CC} =4.5V		500	
		V _{CC} =6.0V		400	

Electrical Characteristics⁽³⁾

Symbol	Parameter	Conditions	V _{CC}	T _A =25°C	T _A =-40 to 85°C	T _A =-55 to 125°C	Units		
				Typ.	Guaranteed Limits				
V _{IH}	Minimum HIGH Level Input Voltage		2.0V		1.50	1.50	1.50	V	
			4.5V		3.15	3.15	3.15		
			6.0V		4.20	4.20	4.20		
V _{IL}	Minimum LOW Level Input Voltage		2.0V		0.50	0.50	0.50	V	
			4.5V		1.35	1.35	1.35		
			6.0V		1.80	1.80	1.80		
V _{OH}	Minimum HIGH Level Output Voltage	V _{IN} =V _{IH} or V _{IL}	I _{OUT} ≤ 20μA	2.0V	2.00	1.90	1.90	1.90	V
				4.5V	4.50	4.40	4.40	4.40	
				6.0V	6.00	5.90	5.90	5.90	
	Q' _H	V _{IN} =V _{IH} or V _{IL}	I _{OUT} ≤ 4.0mA	4.5V	4.20	3.98	3.84	3.70	V
				6.0V	5.20	5.48	5.34	5.20	
	Q _A through Q _H	V _{IN} =V _{IH} or V _{IL}	I _{OUT} ≤ 6.0mA	4.5V	4.20	3.98	3.84	3.70	V
6.0V				5.70	5.48	5.34	5.20		
V _{OL}	Minimum LOW Level Output Voltage	V _{IN} =V _{IH} or V _{IL}	I _{OUT} ≤ 20μA	2.0V	0	0.10	0.10	0.10	V
				4.5V	0	0.10	0.10	0.10	
				6.0V	0	0.10	0.10	0.10	
	Q' _H	V _{IN} =V _{IH} or V _{IL}	I _{OUT} ≤ 4.0mA	4.5V	0.20	0.26	0.33	0.40	V
				6.0V	0.20	0.26	0.33	0.40	
	Q _A through Q _H	V _{IN} =V _{IH} or V _{IL}	I _{OUT} ≤ 6.0mA	4.5V	0.20	0.26	0.33	0.40	V
6.0V				0.20	0.26	0.33	0.40		
I _{IN}	Maximum Input Output Leakage	V _{IN} =V _{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA	
I _{OZ}	Maximum 3-State Output Leakage	V _{OUT} =V _{CC} or GND	G=V _{IH}	6.0V		±0.5	±5.0	±10	μA
I _{CC}	Maximum Quiescent Supply Current	V _{IN} =V _{CC} or GND	I _{OUT} =μA	6.0V		8.0	80	160	μA

Note:

3. For a power supply of 5V ±10%, the worst-case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. The 4.5V values should be used when designing with this supply. Worst-case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V, respectively; V_{IH} value at 5.5V is 3.85V. The worst-case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occurs for CMOS at the higher voltage; so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC} = 5V$, $T_A = 25^\circ C$, $t_r = t_f = 6ns$.

Symbol	Parameter	Conditions	Typ.	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency of SCK		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, SCK to Q'_H	$C_L=45pF$	12	20	ns
	Maximum Propagation Delay, RCK to Q_A thru Q'_H		18	30	
t_{PZH}, t_{PZL}	Maximum Output Enable Time from \overline{G} to Q_A thru Q'_H	$R_L=1k\Omega, C_L=45pF$	17	28	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time from \overline{G} to Q_A thru Q'_H	$R_L=1k\Omega, C_L=45pF$	15	25	ns
t_s	Minimum Setup Time from SER to SCK			20	ns
	Minimum Setup Time from \overline{SCLR} to SCK			20	ns
	Minimum Setup Time from SER to RCK ⁽⁴⁾			40	ns
t_H	Minimum Hold Time from SER to SCK			0	ns
t_w	Minimum Pulse Width of SCK or RCK			16	ns

Note:

- This setup time ensures the register will see stable data from the shift-register outputs. The clocks may be connected together in which case the storage register state will be one clock pulse behind the shift register.

Electrical Characteristics

$V_{CC} = 2.0\text{--}6.0\text{V}$, $C_L = 50\text{pF}$, $t_r = t_f = 6\text{ns}$ unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC}	$T_A=25^\circ\text{C}$		$T_A=-40$ to	$T_A=-55$	Units	
				Typ.	Guaranteed Limits		85°C		to 125°C
f_{MAX}	Maximum Operating Frequency	$C_L=50\text{pF}$	2.0V	10.0	6.0	4.8	4.0	ns	
			4.5V	45.0	30.0	24.0	20.0		
			6.0V	50.0	35.0	28.0	24.0		
t_{PHL}, t_{PLH}	Maximum Propagation Delay, SCK to Q'_H	$C_L=50\text{pF}$	2.0V	58.0	210.0	235.0	315.0	ns	
			2.0V	83.0	294.0	367.0	441.0		
		$C_L=150\text{pF}$	4.5V	14.0	42.0	53.0	63.0		
			4.5V	17.0	58.0	74.0	88.0		
		$C_L=50\text{pF}$	6.0V	10.0	36.0	45.0	54.0		
			6.0V	14.0	50.0	63.0	76.0		
	Maximum Propagation Delay, RCK to Q_A thru Q'_H	$C_L=50\text{pF}$	2.0V	70.0	175.0	220.0	265.0	ns	
			2.0V	105.0	245.0	306.0	368.0		
		$C_L=150\text{pF}$	4.5V	21.0	35.0	44.0	53.0		
			4.5V	28.0	49.0	61.0	74.0		
		$C_L=50\text{pF}$	6.0V	18.0	30.0	37.0	45.0		
			6.0V	26.0	42.0	53.0	63.0		
Maximum Propagation Delay, SCLR to Q'_H		2.0V		175.0	221.0	261.0	ns		
		4.5V		35.0	44.0	52.0			
		6.0V		30.0	37.0	44.0			
t_{PZH}, t_{PZL}	Maximum Output Enable Time from \overline{G} to Q_A thru Q'_H	$R_L=1\text{k}\Omega$	$C_L=50\text{pF}$	2.0V	75.0	175.0	220.0	265.0	ns
			$C_L=150\text{pF}$	2.0V	100.0	245.0	306.0	368.0	
		$C_L=50\text{pF}$	4.5V	15.0	35.0	44.0	53.0		
			4.5V	20.0	49.0	61.0	74.0		
		$C_L=50\text{pF}$	6.0V	13.0	30.0	37.0	45.0		
			6.0V	17.0	42.0	53.0	63.0		
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time from \overline{G} to Q_A thru Q'_H	$R_L=1\text{k}\Omega, C_L=50\text{pF}$	2.0V	75.0	175.0	220.0	265.0	ns	
			4.5V	15.0	35.0	44.0	53.0		
			6.0V	13.0	30.0	37.0	45.0		

Continued on the following page...

Electrical Characteristics

$V_{CC} = 2.0\text{--}6.0\text{V}$, $C_L = 50\text{pF}$, $t_r = t_f = 6\text{ns}$ unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC}	$T_A=25^\circ\text{C}$		$T_A=-40$ to	$T_A=-55$	Units
				Typ.	Guaranteed Limits			
t_s	Minimum Setup Time from SER to SCK	$R_L=1\text{k}\Omega$, $C_L=50\text{pF}$	2.0V		100	125	150	ns
			4.5V		20	25	30	
			6.0V		17	21	25	
t_R	Minimum Removal Time from SCLR to SCK		2.0V		50	63	75	ns
			4.5V		10	13	15	
			6.0V		9	11	13	
t_s	Minimum Setup Time from SCK to RCK		2.0V		100	125	150	ns
			4.5V		20	25	30	
			6.0V		17	21	26	
t_H	Minimum Hold Time from SER to SCK		2.0V		5	5	5	ns
			4.5V		5	5	5	
			6.0V		5	5	5	
t_W	Minimum Pulse Width of SCK or SCLR		2.0V	30	80	100	120	ns
			4.5V	9	16	20	24	
			6.0V	8	14	18	22	
t_R, t_F	Maximum Input Rise and Fall Time, Clock		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	
			6.0V		400	400	400	
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time $Q_A\text{--}Q_H$		2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	
			6.0V	6	10	13	15	
	Maximum Output Rise and Fall Time Q'_H		2.0V		75	95	110	ns
			4.5V		15	19	22	
			6.0V		13	16	19	
C_{PD}	Power Dissipation Capacitance, Outputs Enabled ⁽⁵⁾	$\overline{G}=V_{CC}$		90				pF
		$\overline{G}=GND$		150				
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note:

5. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Timing Diagram



Figure 3. Timing Diagram

Note:

6. XXX Implies that the output is in 3-state mode.

Physical Dimensions

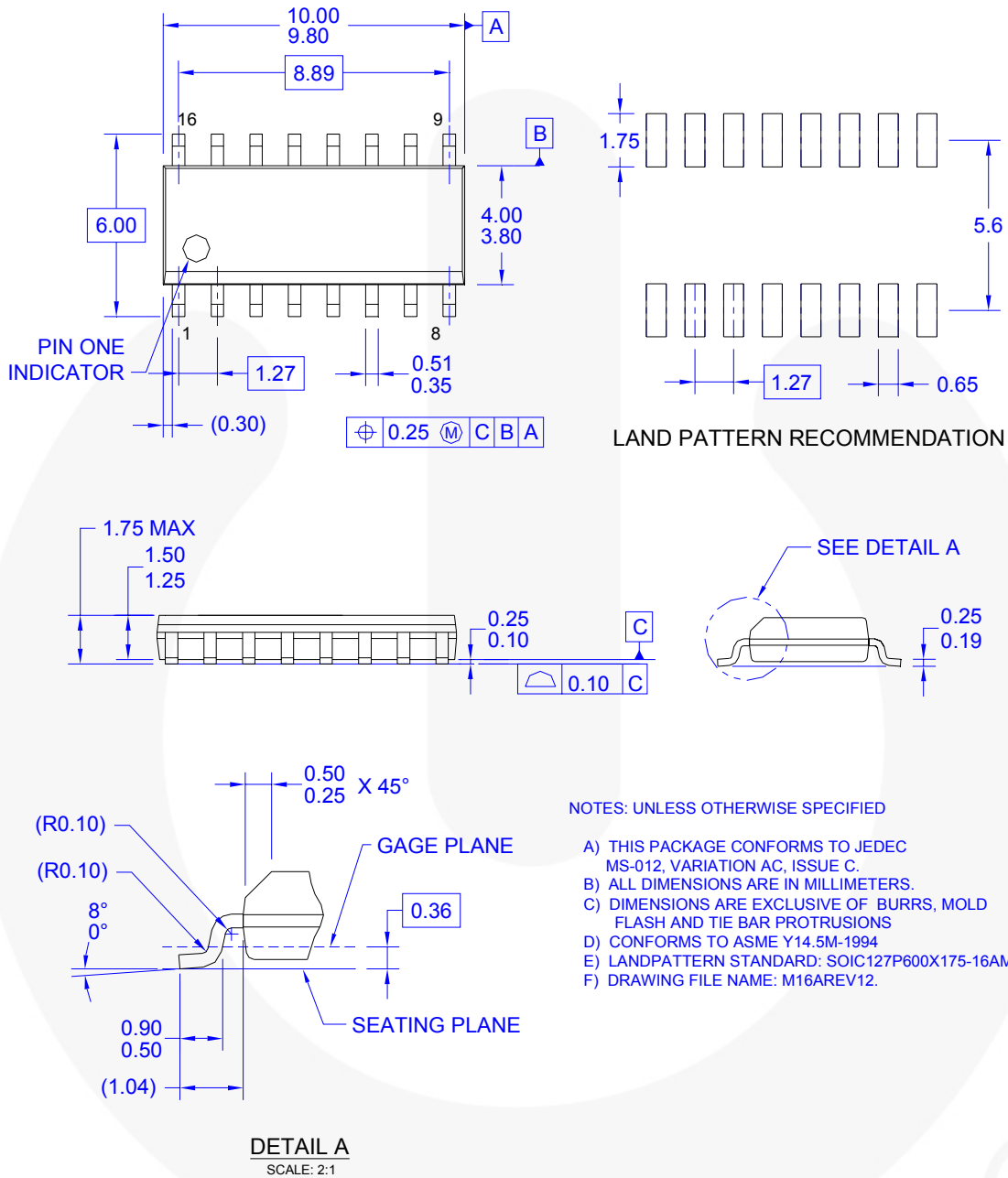


Figure 4. 16-Lead, Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Inch Narrow

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Physical Dimensions



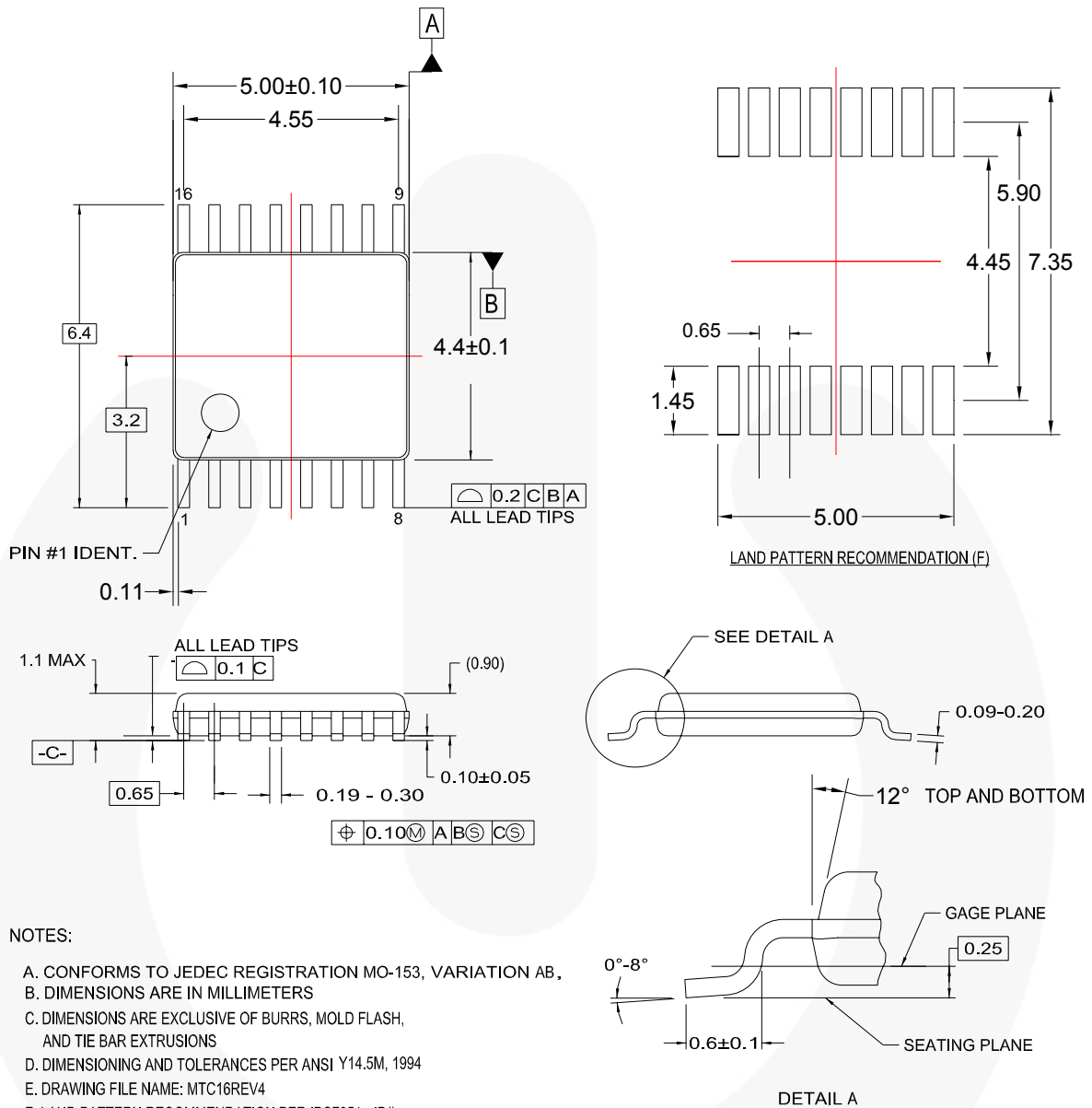
M16DREVC

Figure 5. 16-Lead, Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

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Physical Dimensions



MTC16rev4

Figure 6. 16-Lead, Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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Physical Dimensions



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO JEDEC MS-001 VARIATION BB
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR PROTRUSIONS
 - D) CONFORMS TO ASME Y14.5M-1994
 - E) DRAWING FILE NAME: N16EREV1

Figure 7. 16-Lead, Plastic Dual In-Line Package (PDIP), JEDEC MS-001, 0.300 Inch Wide

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Definition of Terms

Datasheet Identification	Product Status	Definition
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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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