Medium Power Phase Control Thyristors (Power Modules), 50 A, 70 A, 90 A

D-55

FEATURES

- Electrically isolated base plate
- Types up to 1200 V_{RRM}
- 3500 V_{RMS} isolating voltage
- Simplified mechanical designs, rapid assembly
- High surge capability
- Large creepage distances
- UL E78996 approved
- Designed and qualified for industrial level
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT

DESCRIPTION

These series of T-modules are intended for general purpose applications such as battery chargers, welders and plating equipment, regulated power supplies and temperature and speed control circuits. The semiconductors are electrically isolated from the metal base, allowing common heatsinks and compact assemblies to be built.

PRODUCT SUMMARY	
Package	D-55
Diode variation	Single SCR
$I_{T(AV)}$	50 A, 70 A, 90 A
V_{DRM}/V_{RRM}	100 V, 1200 V
V_{TM}	1.55 V
I_{GT}	120 mA
T_J	-40 °C to 125 °C

MAJOR RATINGS AND CHARACTERISTICS					
SYMBOL	CHARACTERISTICS	T50RIA	T70RIA	T90RIA	UNITS
$I_{T(AV)}$	70 °C	50	70	90	A
$I_{T(RMS)}$		80	110	141	A
I_{TSM}	50 Hz	1310	1660	1780	A
	60 Hz	1370	1740	1870	
I^2t	50 Hz	8550	13 860	15 900	A^2s
	60 Hz	7800	12 650	14 500	
$I^2\sqrt{t}$		85 500	138 500	159 100	$A^2\sqrt{s}$
V_{RRM}	Range	100 to 1200			V
T_J		-40 to 125			°C

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS				
TYPE NUMBER	VOLTAGE CODE	V_{RRM}/V_{DRM}, MAXIMUM REPETITIVE PEAK REVERSE AND PEAK OFF-STATE VOLTAGE V	V_{RSM}, MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	I_{RRM}/I_{DRM} MAXIMUM AT T_J = 25 °C µA
VS-T50RIA VS-T70RIA VS-T90RIA	10	100	150	100
	20	200	300	
	40	400	500	
	60	600	700	
	80	800	900	
	100	1000	1100	
	120	1200	1300	

ON-STATE CONDUCTION								
PARAMETER	SYMBOL	TEST CONDITIONS			T50RIA	T70RIA	T90RIA	UNITS
Maximum average on-state current at case temperature	$I_{T(AV)}$	180° conduction, half sine wave			50	70	90	A
					70	70	70	°C
Maximum RMS on-state current	$I_{T(RMS)}$				80	110	141	A
Maximum peak, one-cycle on-state, non-repetitive surge current	I_{TSM}	t = 10 ms	No voltage reapplied	Sine half wave, initial $T_J = T_J$ maximum	1310	1660	1780	A
		t = 8.3 ms			1370	1740	1870	
		t = 10 ms	100 % V_{RRM} reapplied		1100	1400	1500	
		t = 8.3 ms			1150	1460	1570	
Maximum I^2t for fusing	I^2t	t = 10 ms	No voltage reapplied		8550	13 860	15 900	A^2s
		t = 8.3 ms			7800	12 650	14 500	
		t = 10 ms	100 % V_{RRM} reapplied		6050	9800	11 250	
		t = 8.3 ms			5520	8950	10 270	
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 to 10 ms, no voltage reapplied			85 500	138 500	159 100	$A^2\sqrt{s}$
Low level value of threshold voltage	$V_{T(TO)1}$	(16.7 % x π x $I_{T(AV)}$ < I < π x $I_{T(AV)}$), T_J maximum			0.97	0.77	0.78	V
High level value of threshold voltage	$V_{T(TO)2}$	(I > π x $I_{T(AV)}$), T_J maximum			1.13	0.88	0.88	
Low level value of on-state slope resistance	r_{t1}	(16.7 % x π x $I_{T(AV)}$ < I < π x $I_{T(AV)}$), T_J maximum			4.1	3.6	2.9	mΩ
High level value of on-state slope resistance	r_{t2}	(I > π x $I_{T(AV)}$), T_J maximum			3.3	3.2	2.6	
Maximum on-state voltage drop	V_{TM}	I_{TM} = π x $I_{T(AV)}$, T_J = 25 °C, t_p = 400 µs square Average power = $V_{T(TO)}$ x $I_{T(AV)}$ + r_f x $(I_{T(RMS)})^2$			1.60	1.55	1.55	V
Maximum forward voltage drop	V_{FM}	I_{TM} = π x $I_{T(AV)}$, T_J = 25 °C, t_p = 400 µs square Average power = $V_{T(TO)}$ x $I_{T(AV)}$ + r_f x $(I_{T(RMS)})^2$			1.60	1.55	1.55	V
Maximum holding current	I_H	Anode supply = 6 V, initial I_T = 30 A, T_J = 25 °C			200	200	200	mA
Maximum latching current	I_L	Anode supply = 6 V, resistive load = 10 Ω Gate pulse: 10 V, 100 µs, T_J = 25 °C			400	400	400	

SWITCHING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Typical turn-on time	t_{gd}	T_J = 25 °C, V_d = 50 % V_{DRM}, I_{TM} = 50 A I_g = 500 mA, $t_r \leq 0.5$, $t_p \geq 6$ µs	0.9	µs
Typical reverse recovery time	t_{rr}	T_J = 125 °C, I_{TM} = 50 A, t_p = 300 µs, dI/dt = 10 A/µs	3	
Typical turn-off time	t_q	$T_J = T_J$ maximum, I_{TM} = 50 A, t_p = 300 µs, dI/dt = 15 A/µs, V_R = 100 V, linear to 80 % V_{DRM}	110	

BLOCKING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum peak reverse and off-state leakage current	I_{RRM}, I_{DRM}	$T_J = T_J$ maximum	15	mA
RMS isolation voltage	V_{ISOL}	50 Hz, circuit to base, all terminals shorted, T_J = 25 °C, t = 1 s	3500	V
Critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum, linear to 80 % rated V_{DRM} (1)	500	V/µs

Note

(1) Available with dV/dt = 1000 V/µs, to complete code add S90 i.e. T90RIA80S90

TRIGGERING							
PARAMETER	SYMBOL	TEST CONDITIONS		T50RIA	T70RIA	T90RIA	UNITS
Maximum peak gate power	P_{GM}	$T_J = T_J$ maximum, $t_p \leq 5$ ms		10	12	12	W
Maximum average gate power	$P_{G(AV)}$	$T_J = T_J$ maximum, f = 50 Hz		2.5	3	3	
Maximum peak gate current	I_{GM}	$T_J = T_J$ maximum, $t_p \leq 5$ ms		2.5	3	3	A
Maximum peak negative gate voltage	$-V_{GT}$			10	10	10	V
Maximum required DC gate voltage to trigger	V_{GT}	T_J = - 40 °C	Anode supply = 6 V, resistive load; Ra = 1 Ω	4.0	4.0	4.0	V
		T_J = 25 °C		2.5	2.5	2.5	
		$T_J = T_J$ maximum		1.5	1.5	1.5	
Maximum required DC gate current to trigger	I_{GT}	T_J = - 40 °C		250	270	270	mA
		T_J = 25 °C		100	120	120	
		$T_J = T_J$ maximum		50	60	60	
Maximum gate voltage that will not trigger	V_{GD}	$T_J = T_J$ maximum, rated V_{DRM} applied		0.2	0.2	0.2	V
Maximum gate current that will not trigger	I_{GD}			5.0	6.0	6.0	mA
Maximum rate of rise of turned-on current	dI/dt	V_D = 0.67 rated V_{DRM}, I_{TM} = 2 x rated dI/dt I_g = 400 mA for T50RIA and I_g = 500 mA for T70RIA/T90RIA; $t_r < 0.5$ µs, $t_p \geq 6$ µs For repetitive value use 40 % non-repetitive Per JEDEC STD. RS397, 5.2.2.6		200	200	200	A/µs
				180	180	180	
				160	160	160	
				150	150	150	

THERMAL AND MECHANICAL SPECIFICATIONS							
PARAMETER		SYMBOL	TEST CONDITIONS		T50RIA	T70RIA	T90RIA	UNITS
Maximum junction operating temperature range		T_J			- 40 to 125			°C
Maximum storage temperature range		T_{Stg}			- 40 to 150			
Maximum thermal resistance, junction to case per junction		R_{thJC}	DC operation		0.65	0.50	0.38	K/W
Maximum thermal resistance, case to heatsink		R_{thCS}	Mounting surface, smooth, flat and greased		0.2			
Mounting torque, ± 10 %	to heatsink		Non-lubricated threads	M3.5 mounting screws (1)	1.3 ± 10 %			Nm
	terminals			M5 screw terminals	3 ± 10 %			
Approximate weight					54			g
Case style					D-55 (T-module)			

Note

(1) A mounting compound is recommended and the torque should be rechecked after a period of 3 hours to allow for the spread of the compound

ΔR CONDUCTION PER JUNCTION											
DEVICES	SINUSOIDAL CONDUCTION AT T_J MAXIMUM					RECTANGULAR CONDUCTION AT T_J MAXIMUM					UNITS
	180°	120°	90°	60°	30°	180°	120°	90°	60°	30°	
T50RIA	0.08	0.10	0.13	0.19	0.31	0.06	0.10	0.14	0.20	0.32	K/W
T70RIA	0.07	0.08	0.10	0.14	0.24	0.05	0.08	0.11	0.15	0.24	
T90RIA	0.05	0.06	0.08	0.12	0.20	0.04	0.06	0.09	0.12	0.20	

Note

- Table shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC

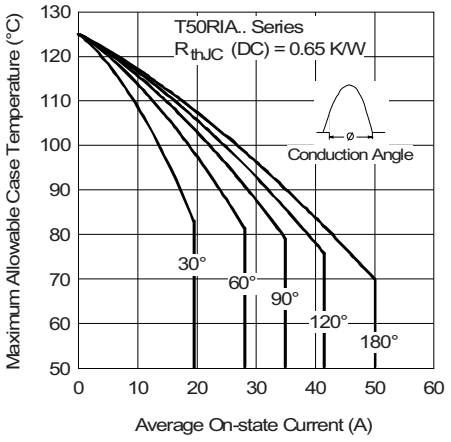


Fig. 1 - Current Ratings Characteristics

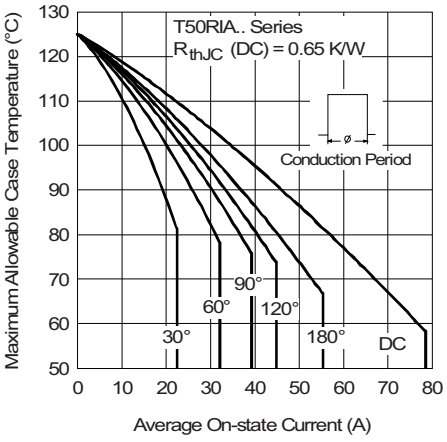


Fig. 2 - Current Ratings Characteristics

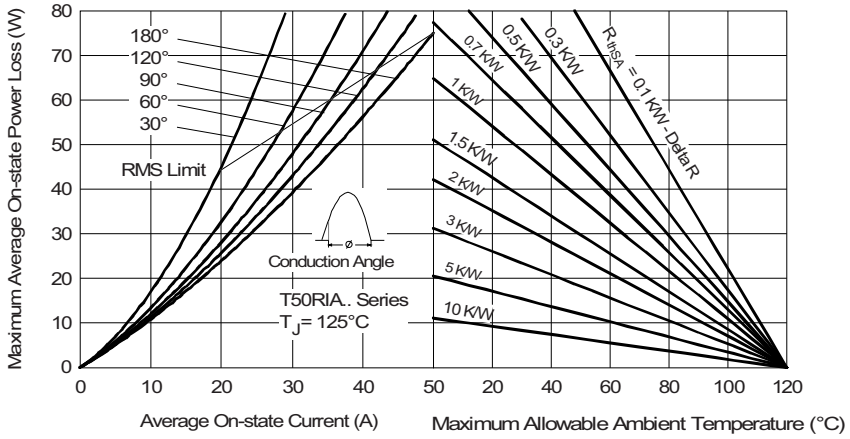


Fig. 3 - On-State Power Loss Characteristics

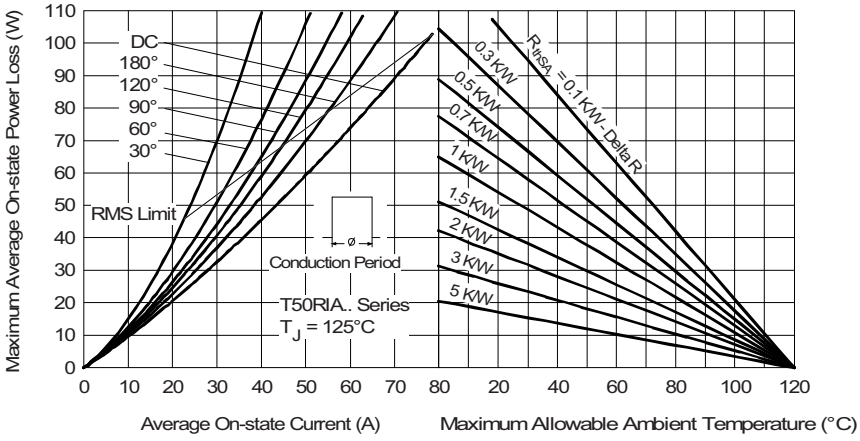


Fig. 4 - On-State Power Loss Characteristics

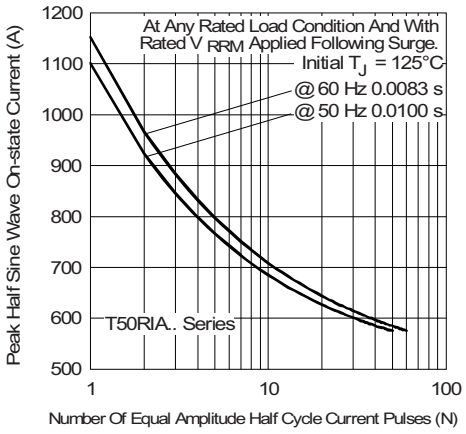


Fig. 5 - Maximum Non-Repetitive Surge Current

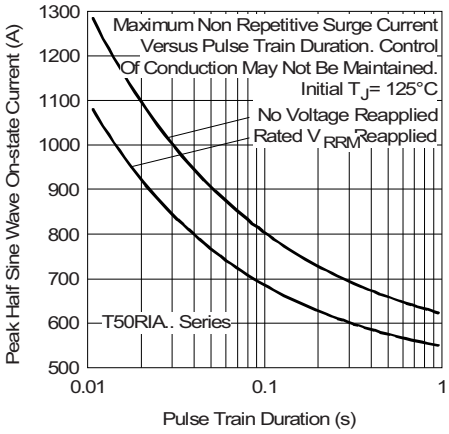


Fig. 6 - Maximum Non-Repetitive Surge Current

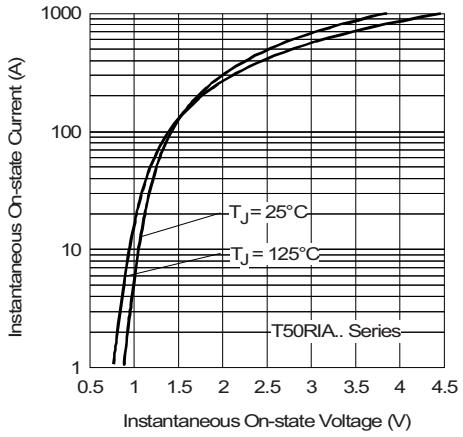


Fig. 7 - On-State Voltage Drop Characteristics

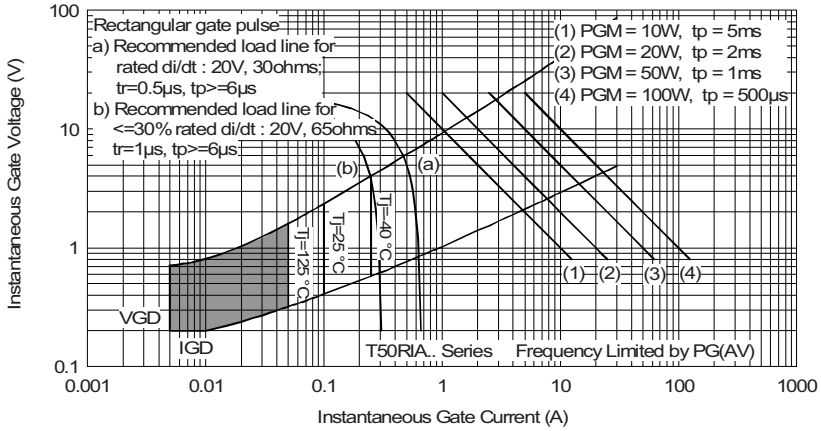


Fig. 8 - Gate Characteristics

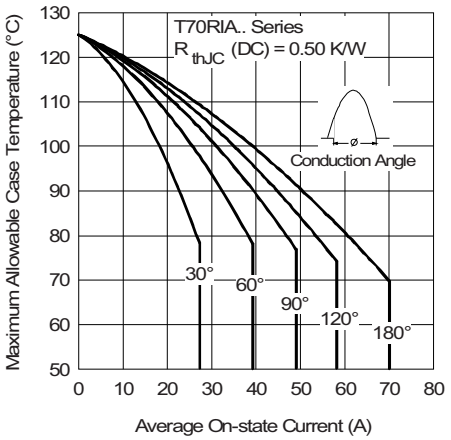


Fig. 9 - Current Ratings Characteristics

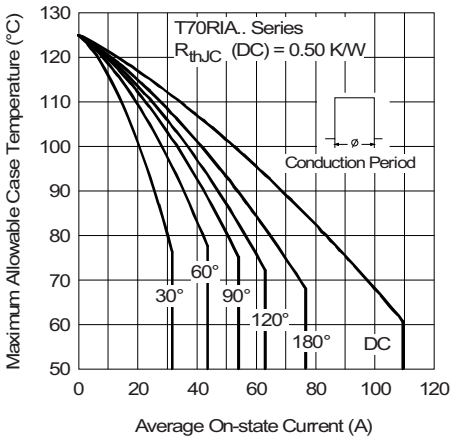


Fig. 10 - Current Ratings Characteristics

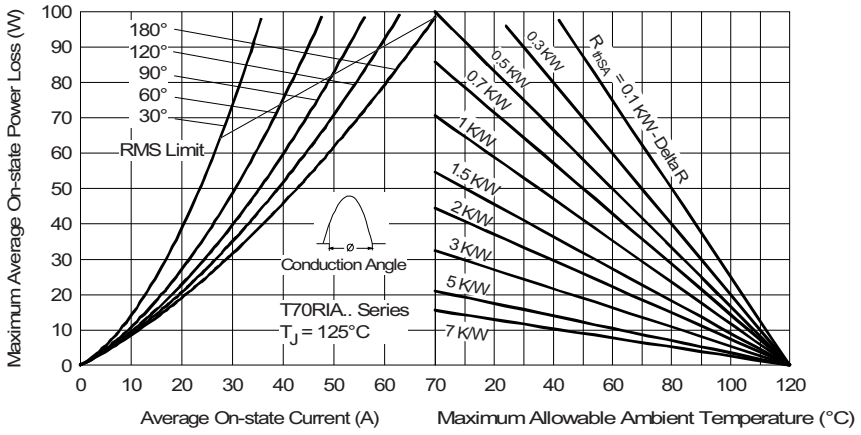


Fig. 11 - On-State Power Loss Characteristics

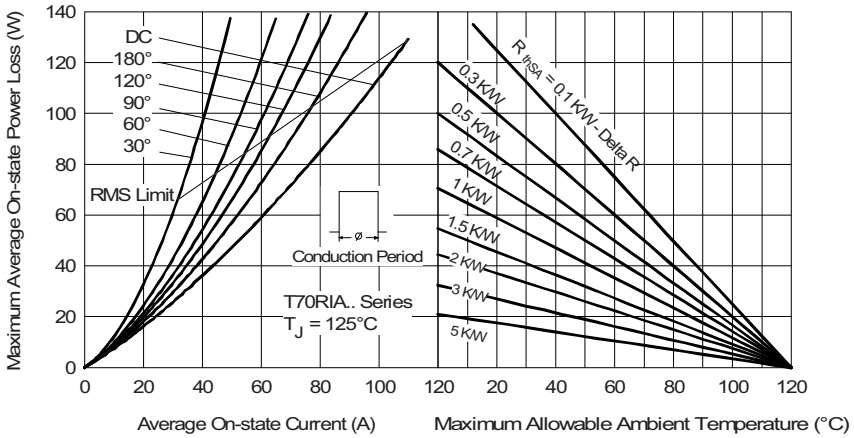


Fig. 12 - On-State Power Loss Characteristics

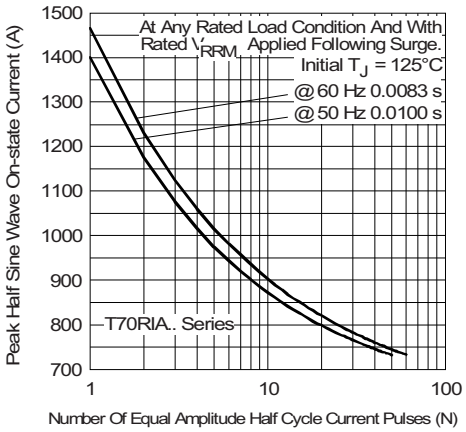


Fig. 13 - Maximum Non-Repetitive Surge Current

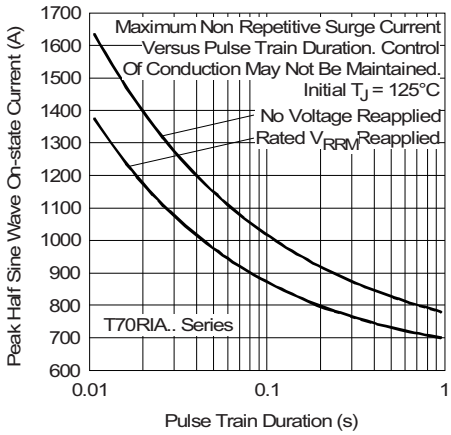


Fig. 14 - Maximum Non-Repetitive Surge Current

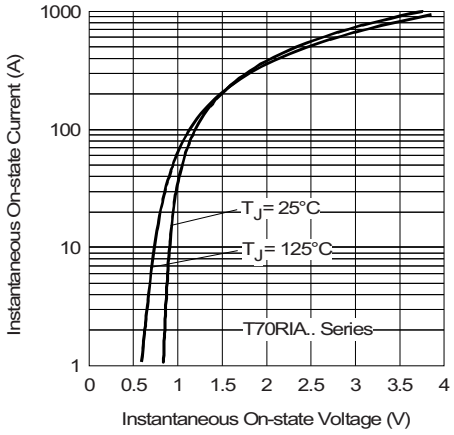


Fig. 15 - On-State Voltage Drop Characteristics

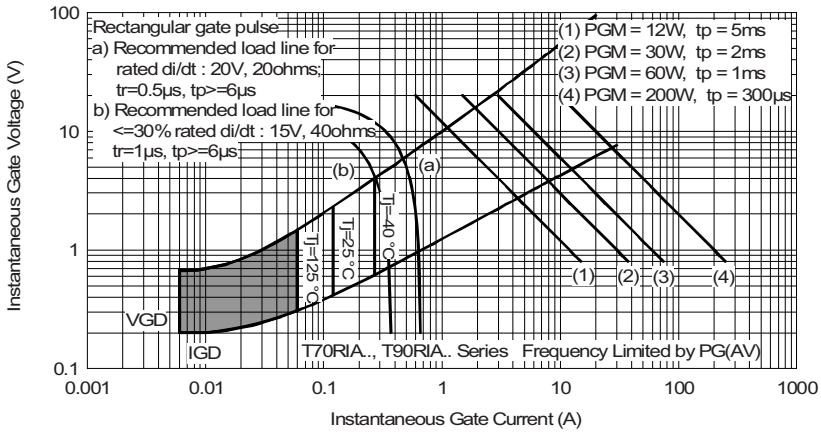


Fig. 16 - Gate Characteristics

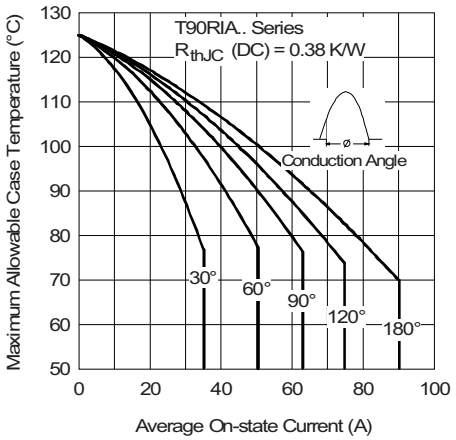


Fig. 17 - Current Ratings Characteristics

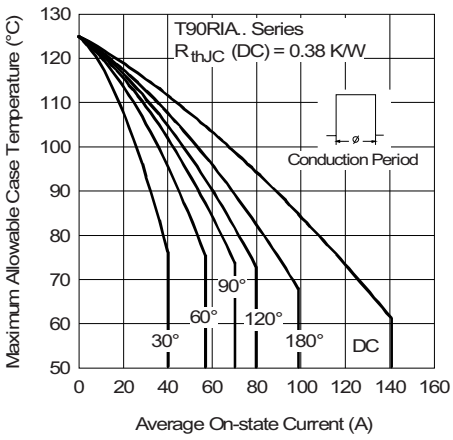


Fig. 18 - Current Ratings Characteristics

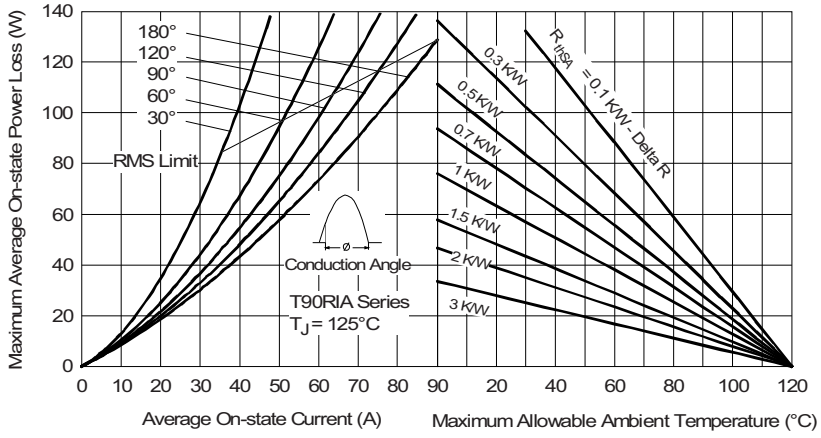


Fig. 19 - On-State Power Loss Characteristics

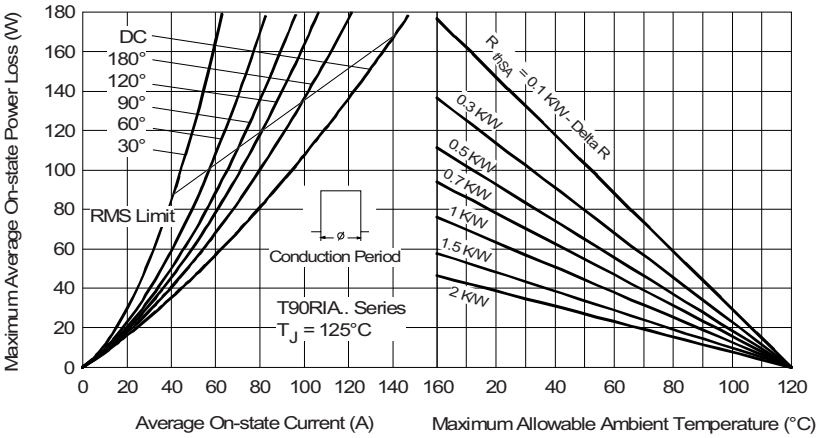


Fig. 20 - On-State Power Loss Characteristics

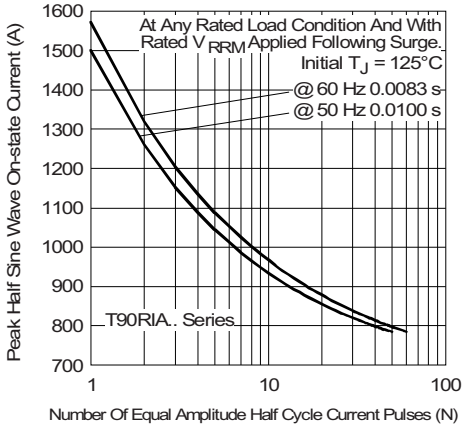


Fig. 21 - Maximum Non-Repetitive Surge Current

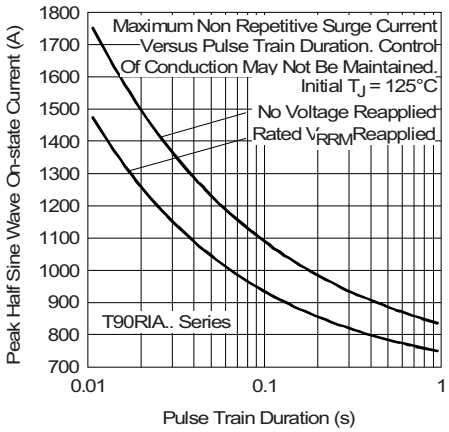


Fig. 22 - Maximum Non-Repetitive Surge Current

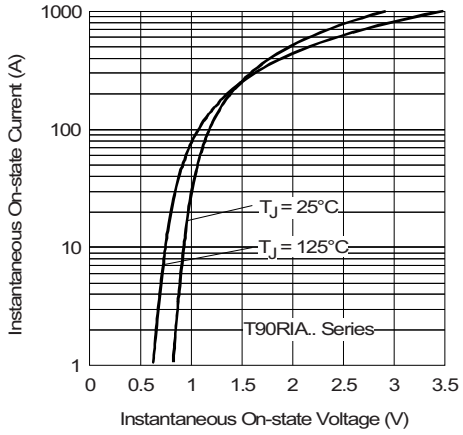


Fig. 23 - On-State Voltage Drop Characteristics

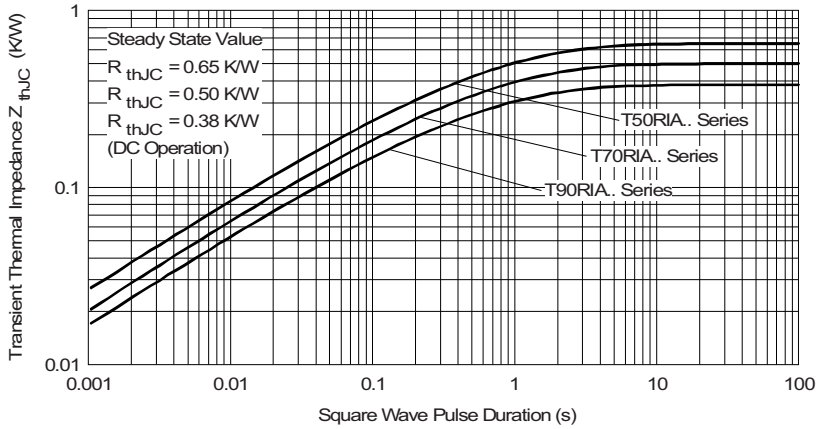


Fig. 24 - Thermal Impedance Z_{thJC} Characteristics

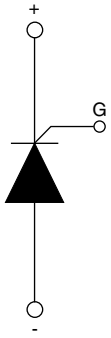
ORDERING INFORMATION TABLE

Device code

VS-	T	50	RIA	120
1	2	3	4	5

1 - Vishay Semiconductors product
2 - Module type
3 - Current rating
4 - Circuit configuration
5 - Voltage code x 10 = V_{RRM}

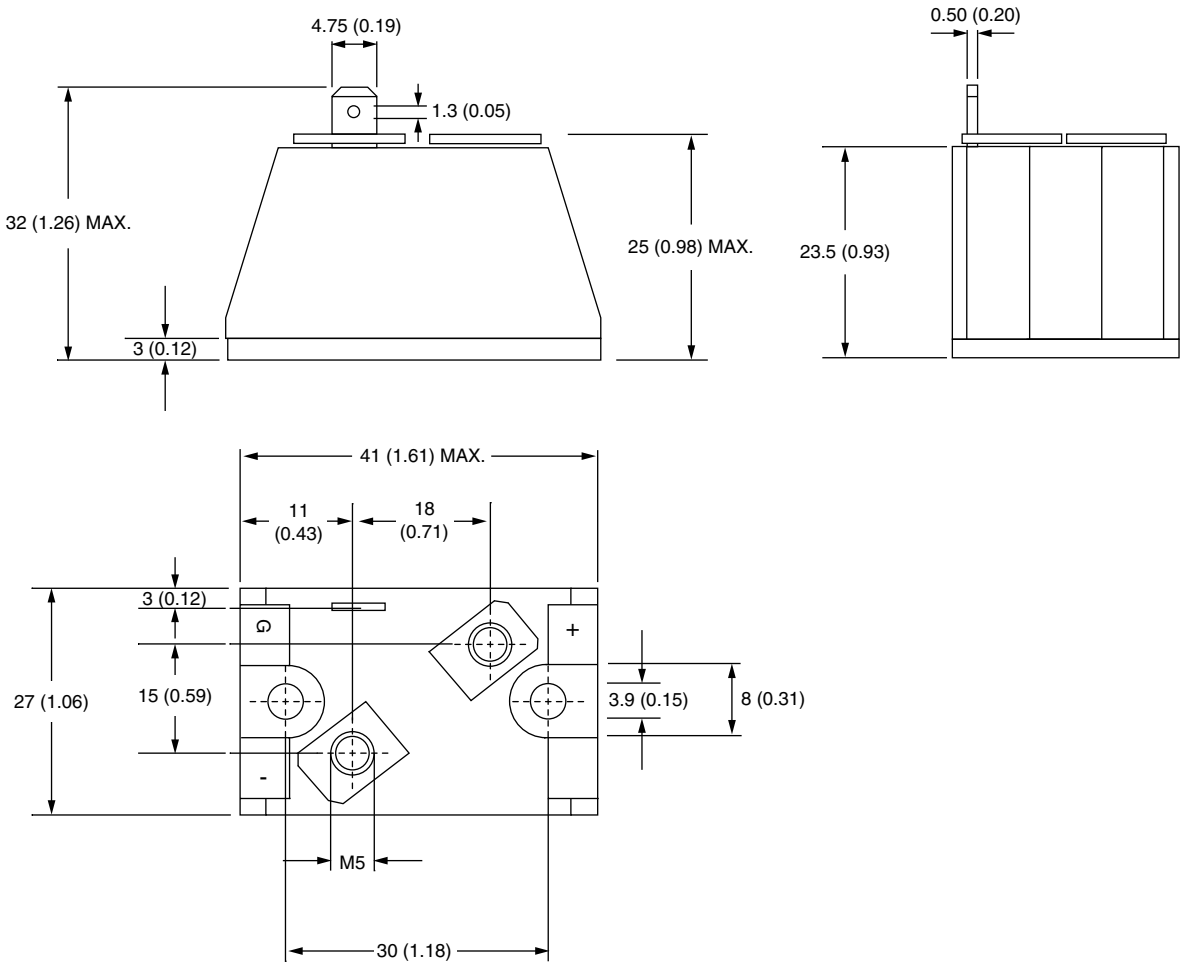
CIRCUIT CONFIGURATION



LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95336

D-55 T-Module Thyristor Standard

DIMENSIONS in millimeters (inches)



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