# Si8285/86 Data Sheet

## 4.0 Amp ISODrivers with System Safety Features

The Si828x (Si8285 and Si8286) are isolated, high current gate drivers with integrated system safety and feedback function. The devices are ideal for driving power MOSFETs and IGBTs used in a wide variety of inverter and motor control applications. The Si8285 and Si8286 isolated gate drivers utilize Silicon Labs' proprietary silicon isolation technology, supporting up to 5.0 kVrms withstand voltage per UL1577. This technology enables higher-performance, reduced variation with temperature and age, tighter part-to-part matching, and superior common-mode rejection compared to other isolated gate driver technologies.

The input to the device is a complementary digital input that can be utilized in several configurations. The input side of the isolation also has several control and feedback digital signals. The controller to the device receives information about the driver side power state (Si8285) and fault state of the device and recovers the device from fault through an active-low reset pin.

On the output side, the Si8285 provides separate pull-up and pull-down pins for the gate. The Si8286 has a single pin for both functions. A dedicated DSAT pin detects the desaturation condition and immediately shuts down the driver in a controlled manner. The Si8285 device also integrates a Miller clamp to facilitate a strong turn-off of the power switch.

**Applications**

- IGBT/ MOSFET gate drives
- Industrial, HEV, and renewable energy inverters
- AC, Brushless, and DC motor controls and drives
- Variable speed motor control in consumer white goods
- Isolated switch mode and UPS power supplies

**Safety Regulatory Approvals (Pending)**

- UL 1577 recognized
  - Up to 5000 $V_{RMS}$ for 1 minute
- CSA component notice 5A approval
  - IEC 60950-1 (reinforced insulation)
- VDE certification conformity
  - VDE0884 Part 10 (reinforced insulation)
- CQC certification approval
  - GB4943.1 (reinforced insulation)

**KEY FEATURES**

- 4 A IGBT driver
- System Safety Features
  - DESAT detection
  - FAULT feedback
  - Undervoltage Lock Out (UVLO)
  - Soft shutdown on fault condition
- Silicon Labs' high-performance isolation technology
  - Industry leading noise immunity
  - High speed, low latency and skew
  - Best reliability available
- 30 V driver-side supply voltage
- Integrated Miller clamp (Si8285 only)
- Power ready pin (Si8285 only)
- Complementary driver control input
- Si8286 pin-out compatible with HCPL-316J
- Compact package: 16-pin wide-body SOIC
- Industrial temperature range: –40 to 125°C


This information applies to a product under development. Its characteristics and specifications are subject to change without notice.

# 1. Ordering Guide

**Table 1.1. Si8285, Si8286 Ordering Guide**

| New Ordering Part Number (OPN) | Ordering Options | | | | |
|---|---|---|---|---|---|
| | Output Configuration | Pin Compatibility | UVLO Voltage | Insulation Rating | Package Type |
| Si8285BD-IS | 4.0 A driver | — | 9 V | 5.0 kVrms | WB SOIC-16 |
| Si8285CD-IS | 4.0 A driver | — | 12 V | 5.0 kVrms | WB SOIC-16 |
| Si8286BD-IS | 4.0 A driver | HCPL-316J | 9 V | 5.0 kVrms | WB SOIC-16 |
| Si8286CD-IS | 4.0 A driver | HCPL-316J | 12 V | 5.0 kVrms | WB SOIC-16 |

**Note:**

1. Visit www.silabs.com for detailed quality data.
2. “Si” and “SI” are used interchangeably.
3. AEC-Q100 qualified.
4. Add an "R" at the end of the Part Number to denote Tape and Reel option.

# 2. System Overview

## 2.1 Isolation Channel Description

The operation of a Si8285 or Si8286 channel is analogous to that of an optocoupler and gate driver, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single Si828x channel is shown in the figure below.

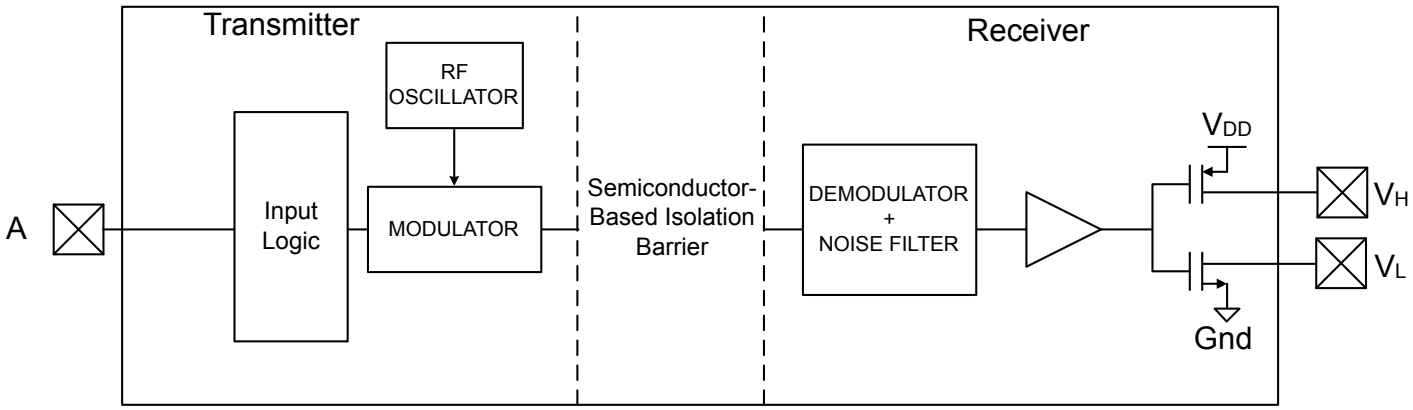



**Figure 2.1. Simplified Channel Diagram**

A channel consists of an RF Transmitter and RF Receiver separated by a semiconductor-based isolation barrier. Referring to the Transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying. The Receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and better immunity to magnetic fields.

### 2.2 Device Behavior

The following tables show the truth tables for the Si8285 and Si8286.

**Table 2.1. Si8285 Truth Table**

| IN+ | IN– | VDDA State | VDDB–VMID State | Desaturation State | VH | VL | RDY | FLTb |
|---|---|---|---|---|---|---|---|---|
| H | H | Powered | Powered | Undetected | Hi-Z | Pull-down | H | H |
| H | L | Powered | Powered | Undetected | Pull-up | Hi-Z | H | H |
| L | X | Powered | Powered | Undetected | Hi-Z | Pull-down | H | H |
| X | X | Powered | Unpowered | — | — | — | L | H |
| X | X | Powered | Powered | Detected | Hi-Z | Pull-down[1] | H | L |

**Note:**
1. Driver state after soft shutdown.

**Table 2.2. Si8286 Truth Table**

| IN+ | IN– | VDDA State | VDDB–VMID State | Desaturation State | VO | /FLT |
|---|---|---|---|---|---|---|
| H | H | Powered | Powered | Undetected | Low | H |
| H | L | Powered | Powered | Undetected | High | H |
| L | X | Powered | Powered | Undetected | Low | H |
| X | X | Powered | Powered | Detected | Low[1] | L |

**Note:**
1. Driver state after soft shutdown.

### 2.3 Input

The IN+ and IN– inputs to the Si828x devices act as a complementary pair. If the IN– is held low, the IN+ will act as a active-high input for the driver control. Alternatively, if IN+ is held high, then the IN– can be used as an active-low input for driver control. When the IN– is used as the control signal, taking the IN+ low will hold the output driver low.

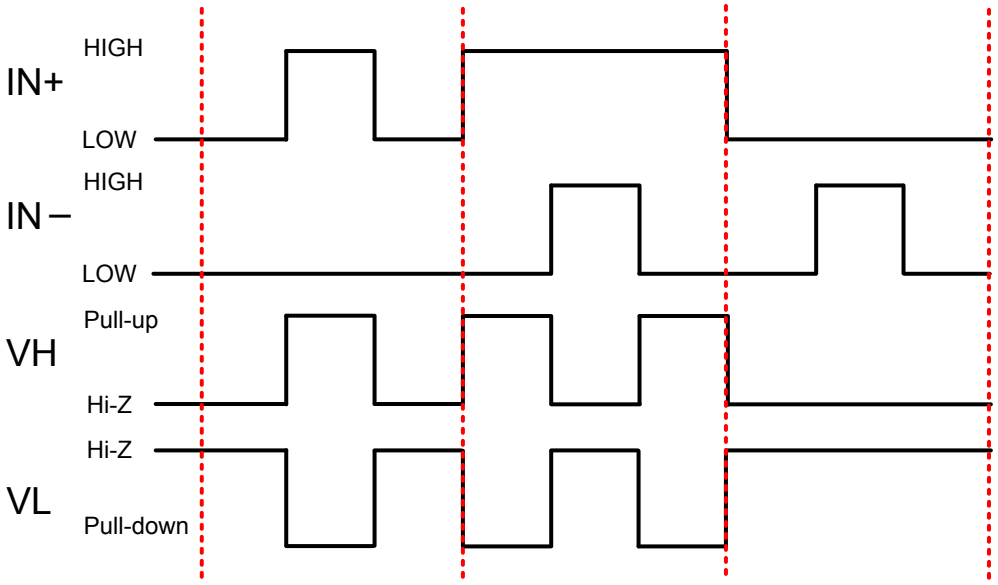



**Figure 2.2. Si828x Complementary Input Diagram**

### 2.4 Output

The Si8285 and Si8286 devices are different in how the driver output is presented. The Si8285 has separate pins for gate drive high (VH) and gate drive low (VL). This makes it simple for the user to use different gate resistors to control IGBT VCE rise and fall time. The Si8286 has both actions combined in the single VO pin. A weak internal pulldown resistor of about 200 kΩ is provided to ensure that the driver output defaults to low if power on the secondary side is interrupted.

### 2.5 Desaturation Detection

The Si828x provides sufficient voltage and current to drive and keep the IGBT in saturation during on time to minimize power dissipation and maintain high efficiency operation. However, abnormal load conditions can force the IGBT out of saturation and cause permanent damage to the IGBT.

To protect the IGBT during abnormal load conditions, the Si828x detects an IGBT desaturation condition, shuts down the driver upon detecting a fault, and provides a fault indication to the controller. These integrated features provide desaturation protection with minimum external BOM cost. The figure below illustrates the Si828x desaturation circuit. When the Si828x driver output is high, the internal current source is on, and this current flows from the DSAT pin to charge the CBL capacitor. The voltage on the DSAT pin is monitored by an internal comparator. Since the DSAT pin is connected to the IGBT collector through the $D_{DSAT}$ and a small $R_{DSAT}$, its voltage is almost the same as the $V_{CE}$ of the IGBT. If the $V_{CE}$ of the IGBT does not drop below the Si828x desaturation threshold voltage within a certain time after turning on the IGBT (blanking period) the block will generate a fault signal. The Si828x desaturation hysteresis is fixed at 220 mV and threshold is nominally 7 V.

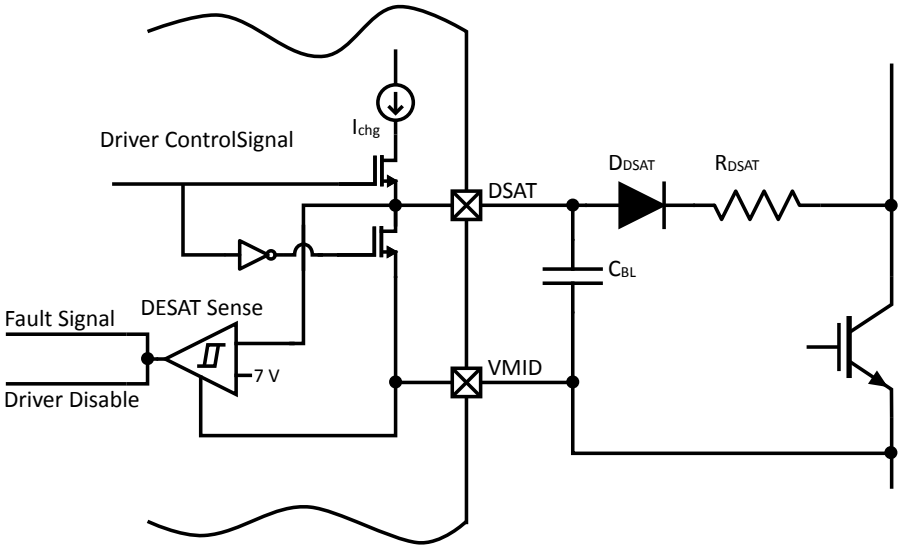



**Figure 2.3. Desaturation Circuit**

As an additional feature, the block supports a blanking timer function to mask the turn-on transient of the external switching device and avoid unexpected fault signal generation. This function requires an external blanking capacitor, $C_{BL}$, of typically 100 pF between DSAT and VMID pins. The block includes a 1 mA current source ($I_{Chg}$) to charge the $C_{BL}$. This current source, the value of the external $C_{BL}$, and the programmed fault threshold, determine the blanking time ($t_{Blanking}$).

$$t_{Blanking} = C_{Bl} \times \frac{V_{DESAT}}{I_{chg}}$$

An internal nmos switch is implemented between DSAT and VMID to discharge the external blanking capacitor, $C_{BL}$, and reset the blanking timer. The current limiting $R_{DSAT}$ resistor protects the DSAT pin from large current flow toward the IGBT collector during the IGBT's body diode freewheeling period (with possible large collector's negative voltage, relative to IGBT's emitter).

### 2.6 Soft Shutdown

To avoid excessive dV/dt on the IGBT's collector during fault shut down, the Si828x implements a soft shut down feature to discharge the IGBT's gate slowly. When soft shut down is activated, the high power driver goes inactive, and a weak pull down via VH and external RH discharges the gate until the gate voltage level is reduced to the VSSB + 2 V level. The high power driver is then turned on to clamp the IGBT gate voltage to VMID.

After the soft shut down, the Si828x driver output voltage is clamped low to keep the IGBT in the off state.

### 2.7 Fault (FLTb) Pin

FLTb is an open-drain type output. Once the UVLO condition is cleared on the driver side of the device, the FLTb pin is released. A pull-up resistor takes the pin high. When the desaturation condition is detected, the Si828x indicates the fault by bringing the FLTb pin low. FLTb stays low until the controller brings the RSTb pin low.

FLTb is also taken low if the UVLO condition is met during device operation. FLTb is released in that case as soon as the UVLO condition is cleared.

### 2.8 Reset (RSTb) Pin

The RSTb pin is used to clear the desaturation condition and bring the Si828x driver back to an operational state. Even though the input may be toggling, the driver will not change state until the fault condition has been reset.

### 2.9 Undervoltage Lockout (UVLO)

The UVLO circuit unconditionally drives VL low when VDDB is below the lockout threshold. The Si828x is maintained in UVLO until VDDB rises above $VDDB_{UV+}$. During power down, the Si828x enters UVLO when VDDB falls below the UVLO threshold plus hysteresis (i.e., VDDB $\leq$ $VDDB_{UV+}$ – $VDDB_{HYS}$).

### 2.10 Ready (RDY) Pin (Si8285 Only)

The ready pin indicates to the controller that power is available on both sides of the isolation, i.e., at VDDA and VDDB. RDY goes high when both the primary side and secondary side UVLO circuits are disengaged. If the UVLO conditions are met on either side of the isolation barrier, the ready pin will return low. RDY is a push-pull output pin and can be floated if not used.

### 2.11 Miller Clamp

IGBT power circuits are commonly connected in a half bridge configuration with the collector of the bottom IGBT tied to the emitter of the top IGBT.

When the upper IGBT turns on (while the bottom IGBT is in the off state), the voltage on the collector of the bottom IGBT flies up several hundred volts quickly (fast dV/dt). This fast dV/dt induces a current across the IGBT collector-to-gate capacitor ($C_{CG}$ that constitutes a positive gate voltage spike and can turn on the bottom IGBT. This behavior is called Miller parasitic turn on and can be destructive to the switch since it causes shoot through current from the rail right across the two IGBTs to ground. The Si828x Miller clamp's purpose is to clamp the gate of the IGBT device being driven by the Si828x to prevent IGBT turn on due to the collector $C_{CG}$ coupling.

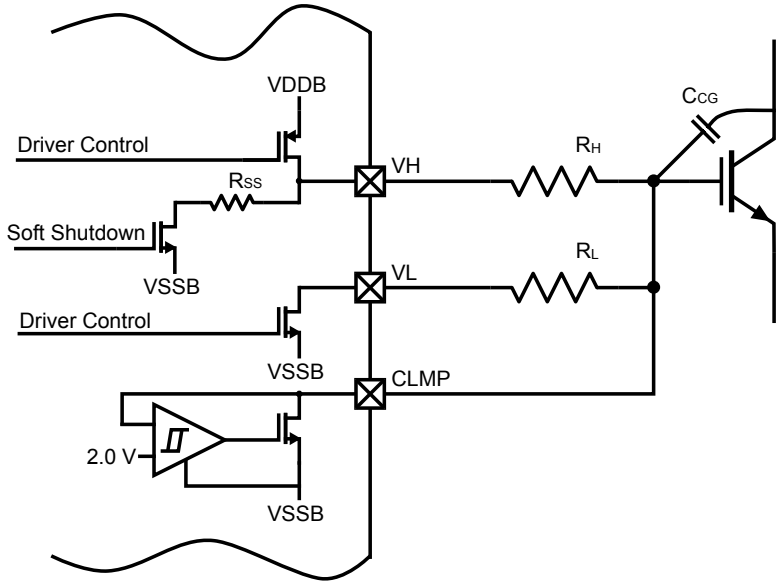



**Figure 2.4. Miller Clamp Device**

The Miller clamp device (Clamp) is engaged after the main driver had been on (VL) and pulled IGBT gate voltage close to VSSB, such that one can consider the IGBT being already off. This timing prevents the Miller clamp from interfering with the driver's operation. The engaging of the Miller Clamp is done by comparing the IGBT gate voltage with a 2.0 V reference (relative to VSSB) before turning on the Miller clamp NMOS.

# 3. Applications Information

The following sections detail the input and output circuits necessary for proper operation.

## 3.1 Recommended Application Circuits

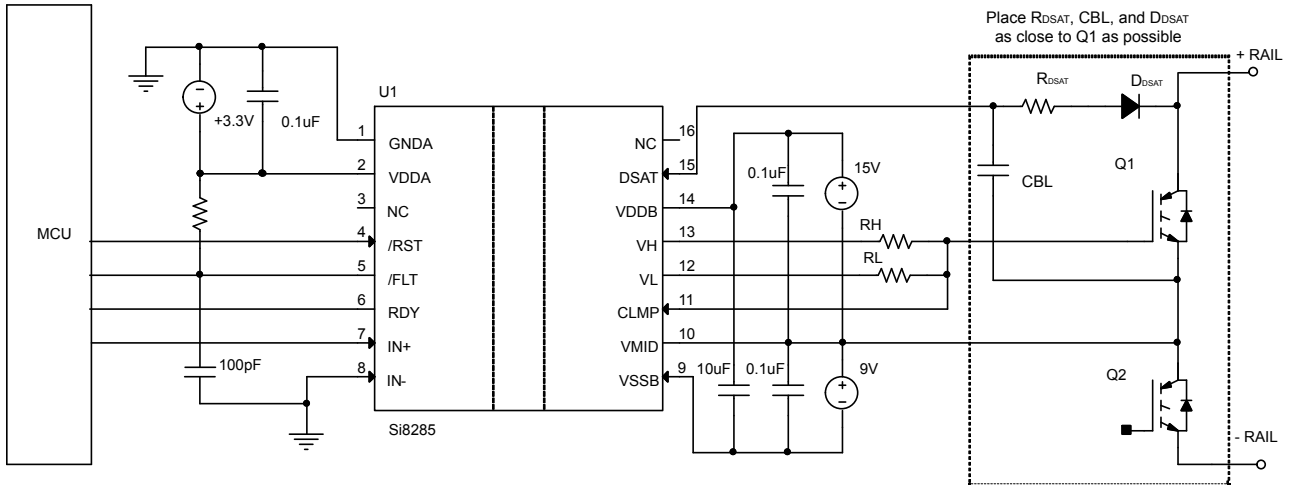



**Figure 3.1. Recommended Si8285 Application Circuit**

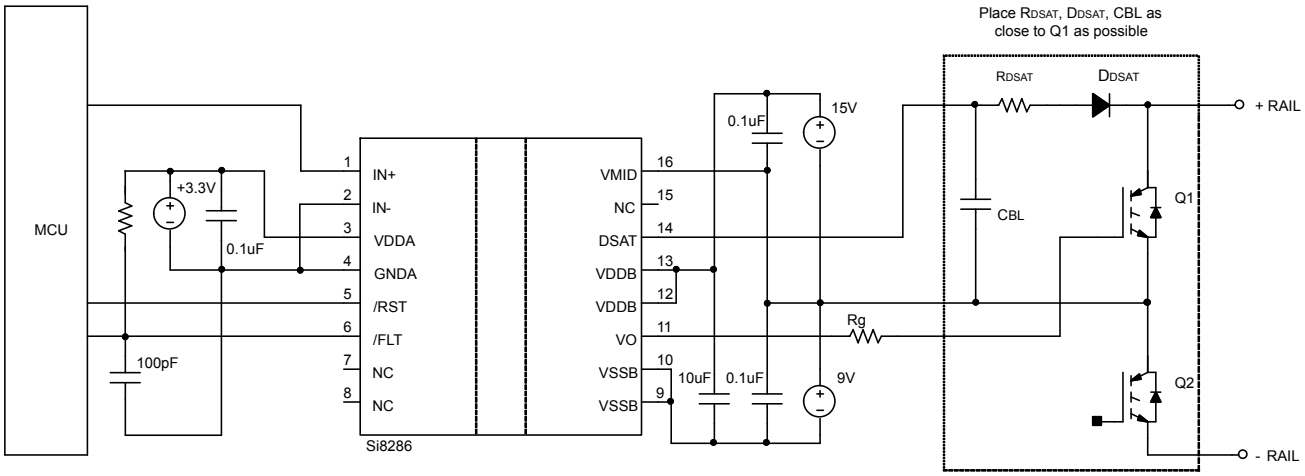



**Figure 3.2. Recommended Si8286 Application Circuit**

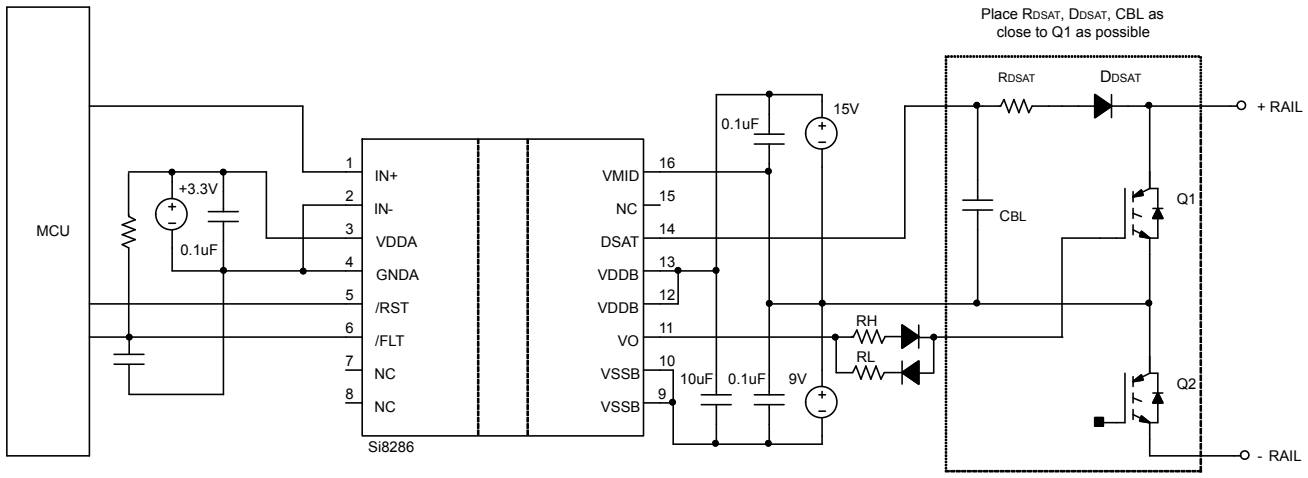



**Figure 3.3. Recommended Si8286 Application Circuit with RH and RL**

The Si828x has both inverting and non-inverting gate control inputs (IN– and IN+). In normal operation, one of the inputs is not used, and should be connected to GNDA (IN–) or VDDA (IN+) respectively for proper logic termination. The Si828s has an active low reset input (RSTb), an active high ready (RDY) push pull output, and an open drain fault (FLTb) output that requires a weak 10 kΩ pull-up resistor. The FLTb outputs from multiple Si828x devices can be connected in an OR wiring configuration to provide one single FLTb signal to the MCU. The Si828x gate driver will shut down when a fault is detected. It then provides FLTb indication to the MCU, and remains in the shutdown state until the MCU applies a reset signal.

To power the Si828x, the supply for VDDA should be able to handle 10 mA of current and the supplies to VDDB, and VSSB have to be able to handle 20 mA. Each supply should have 0.1 µF bypass capacitors to provide large switching transient current. The VSSB supply is optional but it operates better with the CLMP circuit to secure the IGBT in the off state against the collector to gate Miller current. VSSB should be shorted to VMID if VSSB supply is not available.

The desaturation sensing circuit consisted of the 100 pF blanking capacitor, 100 Ω current limiting resistor, and DSAT diode. These components provide current and voltage protection for the Si828x desaturation DSAT pin and it is critical to place these components as close to the IGBT as possible. Also, on the layout, make sure that the loop area forming between these components and the IGBT be minimized for optimum desaturation detection. The Si8285 has VH and VL gate drive outputs with external 10 Ω resistors to limit output gate current. The value of these resistors can be adjusted to independently control IGBT collector voltage rise and fall time. The Si8286 only has one VO gate drive output with an external 10 Ω resistor to control IGBT collector voltage rise and fall time. The CLMP output should be connected to the gate of the IGBT directly to provide clamping action between the gate and VSSB. This clamping action dissipates IGBT Miller current from collector to the gate to secure the IGBT in the off-state.

### 3.1.1 Power

To power the Si828x, the supply for VDDA should be able to handle 10 mA of current, the VDDB, and VSSB have to be able to handle the Si828x biasing current plus the average IGBT gate current drive (see 3.3 Power Dissipation Considerations). Each supply should have 0.1 µF bypass capacitor to provide large switching transient current in parallel with a 10 µF capacitor. The VSSB supply is optional, but it operates better with the CLMP circuit to secure the IGBT in the off state against the collector to gate Miller current. The VSSB pin should be shorted to VMID if VSSB supply is not available.

### 3.1.2 Inputs

The Si828x has both inverting and non-inverting gate control inputs (IN– and IN+). In normal operation, one of the inputs is not used and should be connected to GNDA (IN–) or VDDA (IN+) for proper logic termination. Inputs should be driven by CMOS level push-pull output. If input is driven by the MCU GPIO, it is recommended that the MCU be located as closed to the Si828x as possible to minimize PCB trace parasitic and noise coupling to the input circuit.

### 3.1.3 Reset, RDY, and Fault

The Si828x has an active high ready (RDY) push pull output, an open drain fault (FLTb) output, and an active low reset input (RSTb) that require pull-up resistors. Fast common-mode transients in high-power circuits can inject noise and glitches into these pins due to parasitic coupling. Depending on the IGBT power circuit layout, additional capacitance (100 pF to 470 pF) can be included on these pins to prevent faulty RDY and FLTb indications as well as unintended reset to the device.

The FLTb outputs from multiple Si828x devices can be connected in an OR wiring configuration to provide a single FLTb signal to the MCU.

The Si828x gate driver will shut down when a fault is detected. It then provides FLTb indication to the MCU and remains in the shut-down state until the MCU applies a reset signal.

### 3.1.4 Desaturation

The desaturation sensing circuit consists of the blanking capacitor (100 pF for Si8286 and 390 pF for Si8285), 100 Ω current limiting resistor, and DSAT diode. These components provide current and voltage protection for the Si828x desaturation DSAT pin, and it is critical to place these components as close to the IGBT as possible. Also, on the layout, make sure that the loop area forming between these components and the IGBT is minimized for optimum desaturation detection.

### 3.1.5 Driver Outputs

The Si8285 has VH and VL gate drive outputs (see Figure 3.1 Recommended Si8285 Application Circuit on page 7). They work with external RH and RL resistors to limit output gate current. The value of these resistors can be adjusted to independently control IGBT collector voltage rise and fall time. The Si8286 only has one VO gate drive output with an external gate resistor to control IGBT collector voltage rise and fall time (see Figure 3.2 Recommended Si8286 Application Circuit on page 7). To achieve independent rise and fall time control, it is suggested to add a pair of fast diodes to the Si8286 VO circuit (see Figure 3.3 Recommended Si8286 Application Circuit with RH and RL on page 8).

The CLMP output should be connected to the gate of the IGBT directly to provide clamping action between the gate and VSSB pin. This clamping action dissipates IGBT Miller current from the collector to the gate to secure the IGBT in the off-state. Negative VSSB provides further help to ensure the gate voltage stays below the IGBT's Vth during the off state.

## 3.2 Layout Considerations

It is most important to minimize ringing in the drive path and noise on the supply lines. Care must be taken to minimize parasitic inductance in these paths by locating the Si828x as close as possible to the device it is driving. In addition, the supply and ground trace paths must be kept short. For this reason, the use of power and ground planes is highly recommended. A split ground plane system having separate ground and power planes for power devices and small signal components provides the best overall noise performance.

### 3.3 Power Dissipation Considerations

Proper system design must assure that the Si828x operates within safe thermal limits across the entire load range. The Si828x total power dissipation is the sum of the power dissipated by bias supply current, internal parasitic switching losses, and power dissipated by the series gate resistor and load. Equation 1 shows total Si828x power dissipation.

$$PD = (VDDA)(IDDA) + (VDDB)(IDDB) + f \times Q_{int} \times VDDB + \frac{1}{2}(f)(Q_{IGBT})(VDDB)\left[\frac{Rp}{Rp + RH} + \frac{Rn}{Rn + RL}\right]$$

where:

PD is the total Si828x device power dissipation (W).

IDDA is the input-side maximum bias current (5 mA).

IDDB is the driver die maximum bias current (5 mA).

$Q_{int}$ is the internal parasitic charge (3 nC).

VDDA is the input-side VDD supply voltage (2.7 to 5.5 V).

VDDB is the total driver-side supply voltage (VDDB + VSSB: 12.5 to 30 V).

f is the IGBT switching frequency (Hz).

RH is the VH external gate resistor, RL is the VL external gate resistor. For Si8286, RG works for both RH and RL.

RP is the $RDS_{(ON)}$ of the driver pull-up switch: (2.6 Ω).

Rn is the $RDS_{(ON)}$ of the driver pull-down switch: (0.8 Ω).

**Equation 1**

The maximum power dissipation allowable for the Si828x is a function of the package thermal resistance, ambient temperature, and maximum allowable junction temperature, as shown in Equation 2:

$$PD\text{max} \leq \frac{Tj\text{max} - TA}{\theta ja}$$

where:

PDmax = Maximum Si828x power dissipation (W).

Tjmax = Si823x maximum junction temperature (150 °C).

TA = Ambient temperature (°C)

θja = Si828x junction-to-air thermal resistance (60 °C/W for four-layer PCB)

f = Si828x switching frequency (Hz)

**Equation 2**

Substituting values for PDmax Tjmax (150 °C), TA (125 °C), and θja (90 °C/W) into Equation 2 results in a maximum allowable total power dissipation of 0.42 W.

$$PD\text{max} \leq \frac{150 - 125}{60} = 0.42W$$

Maximum allowable load is found by substituting this limit and the appropriate data sheet values from Table 4.1 into Equation 1 and simplifying. The result is Equation 3.

$$PD = (VDDA)(IDDA) + (VDDB)(IDDB) + f \times Q\text{int} \times VDDB + \frac{1}{2}(f)(Q_L)(VDDB)\left[\frac{Rp}{Rp + RH} + \frac{Rn}{Rn + RL}\right]$$

$$PD = (VDDA)(IDDA) + (VDDB)(IDDB) + f \times Q\text{int} \times VDDB + \frac{1}{2}\left(f\right)\left(C_L\right)\left(VDDB^2\right)\left[\frac{Rp}{Rp + RH} + \frac{Rn}{Rn + RL}\right]$$

$$0.42 = (VDDA)(0.005) + (VDDB)(0.004) + f \times 3 \times 10^{-9} \times VDDB + \frac{1}{2}\left(f\right)\left(C_L\right)\left(VDDB^2\right)\left[\frac{2.6}{2.6 + 15} + \frac{0.8}{0.8 + 10}\right]$$

$$0.42 - (VDDA + VDDB)5 \times 10^{-3} - f \times 3 \times 10^{-9} \times VDDB = 0.111VDDB^2 f\left(C_L\right)$$

$$C_L = \frac{0.42 - (VDDA + VDDB)5 \times 10^{-3}}{0.111 \times VDDB^2(f)} - \frac{2.703 \times 10^{-8}}{VDDB}$$

**Equation 3**

Power dissipation example for Si828x driver using Equation 1 with the following givens:

$V_{DDA}$ = 5.0 V

$V_{DDB}$ = 18 V

f = 30 kHz

$R_H$ = 10 Ω

$R_L$ = 15 Ohms

$Q_G$ = 85 nC

$$PD = (5)(0.005) + (15)(0.005) + (2 \times 10^4)(3 \times 10^{-9})(18) + \frac{1}{2}(2 \times 10^4)(25 \times 10^{-9})(18)\left[\frac{2.6}{2.6 + 10} + \frac{0.8}{0.8 + 15}\right] = 100mW$$

From which the driver junction temperature is calculated using Equation 2, where:

Pd is the total Si828x device power dissipation (W)

θja is the thermal resistance from junction to air (60 °C/W in this example)

TA is the maximum ambient temperature (125 °C)

$$Tj = Pd \times \theta ja + TA$$

$$Tj = (0.1) \times (90) + 125 = 134°C$$

Calculate maximum loading capacitance from equation 3:

1. VDDA = 5 V and VDDB = 12.5 V.

$$C_L = \frac{1.92 \times 10^{-2}}{f} - 2.16 \times 10^{-9}$$

2. VDDA = 5 V and VDDB = 18 V.

$$C_L = \frac{8.48 \times 10^{-3}}{f} - 1.5 \times 10^{-9}$$

3. VDDA = 5 V and VDDB = 30 V.

$$C_L = \frac{2.45 \times 10^{-3}}{f} - 9.01 \times 10^{-10}$$

Graphs are shown in the following figure. All points along the load lines in these graphs represent the package dissipation-limited value of $C_L$ for the corresponding switching frequency.

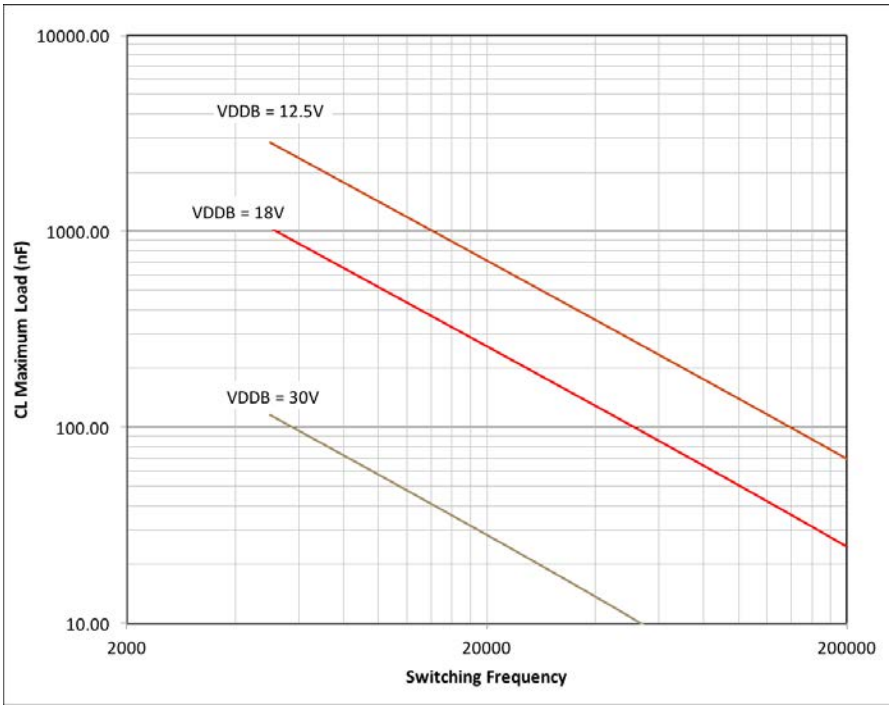



**Figure 3.4. Maximum Load vs. Switching Frequency (25 °C)**

# 4. Electrical Specifications

**Table 4.1. Electrical Specifications**

$V_{IN}$ = 24 V; $V_{DDA}$ = 4.3 V (See Figure 3) for all Si8282/84; $V_{DDA}$ = $V_{DDP}$ = 3.0 to 5.0 V (See Figure 2) for all Si8281/83; $T_A$ = –40 to +125 °C unless otherwise noted.

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **DC Parameters** | | | | | | |
| Input Supply Voltage | VDDA | | 2.8 | — | 5.5 | V |
| Power Input Voltage | VDDP | | 3.0 | — | 5.5 | V |
| Driver Supply Voltage | (VDDB – VSSB) | | 9.5 | — | 30 | V |
| | (VMID – VSSB) | | 0 | — | 15 | V |
| Input Supply Quiescent Current | IDDA(Q) | | — | 2.6 | 3.7 | mA |
| Input Supply Active Current | IDDA | f = 10 kHz | — | 5.2 | — | mA |
| Output Supply Quiescent Current (Si8285) | IDDB(Q) | | — | 5.3 | 6.5 | mA |
| Output Supply Quiescent Current (Si8286) | | | — | 3.5 | 4.5 | mA |
| **Drive Parameters** | | | | | | |
| High Drive Transistor RDS(ON) | $R_{OH}$ | | — | 2.48 | — | Ω |
| Low Drive Transistor RDS(ON) | $R_{OL}$ | | — | 0.86 | — | Ω |
| High Drive Peak Output Current | $I_{OH}$ | VH = VDDB – 15 V<br>$T_{PW_IOH}$ ≤ 250 ns | 2.5 | 2.8 | — | A |
| Low Drive Peak Output Current | $I_{OL}$ | VL = VSSB + 6.0 V<br>$T_{PW_IOL}$≤ 250 ns | 3.0 | 3.4 | — | A |
| **UVLO Parameters** | | | | | | |
| UVLO Threshold + | $VDDA_{UV+}$ | | 2.4 | 2.7 | 3.0 | |
| UVLO Threshold – | $VDDA_{UV–}$ | | 2.3 | 2.6 | 2.9 | |
| UVLO Lockout Hysteresis– (Input Side) | $VDDA_{HYS}$ | | — | 100 | — | mV |
| UVLO Threshold + (Driver Side)<br>9 V Threshold (Si828xBD)<br>12 V Threshold (Si828xCD) | $VDDB_{UV+}$ | | <br>8.0<br>10.8 | <br>9.0<br>12.0 | <br>10.0<br>13.2 | <br>V<br>V |
| UVLO Threshold – (Driver Side)<br>9 V Threshold (Si828xBD)<br>12 V Threshold (Si828xCD) | $VDDB_{UV–}$ | | <br>7.0<br>9.8 | <br>8.0<br>11.0 | <br>9.0<br>12.2 | <br>V<br>V |
| UVLO lockout hysteresis (Driver Side) | $VDDB_{HYS}$ | | — | 1 | — | V |
| UVLO+ to RDY High Delay | $t_{UVLO+ \text{ to RDY}}$ | | — | | 100 | µs |
| ULVO– to RDY Low Delay | $t_{UVLO– \text{ to RDY}}$ | | — | | 0.79 | µs |
| **Desaturation Detector Parameters** | | | | | | |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| DESAT Threshold | VDESAT | VDDB – VSSB > VDDBUV+ | 6.5 | 6.9 | 7.3 | V |
| $C_{BI}$ charging current (Si8285) | $I_{Chg}$ | | — | 1 | — | mA |
| $C_{BI}$ charging current (Si8286) | | | — | 0.25 | — | mA |
| DESAT Sense to 90% VOUT Delay | $t_{DESAT(90\%)}$ | | — | 220 | 300 | ns |
| DESAT Sense to 10% VOUT Delay | $t_{DESAT(10\%)}$ | | 0.77 | 2.5 | 2.7 | µs |
| DESAT Sense to FLT Low Delay | $t_{DESAT\ to\ FLT}$ | | — | 220 | 300 | ns |
| Reset to FLT High Delay | $t_{RST\ to\ FLT}$ | | — | 37 | 45 | ns |
| **Miller Clamp Parameters (Si8285 Only)** | | | | | | |
| Clamp Pin Threshold Voltage | $V_t$ Clamp | | — | 2.0 | — | V |
| Miller Clamp Transistor RDS (ON) | $R_{MC}$ | | — | 1.07 | — | Ω |
| Clamp Low Level Sinking Current | $I_{CL}$ | VCLMP = VSSB + 6.0 | 3.0 | 3.4 | — | A |
| **Digital Parameters** | | | | | | |
| Logic High Input Threshold | VIH | | 2.0 | — | — | V |
| Logic Low Input Threshold | VIL | | — | — | 0.8 | V |
| Input Hysteresis | VIHYST | | — | 440 | — | mV |
| High Level Output Voltage (RDY pin only) | VOH | IO = –4 mA | VDDA – 0.4 | — | — | V |
| Low Level Output Voltage (RDY pin only) | VOL | IO = 4 mA | — | — | 0.4 | V |
| Open-Drain Low Level Output Voltage (FLT pin only) | | VDDA = 5 V, 5 kΩ pull-up resistor | — | — | 200 | mV |
| **AC Switching Parameters** | | | | | | |
| Propagation Delay (Low-to-High) | $t_{PLH}$ | CL = 200 pF | 30 | 40 | 50 | ns |
| Propagation Delay (High-to-Low) | $t_{PHL}$ | CL = 200 pF | 30 | 40 | 50 | ns |
| Pulse Width Distortion | PWD | $\lvert t_{PLH} - t_{PHL} \rvert$ | — | 1 | 5 | ns |
| Propagation Delay Difference[4] | PDD | $t_{PHLMAX} - t_{PLHMIN}$ | –1 | — | 25 | ns |
| Rise Time | $t_R$ | CL = 200 pF | — | 5.5 | 15 | ns |
| Fall Time | $t_F$ | CL = 200 pF | — | 8.5 | 20 | ns |
| Common Mode Transient Immunity | | Output = low or high (VCM = 1500 V) | 35 | 50 | — | kV/µs |

1. See 1. Ordering Guide for more information.
2. Minimum value of (VDD – GND) decoupling capacitor is 1 µF.
3. When performing this test, it is recommended that the DUT be soldered to avoid trace inductances, which may cause overstress conditions.
4. Guaranteed by characterization.

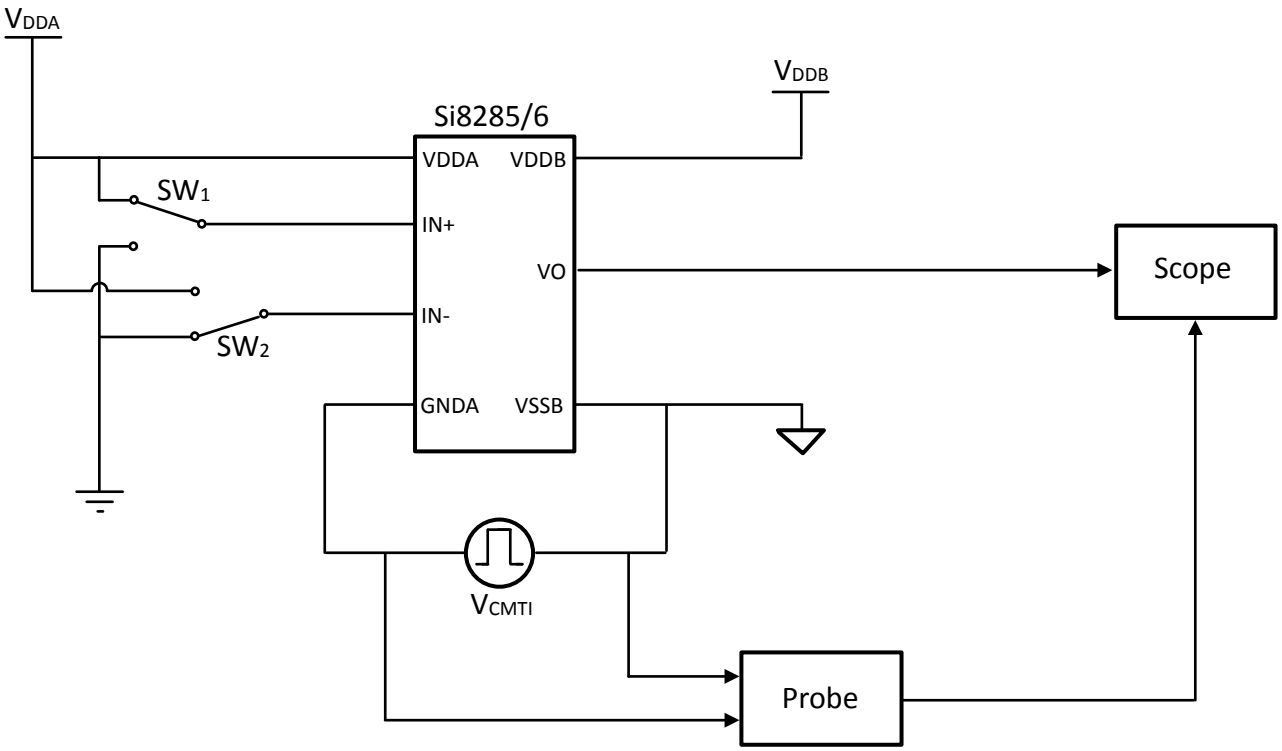



**Figure 4.1. Common-Mode Transient Immunity Characterization Circuit**

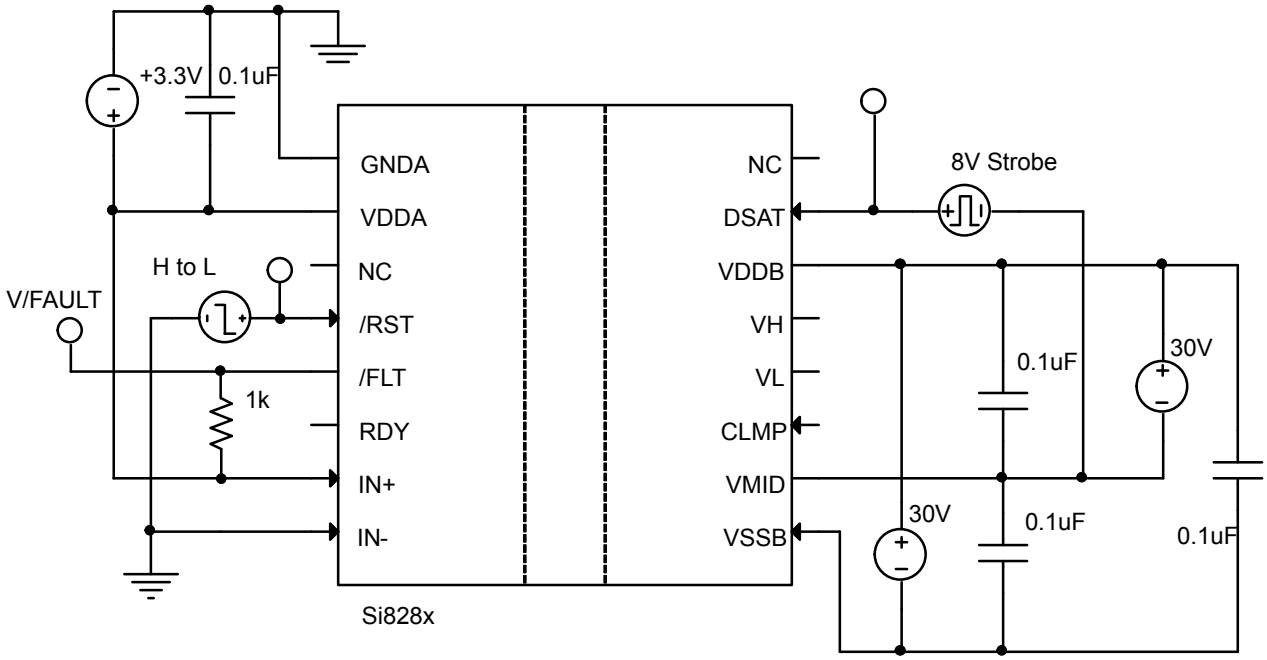



**Figure 4.2. Si828x RST FLT CLEAR Test Circuit**

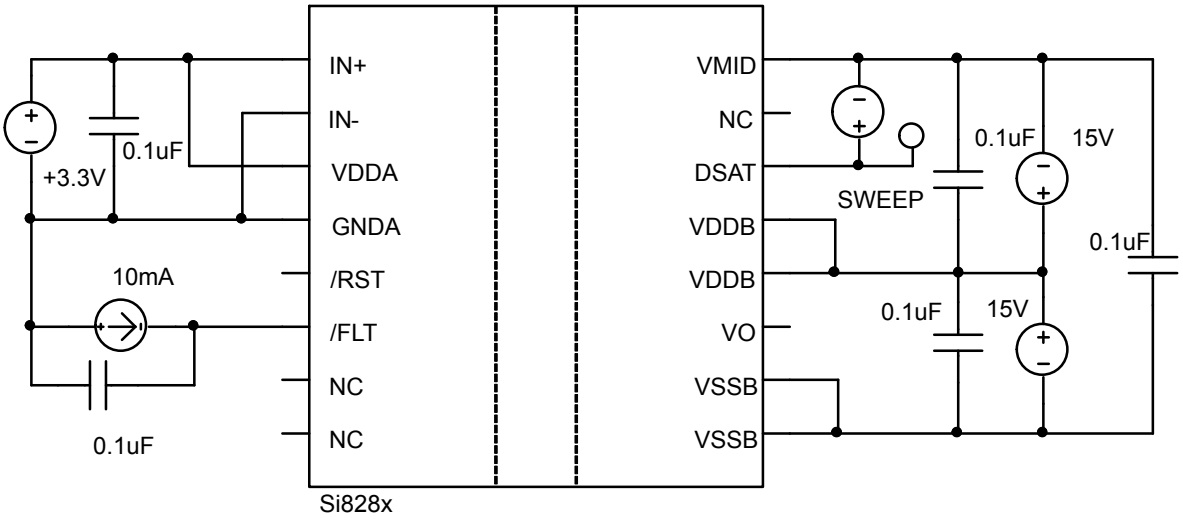



**Figure 4.3. Si828x DSAT Threshold Test Circuit**

**Table 4.2. Absolute Maximum Ratings[1]**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Storage Temperature | $T_{STG}$ | –65 | +150 | °C |
| Operating Temperature | $T_A$ | –40 | +125 | °C |
| Junction Temperature | $T_J$ | — | +140 | °C |
| Peak Output Current ($t_{PW}$ = 10 µs) | $I_{OPK}$ | — | 4.0 | A |
| Supply Voltage | VDD | –0.5 | 36 | V |
| Output Voltage | $V_{OUT}$ | –0.5 | 36 | V |
| Input Power Dissipation | $P_I$ | — | 100 | mW |
| Output Power Dissipation | $P_O$ | — | 800 | mW |
| Total Power Dissipation (All Packages Limited by Thermal Derating Curve) | $P_T$ | — | 900 | mW |
| Lead Solder Temperature (10 s) | | — | 260 | °C |
| HBM Rating ESD | | 4 | — | kV |
| Machine Model ESD | | 300 | — | V |
| CDM | | 2000 | — | V |
| Maximum Isolation (Input to Output) (1 sec) WB SOIC-16 | | — | 6500 | $V_{RMS}$ |

**Note:**

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### 4.1 Timing Diagrams

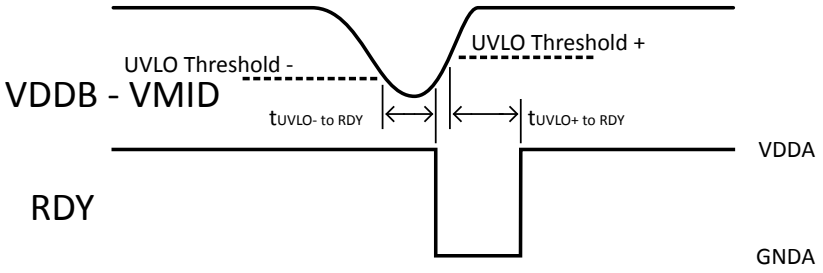



**Figure 4.4. UVLO Condition to RDY Output**

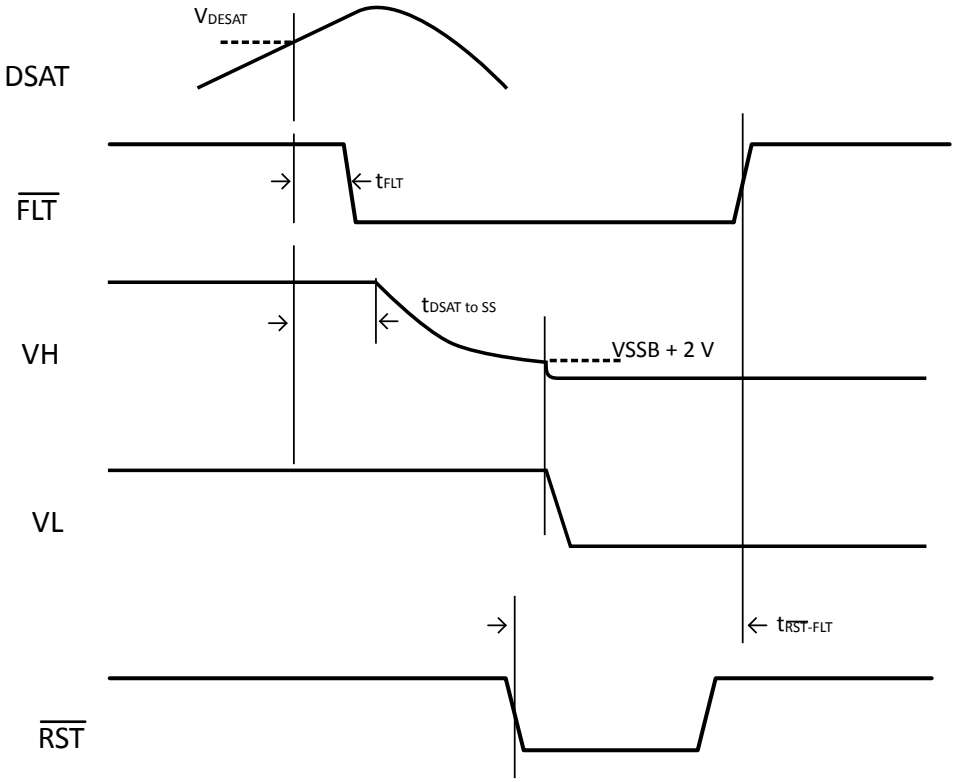
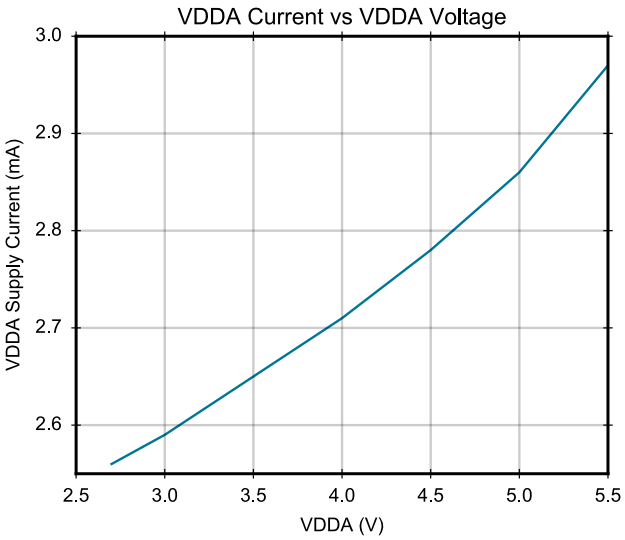
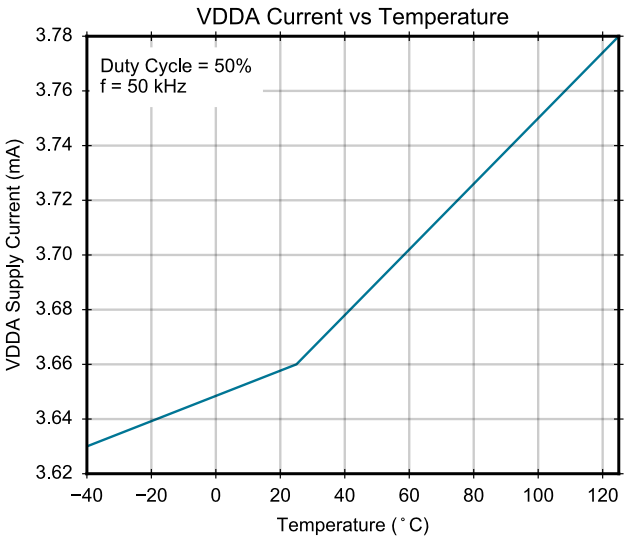
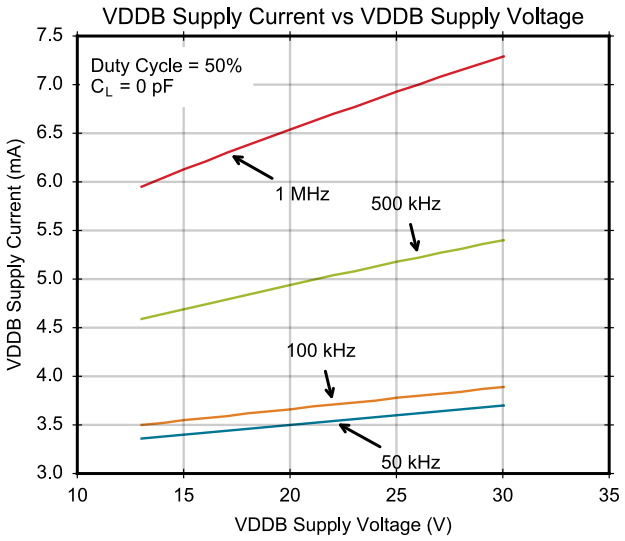


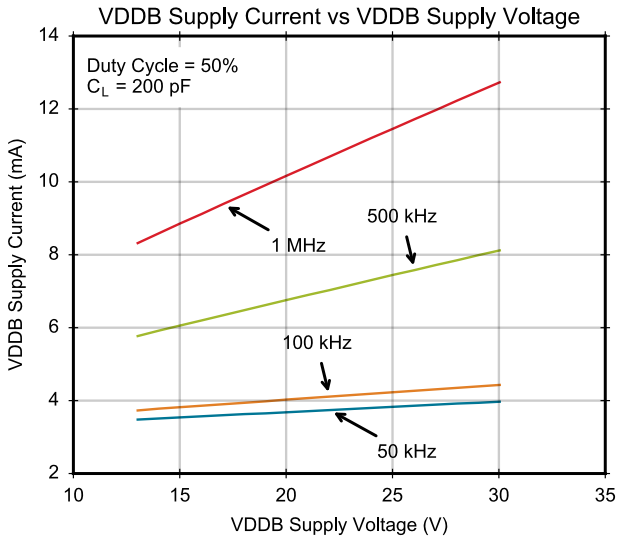

**Figure 4.5. Device Reaction to Desaturation Event**

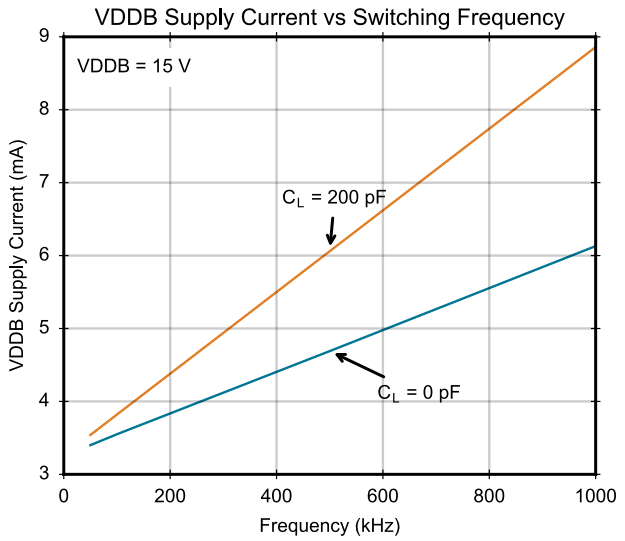
## 4.2 Typical Operating Characteristics

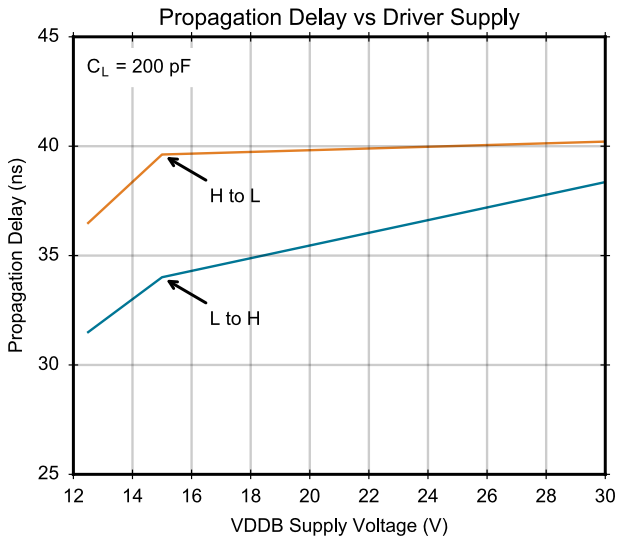


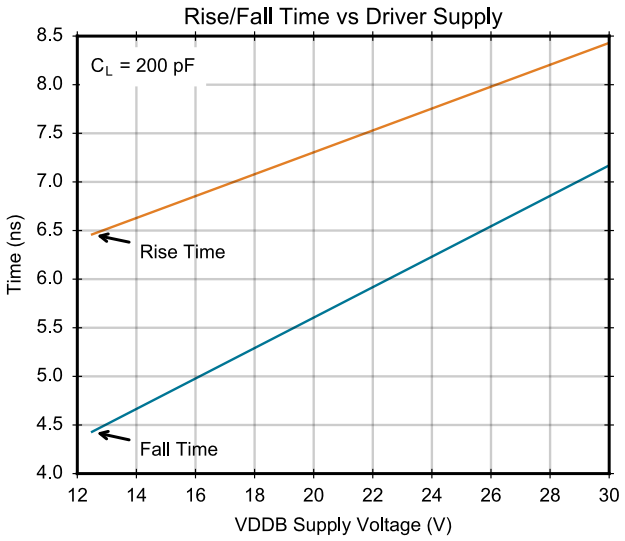



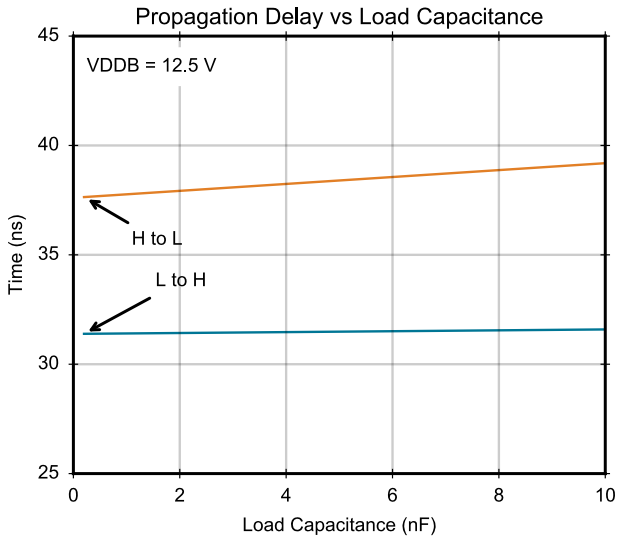



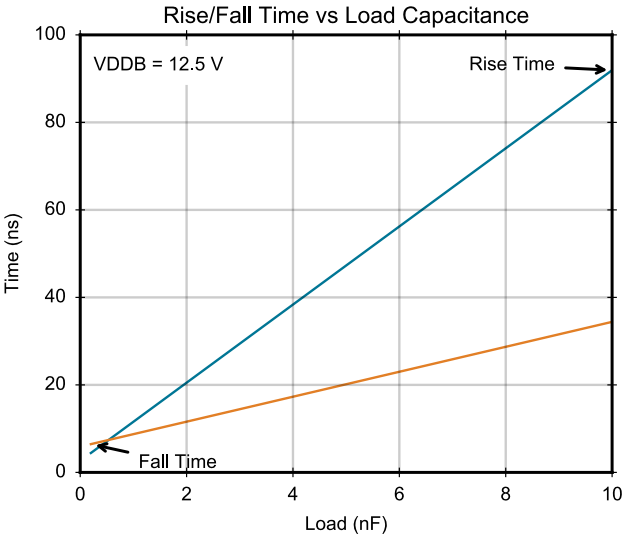



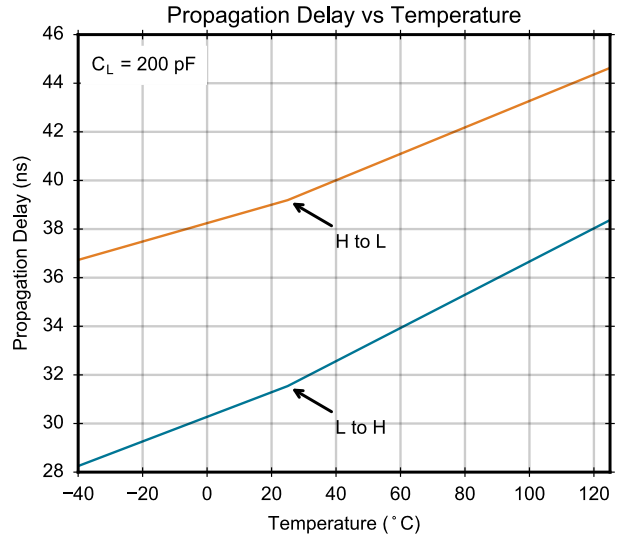



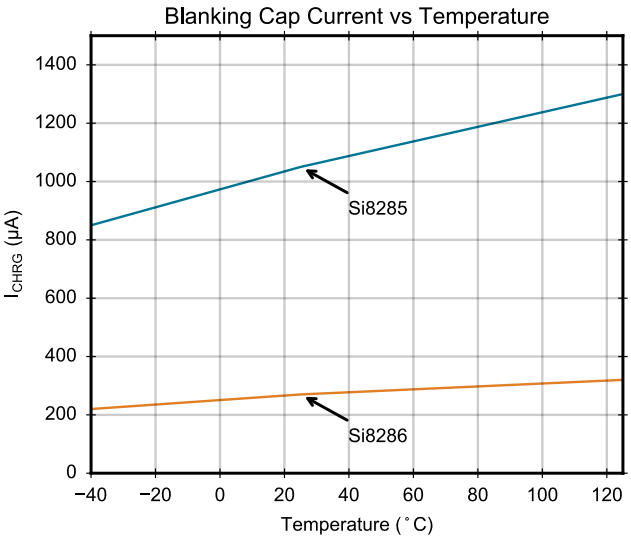



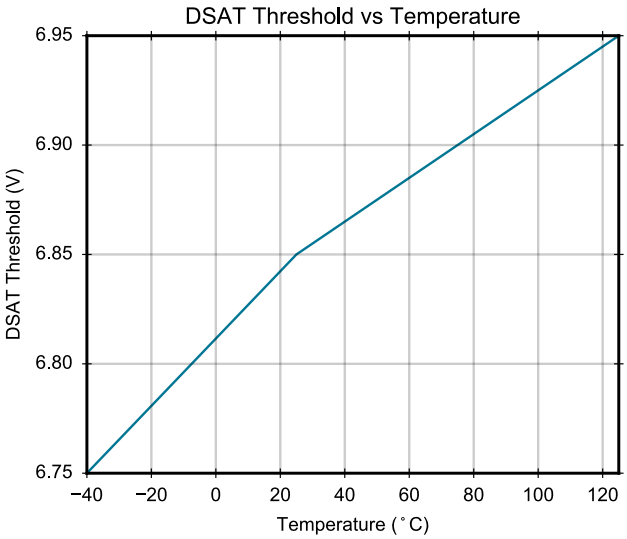

Rise/Fall Time vs Driver Supply
$C_L$ = 200 pF
Rise Time
Fall Time
Time (ns)
VDDB Supply Voltage (V)

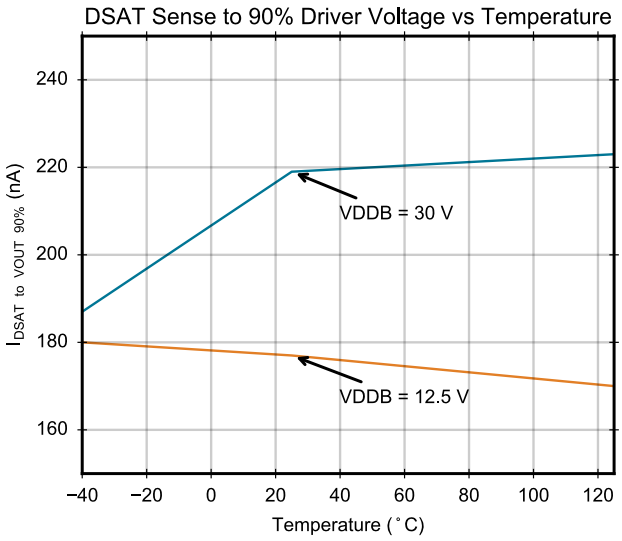

Propagation Delay vs Load Capacitance
VDDB = 12.5 V
H to L
L to H
Time (ns)
Load Capacitance (nF)

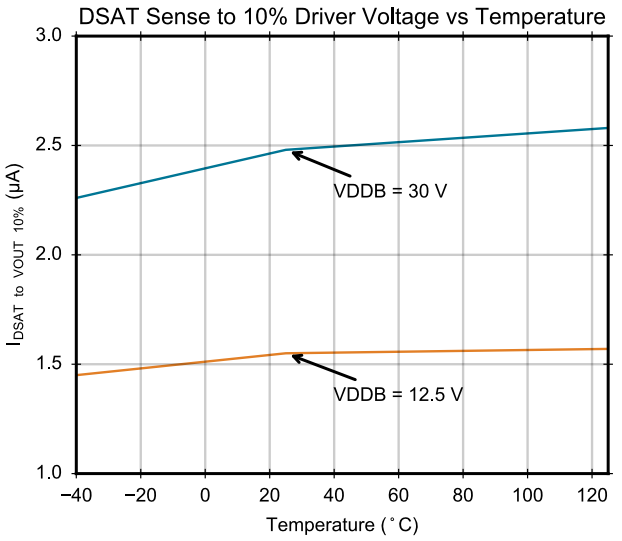

Rise/Fall Time vs Load Capacitance
VDDB = 12.5 V
Rise Time
Fall Time
Time (ns)
Load (nF)

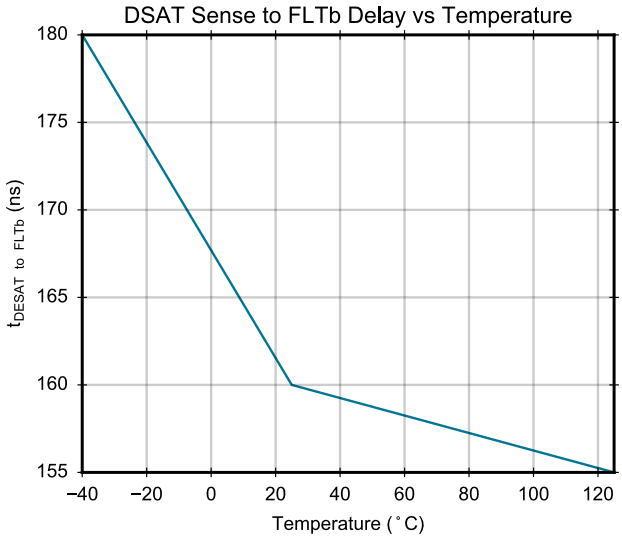

Propagation Delay vs Temperature
$C_L$ = 200 pF
H to L
L to H
Propagation Delay (ns)
Temperature (˚C)

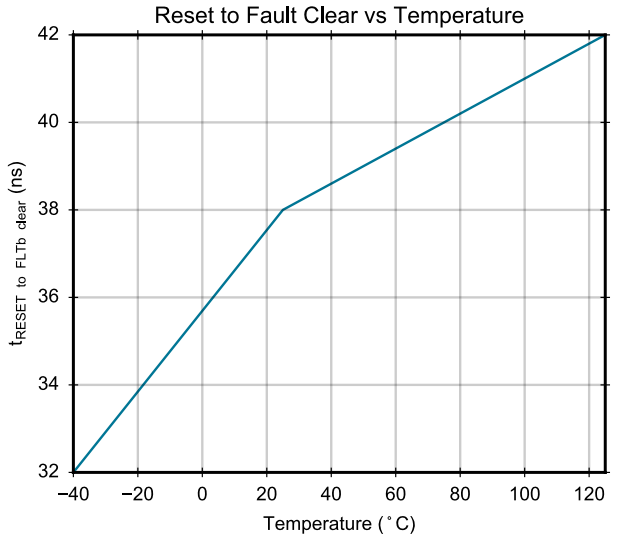

Blanking Cap Current vs Temperature
Si8285
Si8286
$I_{CHRG}$ (µA)
Temperature (˚C)


DSAT Threshold vs Temperature
DSAT Threshold (V)
Temperature (˚C)


DSAT Sense to 90% Driver Voltage vs Temperature
240
220
200
180
160
IDSAT to VOUT 90% (nA)
VDDB = 30 V
VDDB = 12.5 V
−40
−20
0
20
40
60
80
100
120
Temperature (˚C)


DSAT Sense to 10% Driver Voltage vs Temperature
3.0
2.5
2.0
1.5
1.0
IDSAT to VOUT 10% (µA)
VDDB = 30 V
VDDB = 12.5 V
−40
−20
0
20
40
60
80
100
120
Temperature (˚C)


DSAT Sense to FLTb Delay vs Temperature
180
175
170
165
160
155
tDESAT to FLTb (ns)
−40
−20
0
20
40
60
80
100
120
Temperature (˚C)


Reset to Fault Clear vs Temperature
42
40
38
36
34
32
tRESET to FLTb clear (ns)
−40
−20
0
20
40
60
80
100
120
Temperature (˚C)

### 4.3 Regulatory Information

**Table 4.3. Regulatory Information (Pending)[1, 2]**

| |
|---|
| **CSA** |
| The Si828x is certified under CSA Component Acceptance Notice 5A. For more details, see File 232873. |
| 60950-1: Up to 600 $V_{RMS}$ reinforced insulation working voltage; up to 1000 $V_{RMS}$ basic insulation working voltage. |
| **VDE** |
| The Si828x is certified according to VDE0884. For more details, see File 5006301-4880-0001. |
| VDE 0884-10: Up to 1414 $V_{peak}$ for reinforced insulation working voltage. |
| **UL** |
| The Si828x is certified under UL1577 component recognition program. For more details, see File E257455. |
| Rated up to 5000 $V_{RMS}$ isolation voltage for basic protection. |
| **CQC** |
| The Si828x is certified under GB4943.1-2011. |
| Rated up to 600 $V_{RMS}$ reinforced insulation working voltage; up to 1000 $V_{RMS}$ basic insulation working voltage. |
| **Note:**<br>1. Regulatory Certifications apply to 5.0 $kV_{RMS}$ rated devices, which are production tested to 6.0 $kV_{RMS}$ for 1 sec.<br>2. For more information, see 1. Ordering Guide. |

**Table 4.4. Insulation and Safety-Related Specifications**

| Parameter | Symbol | Test Condition | Value | Unit |
|---|---|---|---|---|
| | | | WB SOIC-16 | |
| Nominal Air Gap (Clearance)[1] | L(1O1) | | 8.0 | mm |
| Nominal External Tracking (Creepage) | L(1O2) | | 8.0 | mm |
| Minimum Internal Gap (Internal Clearance) | | | 0.016 | mm |
| Tracking Resistance (Proof Tracking Index) | PTI | IEC60112 | 600 | V |
| Erosion Depth | ED | | 0.019 | mm |
| Resistance (Input-Output)[2] | $R_{IO}$ | | $10^{12}$ | Ω |
| Capacitance (Input-Output)[2] | $C_{IO}$ | f = 1 MHz | 1 | pF |

**Note:**

1. The values in this table correspond to the nominal creepage and clearance values as detailed in PACKAGE OUTLINE: 16-PIN WIDE BODY SOIC. VDE certifies the clearance and creepage limits as 8.5 mm minimum for the WB SOIC-16. UL does not impose a clearance and creepage minimum for component level certifications. CSA certifies the clearance and creepage limits as 7.6 mm minimum for the WB SOIC-16 package.
2. To determine resistance and capacitance, the Si828x is converted into a 2-terminal device. Pins 1–8 are shorted together to form the first terminal, and pins 9–16 are shorted together to form the second terminal. The parameters are then measured between these two terminals.

**Table 4.5. IEC 60664-1 Ratings**

| Parameter | Test Condition | Specification |
|---|---|---|
| | | WB SOIC-16 |
| Basic Isolation Group | Material Group | I |
| Installation Classification | Rated Mains Voltages ≤ 150 $V_{RMS}$ | I-IV |
| | Rated Mains Voltages ≤ 300 $V_{RMS}$ | I-IV |
| | Rated Mains Voltages ≤ 600 $V_{RMS}$ | I-IV |

**Table 4.6. VDE0884-10 Insulation Characteristics[1]**

| Parameter | Symbol | Test Condition | Characteristic | Unit |
|---|---|---|---|---|
| | | | WB SOIC-16 | |
| Maximum Working Insulation Voltage | $V_{IORM}$ | | 1414 | V peak |
| Input to Output Test Voltage | $V_{PR}$ | Method b1 ($V_{IORM}$ x 1.875 = $V_{PR}$, 100% Production Test, $t_m$ = 1 sec, Partial Discharge < 5 pC) | 2652 | V peak |
| Transient Overvoltage | $V_{IOTM}$ | t = 60 sec | 8000 | V peak |
| Surge Voltage | $V_{IOSM}$ | Tested per IEC 60065 with surge voltage of 1.2 µs/50 µs with magnitude 6250 V x 1.6 = 10 kV | 6250 | kV peak |
| Pollution Degree (DIN VDE 0110) | | | 2 | |
| Insulation Resistance at $T_S$, $V_{IO}$ = 500 V | $R_S$ | | $>10^9$ | Ω |

**Note:**
1. This isolator is suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The Si828x provides a climate classification of 40/125/21.

**Table 4.7. IEC Safety Limiting Values[1, 2]**

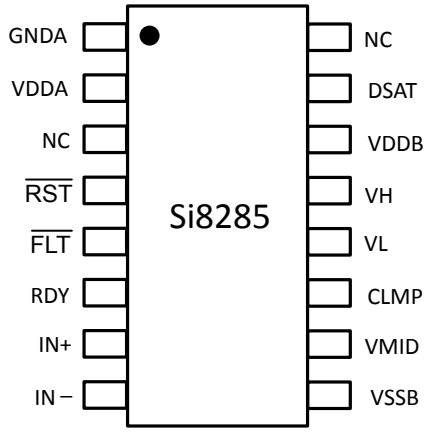
| Parameter | Symbol | Test Condition | Max | Unit |
|---|---|---|---|---|
| | | | WB SOIC-16 | |
| Case Temperature | $T_S$ | | 150 | °C |
| Input Current | $I_S$ | $\theta_{JA}$ = 60 °C/W<br>$V_{DDA}$ = 5.5 V, $V_{DDB}$–$V_{SSB}$ = 30 V<br>$T_J$ = 150 °C, $T_A$ = 25 °C | 30 | mA |
| Device Power Dissipation | $P_D$ | | 0.9 | W |

**Note:**
1. Maximum value allowed in the event of a failure.
2. The Si828x is tested with $R_H$ = $R_L$ = 0 Ω, $C_L$ = 5 nF, and a 200 kHz, 50% duty cycle square wave input.

**Table 4.8. Thermal Characteristics**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| | | WB SOIC-16 | |
| IC Junction-to-Air Thermal Resistance | $\theta_{JA}$ | 60 | °C/W |

## 5. Pin Descriptions



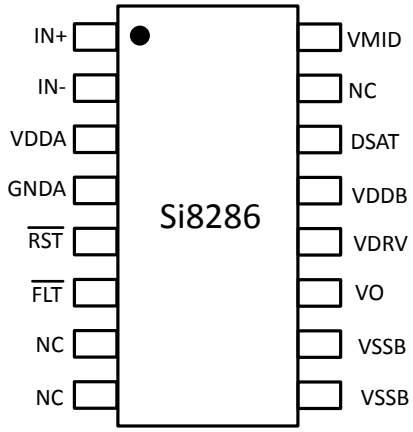




**Table 5.1. Si8285/86 Pin Descriptions**

| Name | Si8285 Pin # | Si8286 Pin # | Description |
|---|---|---|---|
| GNDA | 1 | 4 | Input side ground |
| VDDA | 2 | 3 | Input side power supply |
| RSTb | 4 | 5 | Reset fault condition pin |
| FLTb | 5 | 6 | Driver fault condition signal |
| RDY | 6 | — | UVLO ready signal |
| IN+ | 7 | 1 | Driver control complementary input (+) |
| IN– | 8 | 2 | Driver control complementary input (–) |
| VSSB | 9 | 9, 10 | Driver output side ground |
| VMID | 10 | 16 | IGBT source reference |
| CLMP | 11 | — | Miller clamp drain |
| VL | 12 | — | Pull-low driver output |
| VH | 13 | — | Pull-high driver output |
| VO | — | 11 | Driver output |
| VDDB | 14 | 12, 13 | Driver output power supply |
| DSAT | 15 | 14 | Desaturation detection sensor input |
| VDRV | — | 12 | Driver output supply |
| NC[1] | 16 | 7, 8, 15 | No Connect |

**Note:**

1. No Connect. These pins may be internally connected. To maximize CMTI performance, these pins should be connected to the ground plane.

# 6. Packaging

## 6.1 Package Outline: 16-Pin Wide Body SOIC

The figure below illustrates the package details for the Si828x in a 16-Pin Wide Body SOIC. The table lists the values for the dimensions shown in the illustration.

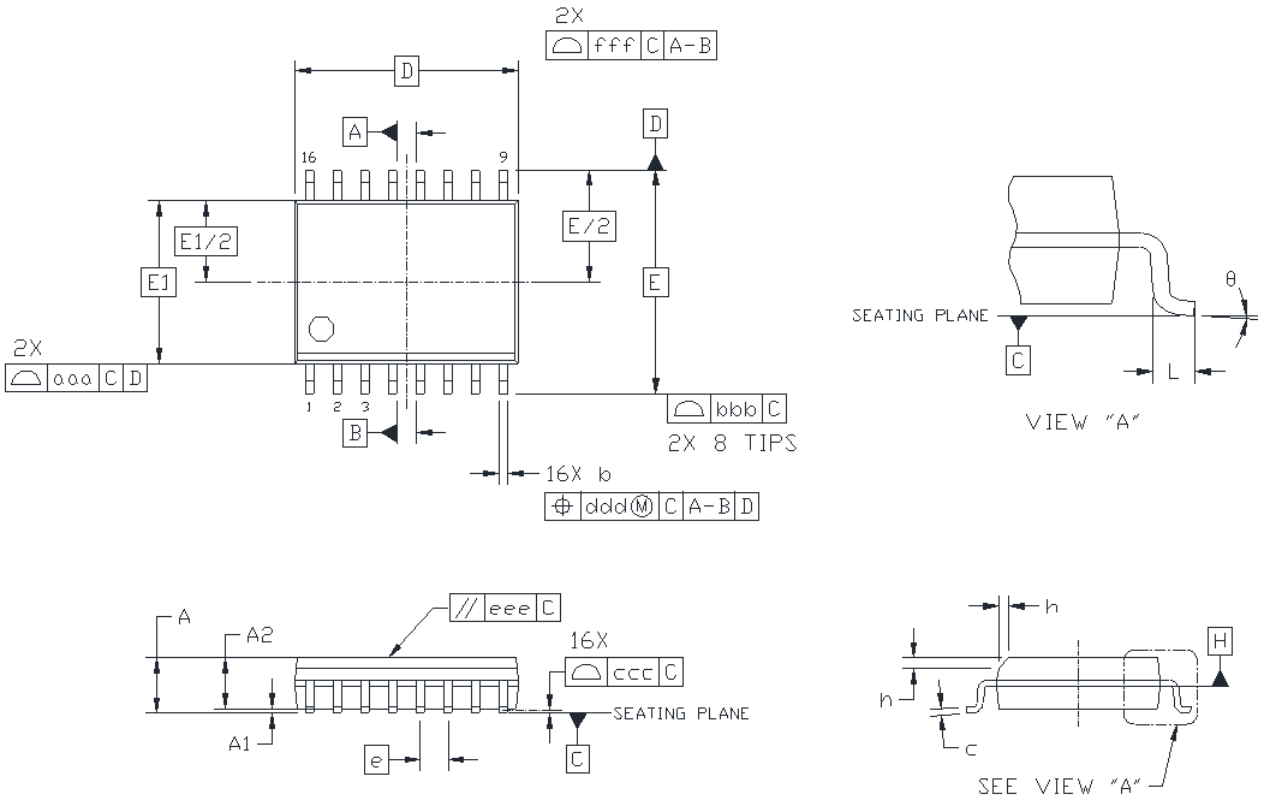



**Figure 6.1. 16-Pin Wide Body SOIC**

| Symbol | Millimeters | |
|---|---|---|
| | Min | Max |
| A | — | 2.65 |
| A1 | 0.10 | 0.30 |
| A2 | 2.05 | — |
| b | 0.31 | 0.51 |
| c | 0.20 | 0.33 |
| D | 10.30 BSC | |
| E | 10.30 BSC | |
| E1 | 7.50 BSC | |
| e | 1.27 BSC | |
| L | 0.40 | 1.27 |
| h | 0.25 | 0.75 |
| θ | 0° | 8° |
| aaa | — | 0.10 |

| Symbol | Millimeters | |
|---|---|---|
| | Min | Max |
| bbb | — | 0.33 |
| ccc | — | 0.10 |
| ddd | — | 0.25 |
| eee | — | 0.10 |
| fff | — | 0.20 |

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Outline MS-013, Variation AA.
4. Recommended reflow profile per JEDEC J-STD-020C specification for small body, lead-free components.

### 6.2 Land Pattern: 16-Pin Wide Body SOIC

The figure below illustrates the recommended land pattern details for the Si828x in a 16-Pin Wide Body SOIC. The table lists the values for the dimensions shown in the illustration.

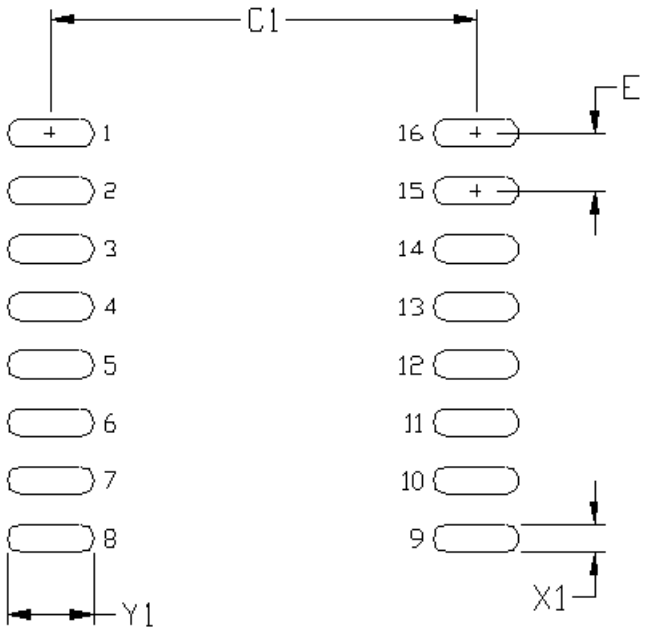



**Figure 6.2. PCB Land Pattern: 16-Pin Wide Body SOIC**

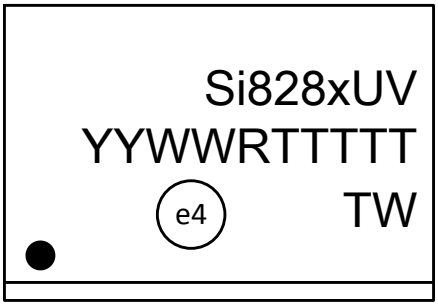
**Table 6.1. 16-Pin Wide Body SOIC Land Pattern Dimensions[1, 2]**

| Dimension | Feature | (mm) |
|---|---|---|
| C1 | Pad Column Spacing | 9.40 |
| E | Pad Row Pitch | 1.27 |
| X1 | Pad Width | 0.60 |
| Y1 | Pad Length | 1.90 |

**Note:**

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P1032X265-16AN for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC), and a card fabrication tolerance of 0.05 mm is assumed.

### 6.3 Top Marking: 16-Pin Wide Body SOIC




**Si8285/86 Top Marking**

**Table 6.2. Si8285/86 Top Marking Explanation**

| | | |
|---|---|---|
| **Line 1 Marking:** | Customer Part Number | Si8285, Si8286 = Product Configuration<br>U = UVLO level<br>B = 9 V; C = 12 V<br>V = Isolation rating<br>D = 5.0 kV |
| **Line 2 Marking:** | YY = Year<br>WW = Workweek | Assigned by the assembly house. Corresponds to the year and workweek of the mold date. |
| | RTTTTT = Mfg Code | Manufacturing code from the Assembly Purchase Order form<br>“R” indicates revision |

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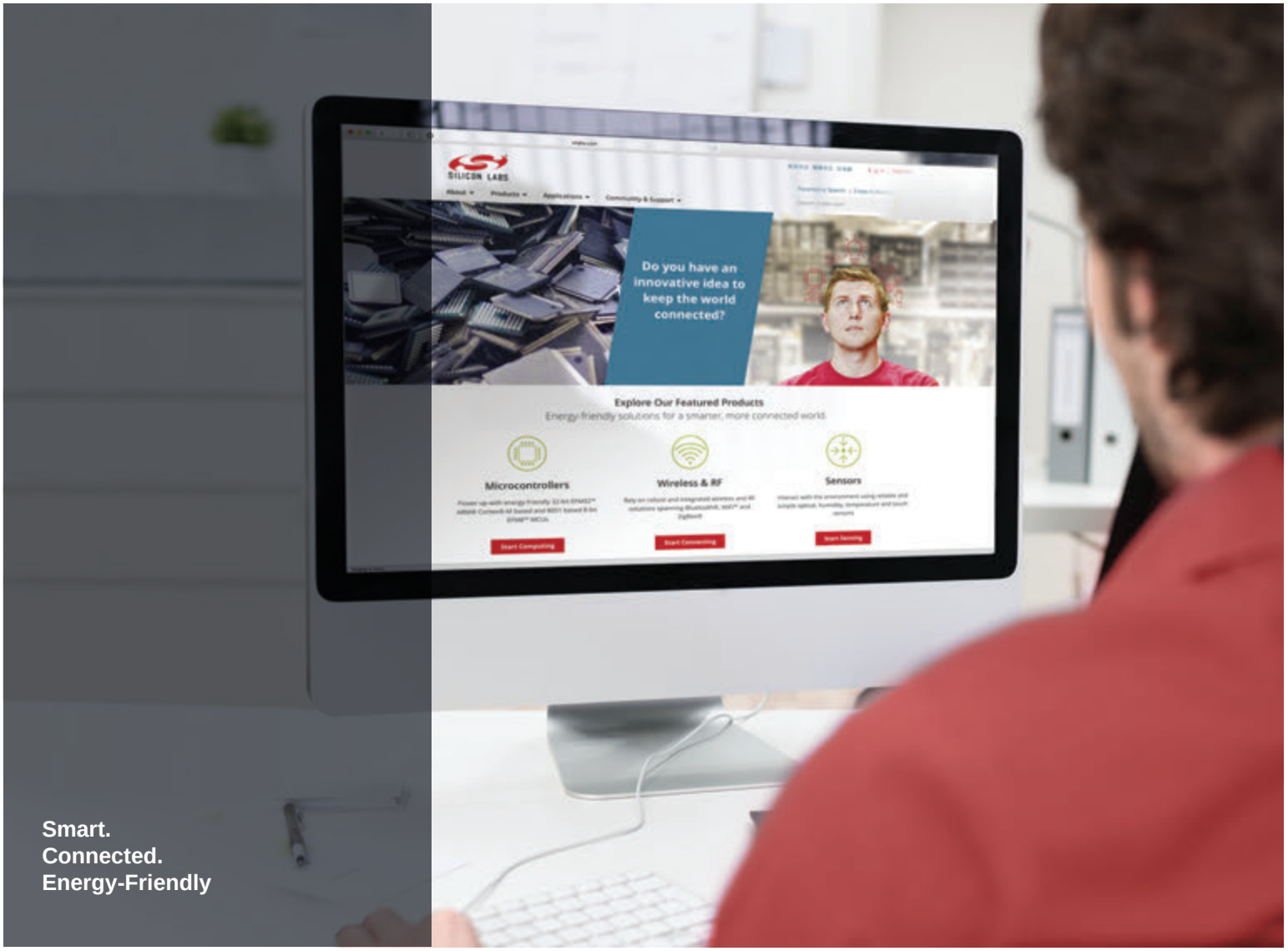


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