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# FAN103

## Primary-Side-Regulation PWM Controller (PWM-PSR)

### Features

- Low Standby Power Under 30 mW
- High Voltage Startup
- Fewest External Component Counts
- Constant-Voltage (CV) and Constant-Current (CC) Control without Secondary-Feedback Circuitry
- Green-Mode Function: Linearly-Decreasing PWM Frequency
- Fixed PWM Frequency at 50 kHz with Frequency Hopping to Solve EMI Problem
- Cable Compensation in CV Mode
- Peak-Current-Mode Control in CV Mode
- Cycle-by-Cycle Current Limiting
- V<sub>DD</sub> Over-Voltage Protection with Auto Restart
- V<sub>DD</sub> Under-Voltage Lockout (UVLO)
- Gate Output Maximum Voltage Clamped at 15 V
- Fixed Over-Temperature Protection with Auto Restart
- Available in the 8-Lead SOP Package

### Applications

- Battery chargers for cellular phones, cordless phones, PDA, digital cameras, power tools, etc.
- Replaces linear transformer and RCC SMPS

### Description

This third-generation Primary-Side-Regulation (PSR) and highly integrated PWM controller provides several features to enhance the performance of low-power flyback converters. The proprietary topology, TRUECURRENT<sup>®</sup>, of FAN103 enables precise CC regulation and simplified circuit for battery charger applications. A low-cost, smaller and lighter charger results as compared to a conventional design or a linear transformer.

To minimize standby power consumption, the proprietary green-mode function provides off-time modulation to linearly decrease PWM frequency under light-load conditions. This green mode assists the power supply in meeting the power conservation requirement.

By using the FAN103, a charger can be implemented with few external components and minimized cost. A typical output CV/CC characteristic envelope is shown in Figure 1.

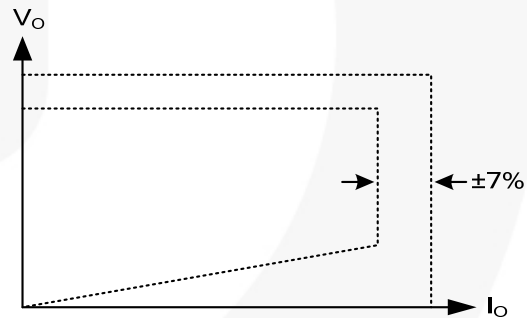


Figure 1. Typical Output V-I Characteristic

### Ordering Information

| Part Number | Operating Temperature Range | Package                               | Packing Method |
|-------------|-----------------------------|---------------------------------------|----------------|
| FAN103MY    | -40°C to +105°C             | 8-Lead, Small Outline Package (SOP-8) | Tape & Reel    |

### Application Diagram

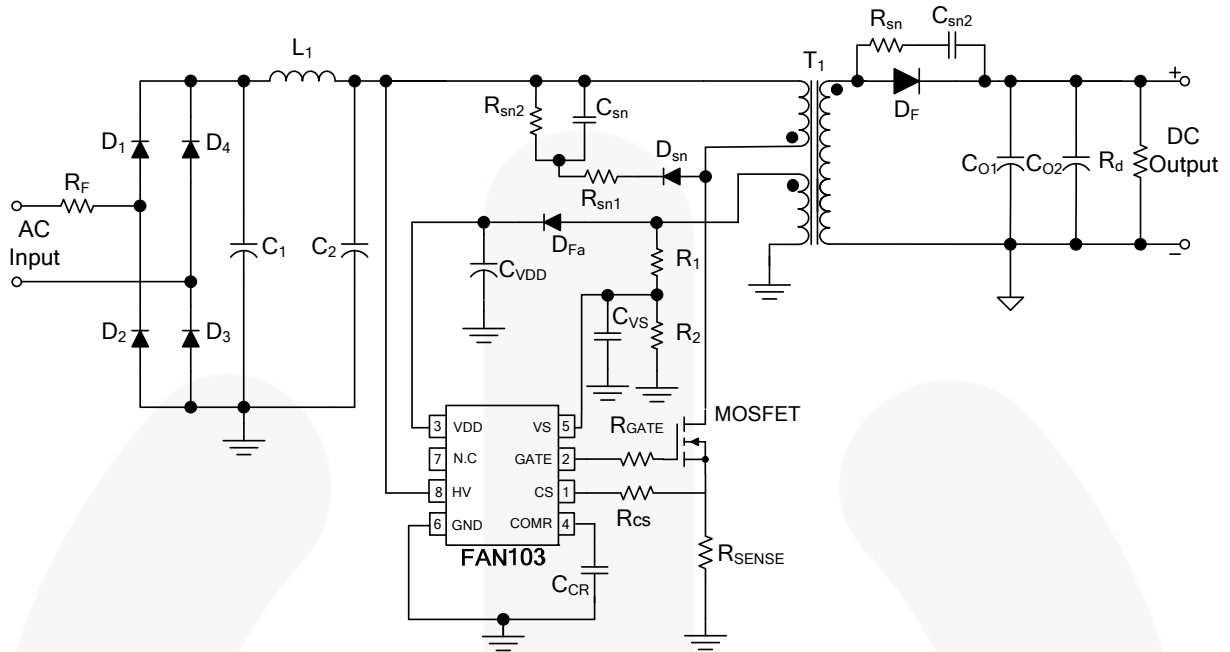


Figure 2. Typical Application

### Internal Block Diagram

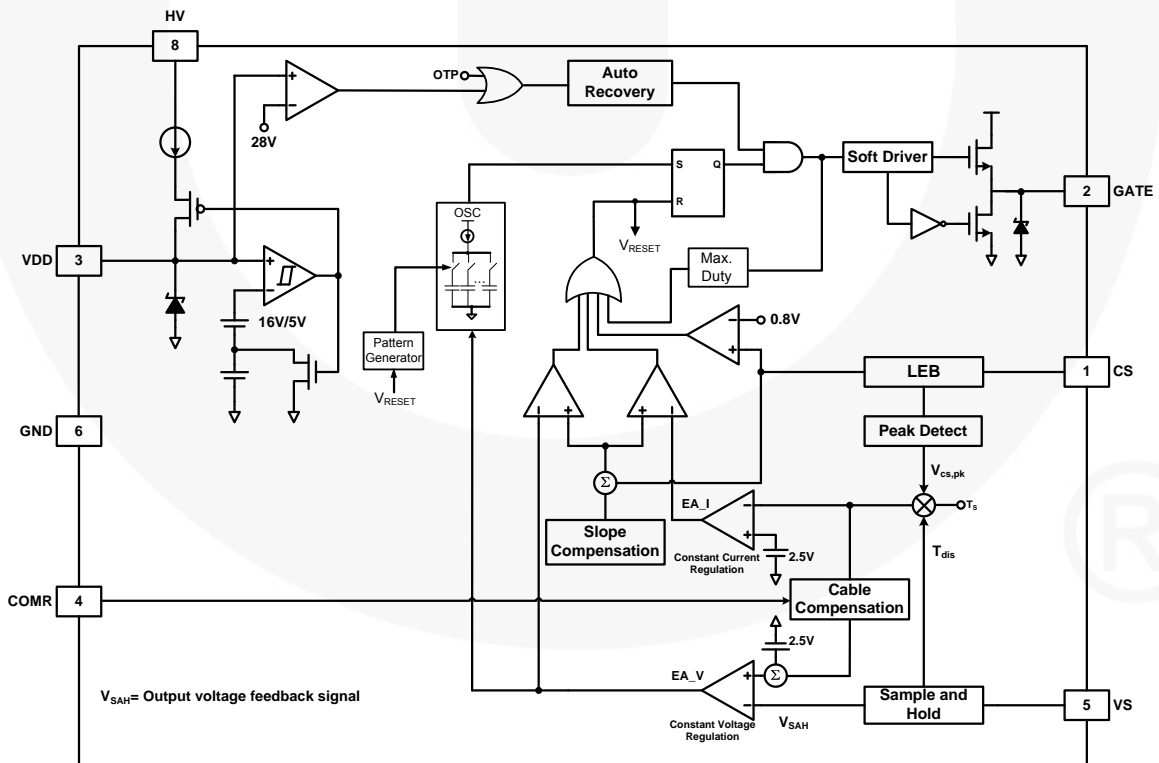
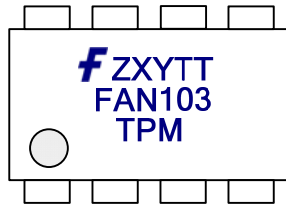


Figure 3. Functional Block Diagram

## Marking Information



F: Fairchild Logo  
 Z: Plant Code  
 X: 1-Digit Year Code  
 Y: 1-Digit Week Code  
 TT: 2-Digit Die Run Code  
 T: Package Type (M=SOP)  
 P: Y=Green Package  
 M: Manufacture Flow Code

Figure 4. Top Mark

## Pin Configuration

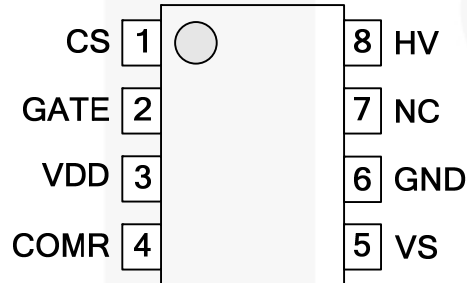


Figure 5. Pin Configuration

## Pin Definitions

| Pin # | Name | Description  |
|-------|------|--|
| 1     | CS   | <b>Current Sense.</b> This pin connects a current sense resistor, to detect the MOSFET current for peak-current-mode control in CV mode, and provides the output-current regulation in CC mode.  |
| 2     | GATE | <b>PWM Signal Output.</b> This pin uses the internal totem-pole output driver to drive the power MOSFET. It is internally clamped below 15 V.  |
| 3     | VDD  | <b>Power Supply.</b> IC operating current and MOSFET driving current are supplied using this pin. This pin is connected to an external $V_{DD}$ capacitor of typically 10 $\mu$ F. The threshold voltages for startup and turn-off are 16 V and 5 V, respectively. The operating current is lower than 5 mA. |
| 4     | COMR | <b>Cable Compensation.</b> This pin connects a capacitance between the COMR and GND pins for compensation voltage drop due to output cable loss in CV mode.  |
| 5     | VS   | <b>Voltage Sense.</b> This pin detects the output voltage information and discharge time based on voltage of auxiliary winding.  |
| 6     | GND  | <b>Ground</b>  |
| 7     | NC   | <b>No Connect</b>  |
| 8     | HV   | <b>High Voltage.</b> This pin connects to bulk capacitor for high-voltage startup.   |

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol        | Parameter   |  | Min. | Max. | Unit                      |
|---------------|---|--|------|------|---------------------------|
| $V_{HV}$      | HV Pin Input Voltage  |  |      | 500  | V                         |
| $V_{VDD}$     | DC Supply Voltage <sup>(1)(2)</sup>                             |  |      | 30   | V                         |
| $V_{VS}$      | VS Pin Input Voltage  |  | -0.3 | 7.0  | V                         |
| $V_{CS}$      | CS Pin Input Voltage  |  | -0.3 | 7.0  | V                         |
| $V_{COMV}$    | Voltage Error Amplifier Output Voltage                          |  | -0.3 | 7.0  | V                         |
| $V_{COMI}$    | Current Error Amplifier Output Voltage                          |  | -0.3 | 7.0  | V                         |
| $P_D$         | Power Dissipation ( $T_A < 50^\circ\text{C}$ )                  |  |      | 660  | mW                        |
| $\theta_{JA}$ | Thermal Resistance (Junction-to-Air)                            |  |      | 150  | $^\circ\text{C}/\text{W}$ |
| $\theta_{JC}$ | Thermal Resistance (Junction-to-Case)                           |  |      | 39   | $^\circ\text{C}/\text{W}$ |
| $T_J$         | Operating Junction Temperature                                  |  | -40  | +150 | $^\circ\text{C}$          |
| $T_{STG}$     | Storage Temperature Range                                       |  | -55  | +150 | $^\circ\text{C}$          |
| $T_L$         | Lead Temperature (Wave Soldering or IR, 10 Seconds)             |  |      | +260 | $^\circ\text{C}$          |
| ESD           | Electrostatic Discharge Capability Except HV Pin <sup>(3)</sup> | Human Body Model, JEDEC-JESD22_A114    | 5000 |      | V                         |
|               |   | Charged Device Model, JEDEC-ESD22_C101 | 2000 |      |                           |

### Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
2. All voltage values, except differential voltages, are given with respect to GND pin.
3. Including HV pin: HBM=500 V, CDM=750 V.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

| Symbol | Parameter                     | Min. | Max. | Unit             |
|--------|-------------------------------|------|------|------------------|
| $T_A$  | Operating Ambient Temperature | -40  | +105 | $^\circ\text{C}$ |

## Electrical Characteristics

Unless otherwise specified,  $V_{DD}=15\text{ V}$  and  $T_A=25^\circ\text{C}$ .

| Symbol                                   | Parameter                                      | Condition  | Min.  | Typ.      | Max.      | Unit          |     |
|--|--|--|-------|-----------|-----------|---------------|-----|
| <b>V<sub>DD</sub> Section</b>            |  |  |       |           |           |               |     |
| $V_{OP}$                                 | Continuously Operating Voltage                 |  |       |           | 25        | V             |     |
| $V_{DD-ON}$                              | Turn-On Threshold Voltage                      |  | 15    | 16        | 17        | V             |     |
| $V_{DD-OFF}$                             | Turn-Off Threshold Voltage                     |  | 4.5   | 5.0       | 5.5       | V             |     |
| $I_{DD-OP}$                              | Operating Current                              |  |       | 3.2       | 5.0       | mA            |     |
| $I_{DD-GREEN}$                           | Green-Mode Operating Supply Current            |  |       | 0.95      | 1.20      | mA            |     |
| $V_{DD-OVP}$                             | $V_{DD}$ Over-Voltage Protection Level         |  |       | 28        |           | V             |     |
| $t_{D-VDDOVP}$                           | $V_{DD}$ Over-Voltage-Protection Debounce Time |  | 90    | 200       | 350       | $\mu\text{s}$ |     |
| <b>HV Startup Current Source Section</b> |  |  |       |           |           |               |     |
| $V_{HV-MIN}$                             | Minimum Startup Voltage on HV Pin              |  |       |           | 50        | V             |     |
| $I_{HV}$                                 | Supply Current Drawn from Pin HV               | $V_{DC}=100\text{ V}$                              |       | 1.2       | 5.0       | mA            |     |
| $I_{HV-LC}$                              | Leakage Current after Startup                  | $HV=500\text{ V}$ , $V_{DD}=V_{DD-OFF}+1\text{ V}$ |       | 0.5       | 3.0       | $\mu\text{A}$ |     |
| <b>Oscillator Section</b>                |  |  |       |           |           |               |     |
| $f_{OSC}$                                | Frequency                                      | Center Frequency                                   |       | 47        | 50        | 53            | kHz |
|  |  | Frequency Hopping Range                            |       | $\pm 1.5$ | $\pm 2.0$ | $\pm 2.5$     |     |
| $t_{FHR}$                                | Frequency Hopping Period                       |  |       | 3         |           | ms            |     |
| $f_{OSC-N-MIN}$                          | Minimum Frequency at No-Load                   |  |       | 370       |           | Hz            |     |
| $f_{OSC-CM-MIN}$                         | Minimum Frequency at CCM                       |  |       | 13        |           | kHz           |     |
| $f_{DV}$                                 | Frequency Variation vs. $V_{DD}$ Deviation     | $V_{DD}=10\sim 25\text{ V}$                        |       | 1         | 2         | %             |     |
| $f_{DT}$                                 | Frequency Variation vs. Temperature Deviation  | $T_A=-40^\circ\text{C}$ to $+105^\circ\text{C}$    |       |           | 15        | %             |     |
| <b>Voltage-Error-Amplifier Section</b>   |  |  |       |           |           |               |     |
| $V_{VR}$                                 | Reference Voltage                              |  | 2.475 | 2.500     | 2.525     | V             |     |
| $V_N$                                    | Green-Mode Starting Voltage on EA_V            | $f_{OSC}=2\text{ kHz}$                             |       | 2.5       |           | V             |     |
| $V_G$                                    | Green-Mode Ending Voltage on EA_V              | $f_{OSC}=1\text{ kHz}$                             |       | 0.5       |           | V             |     |
| <b>Voltage-Sense Section</b>             |  |  |       |           |           |               |     |
| $V_{BIAS-COMV}$                          | Adaptive Bias Voltage Dominated by $V_{COMV}$  | $R_{VS}=20\text{ k}\Omega$                         |       | 1.4       |           | V             |     |
| $I_{IC}$                                 | IC Bias Current                                |  |       | 10        |           | $\mu\text{A}$ |     |
| <b>Current-Sense Section</b>             |  |  |       |           |           |               |     |
| $t_{PD}$                                 | Propagation Delay to GATE Output               |  |       | 90        | 200       | ns            |     |
| $t_{MIN-N}$                              | Minimum On Time at No-Load                     | $V_{COMR}=1\text{ V}$                              |       | 950       |           | ns            |     |
| $V_{TH}$                                 | Threshold Voltage for Current Limit            |  |       | 0.8       |           | V             |     |
| $V_{TL}$                                 | Threshold Voltage on VS Pin Smaller than 0.5 V |  |       | 0.25      |           | V             |     |

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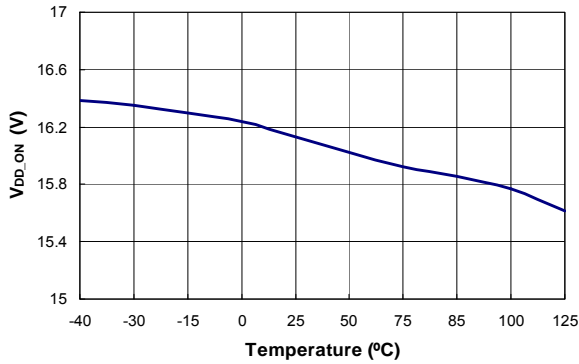
**Electrical Characteristics** (Continued)Unless otherwise specified,  $V_{DD}=15\text{ V}$  and  $T_A=25^\circ\text{C}$ .

| Symbol                                     | Parameter                                    | Condition                               | Min.  | Typ.  | Max.  | Unit             |
|--|--|---|-------|-------|-------|------------------|
| <b>Current-Error-Amplifier Section</b>     |  |   |       |       |       |                  |
| $V_{IR}$                                   | Reference Voltage                            |   | 2.475 | 2.500 | 2.525 | V                |
| <b>Cable Compensation Section</b>          |  |   |       |       |       |                  |
| $V_{COMR}$                                 | COMR Pin for Cable Compensation              |   |       | 0.85  |       | V                |
| <b>Gate Section</b>                        |  |   |       |       |       |                  |
| $DCY_{MAX}$                                | Maximum Duty Cycle                           |   | 76    | 81    | 86    | %                |
| $V_{OL}$                                   | Output Voltage Low                           | $V_{DD}=20\text{ V}$ , Gate Sinks 10 mA |       |       | 1.5   | V                |
| $V_{OH}$                                   | Output Voltage High                          | $V_{DD}=8\text{ V}$ , Gate Sources 1 mA | 5     |       |       | V                |
| $t_r$                                      | Rising Time                                  | $C_L=1\text{ nF}$                       |       | 200   | 250   | ns               |
| $t_f$                                      | Falling Time                                 | $C_L=1\text{ nF}$                       |       | 60    | 100   | ns               |
| $V_{CLAMP}$                                | Output Clamp Voltage                         | $V_{DD}=25\text{ V}$                    |       | 15    | 18    | V                |
| <b>Over-Temperature-Protection Section</b> |  |   |       |       |       |                  |
| $T_{OTP}$                                  | Threshold Temperature for OTP <sup>(4)</sup> |   |       | +140  |       | $^\circ\text{C}$ |

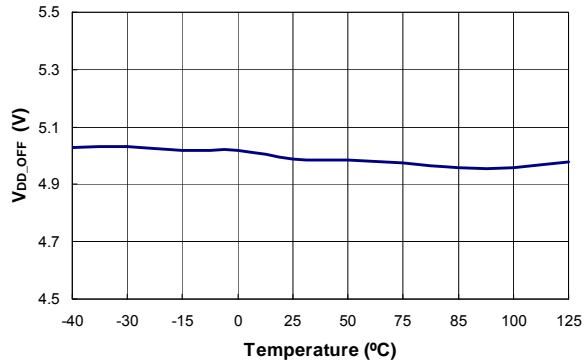
**Note:**

- When the over-temperature protection is activated, the power system enters auto restart mode and output is disabled.

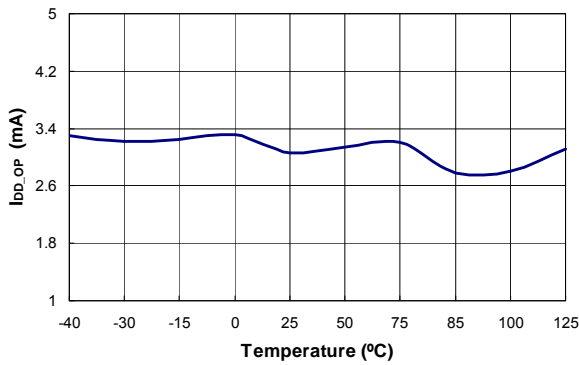
## Typical Performance Characteristics



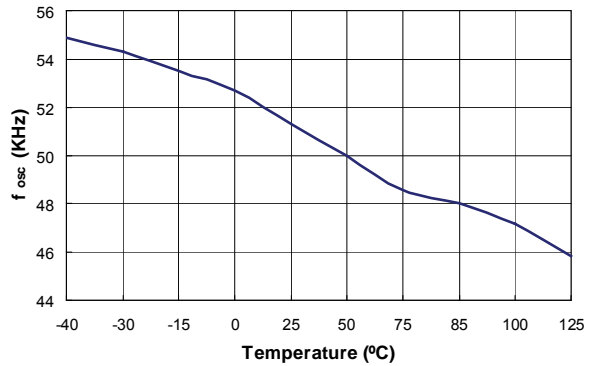
**Figure 6. Turn-On Threshold Voltage (V<sub>DD-ON</sub>) vs. Temperature**



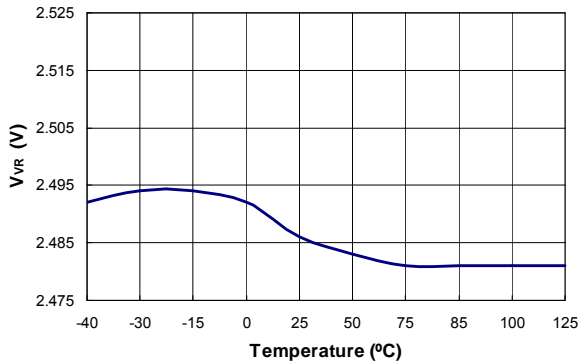
**Figure 7. Turn-Off Threshold Voltage (V<sub>DD-OFF</sub>) vs. Temperature**



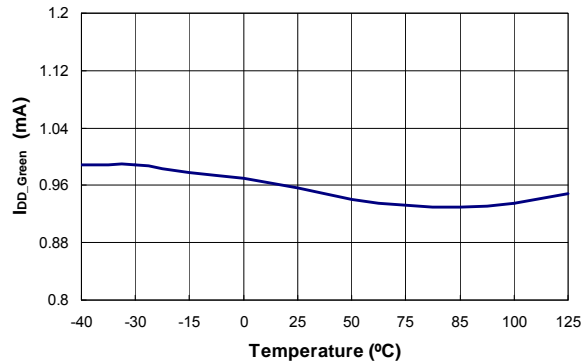
**Figure 8. Operating Current (I<sub>DD-OP</sub>) vs. Temperature**



**Figure 9. Center Frequency (f<sub>OSC</sub>) vs. Temperature**



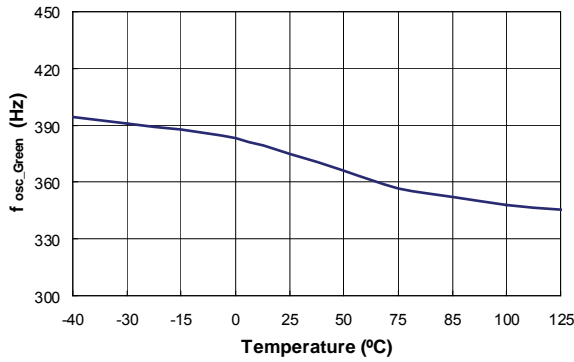
**Figure 10. Reference Voltage (V<sub>VR</sub>) vs. Temperature**



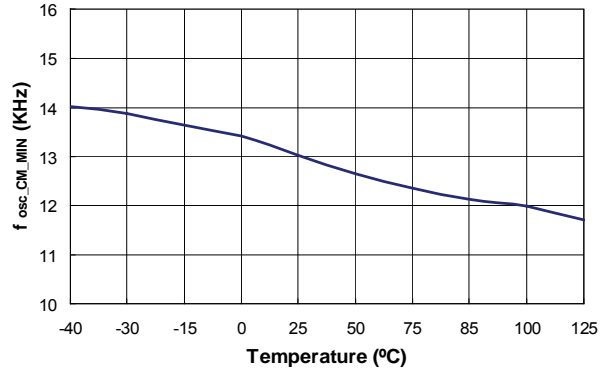
**Figure 11. Green-Mode Operating Supply Current (I<sub>DD-GREEN</sub>) vs. Temperature**



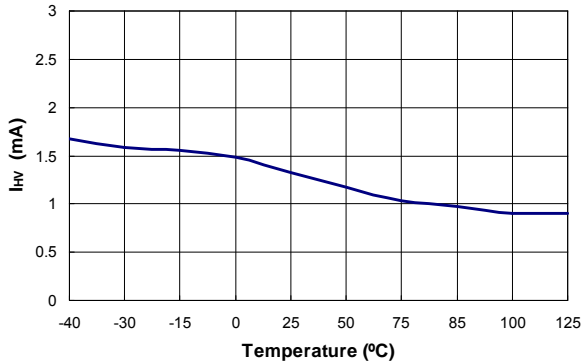
## Typical Performance Characteristics



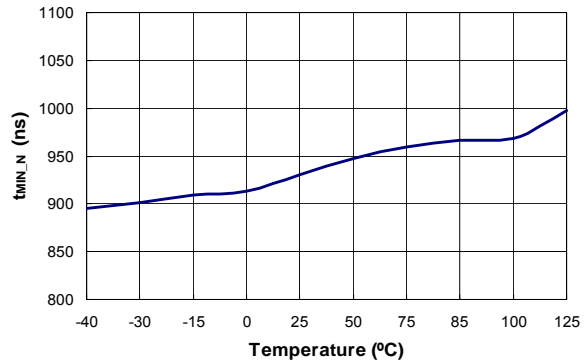
**Figure 12. Minimum Frequency at No Load (f<sub>osc-N-MIN</sub>) vs. Temperature**



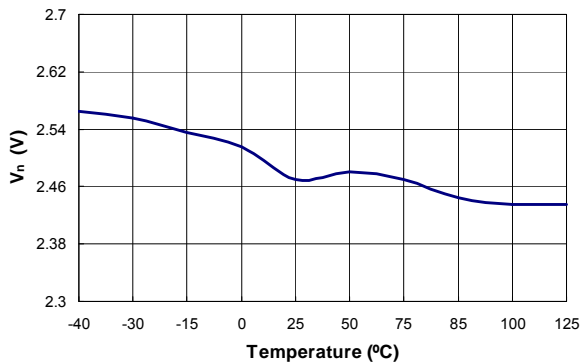
**Figure 13. Minimum Frequency at CCM (f<sub>osc-CM-MIN</sub>) vs. Temperature**



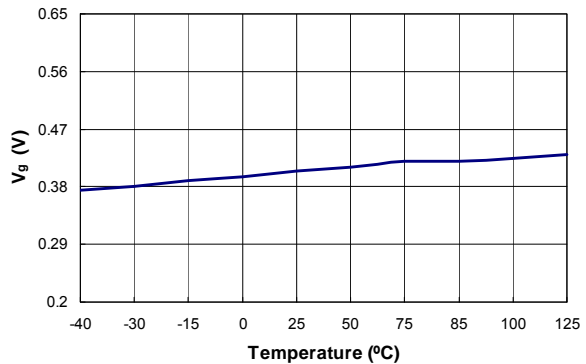
**Figure 14. Supply Current Drawn from Pin HV (I<sub>HV</sub>) vs. Temperature**



**Figure 15. Minimum On Time at No Load (t<sub>MIN-N</sub>) vs. Temperature**



**Figure 16. Green Mode Starting Voltage on EA\_V (V<sub>N</sub>) vs. Temperature**



**Figure 17. Green Mode Ending Voltage on EA\_V (V<sub>G</sub>) vs. Temperature**

## Typical Performance Characteristics

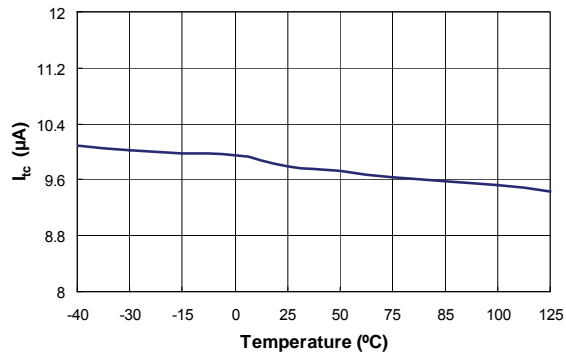


Figure 18. IC Bias Current ( $I_{tc}$ ) vs. Temperature

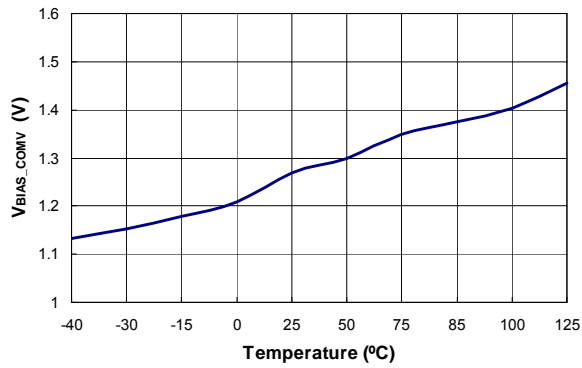


Figure 19. Output Clamp Voltage ( $V_{CLAMP}$ ) vs. Temperature

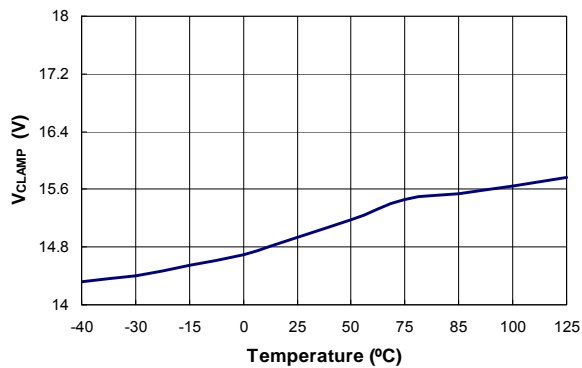


Figure 20. Variation Test Voltage on COMR Pin for Cable Compensation ( $V_{COMR}$ ) vs. Temperature

## Functional Description

Figure 21 shows the basic circuit diagram of a primary-side regulated flyback converter with typical waveforms shown in Figure 22. Generally, discontinuous conduction mode (DCM) operation is preferred for primary-side regulation since it allows better output regulation. The operation principles of DCM flyback converter are as follows:

During the MOSFET on time ( $t_{ON}$ ), input voltage ( $V_{DL}$ ) is applied across the primary-side inductor ( $L_m$ ). Then, MOSFET current ( $I_{ds}$ ) increases linearly from zero to the peak value ( $I_{pk}$ ). During this time, the energy is drawn from the input and stored in the inductor.

When the MOSFET is turned off, the energy stored in the inductor forces the rectifier diode (D) to be turned on. While the diode is conducting, the output voltage ( $V_o$ ), together with diode forward voltage drop ( $V_F$ ), are applied across the secondary-side inductor ( $L_m \times N_s^2 / N_p^2$ ) and the diode current ( $I_D$ ) decreases linearly from the peak value ( $I_{pk} \times N_p / N_s$ ) to zero. At the end of inductor current discharge time ( $t_{DIS}$ ), all the energy stored in the inductor has been delivered to the output.

When the diode current reaches zero, the transformer auxiliary winding voltage ( $V_w$ ) begins to oscillate by the resonance between the primary-side inductor ( $L_m$ ) and the effective capacitor loaded across MOSFET.

During the inductor current discharge time, the sum of output voltage and diode forward-voltage drop is reflected to the auxiliary winding side as  $(V_o + V_F) \times N_a / N_s$ . Since the diode forward-voltage drop decreases as current decreases, the auxiliary winding voltage reflects the output voltage best at the end of diode conduction time, where the diode current diminishes to zero. Thus, by sampling the winding voltage at the end of the diode conduction time, the output voltage information can be obtained. The internal error amplifier for output voltage regulation (EA\_V) compares the sampled voltage with internal precise reference to generate error voltage ( $V_{COMV}$ ), which determines the duty cycle of the MOSFET in CV mode.

Meanwhile, the output current can be estimated using the peak drain current and inductor current discharge time since output current is same as average of the diode current in steady state.

The output current estimator recognizes the peak value of the drain current with a peak-detection circuit and calculates the output current using inductor discharge time ( $t_{DIS}$ ) and switching period ( $t_s$ ). This output information is compared with internal precise reference to generate error voltage ( $V_{COMI}$ ), which determines the duty cycle of the MOSFET in CC Mode. With Fairchild's innovative TRUECURRENT<sup>®</sup> technique, constant current (CC) output can be precisely controlled.

Among the two error voltages,  $V_{COMV}$  and  $V_{COMI}$ , the small one determines the duty cycle. Therefore, during constant voltage regulation mode,  $V_{COMV}$  determines the duty cycle while  $V_{COMI}$  is saturated to HIGH. During

constant current regulation mode,  $V_{COMI}$  determines the duty cycle while  $V_{COMV}$  is saturated to HIGH.

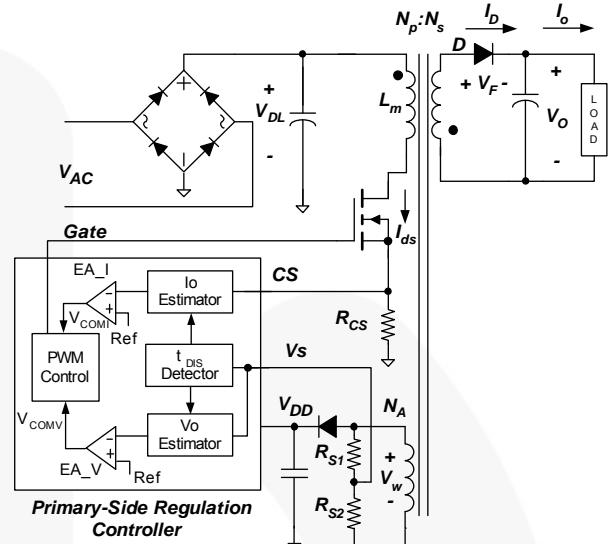


Figure 21. Simplified PSR Flyback Converter Circuit

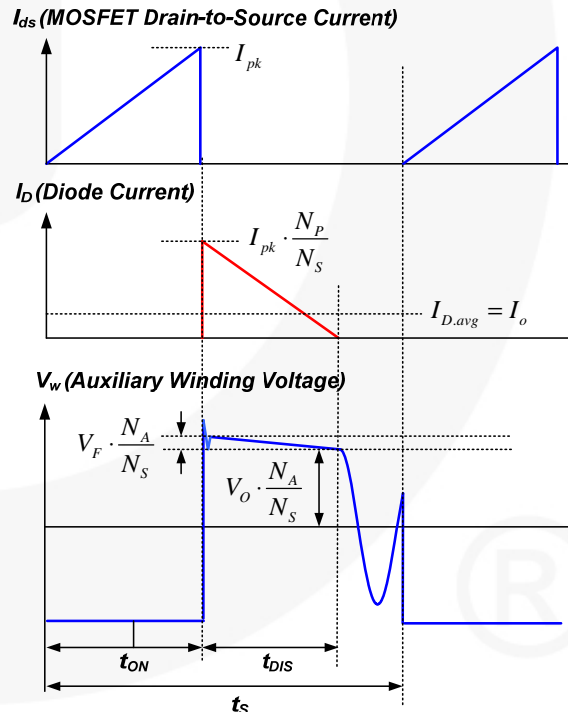


Figure 22. Key Waveforms of DCM Flyback Converter



## Under-Voltage Lockout (UVLO)

The turn-on and turn-off thresholds are fixed internally at 16 V and 5 V, respectively. During startup, the hold-up capacitor must be charged to 16 V through the startup resistor to enable the FAN103. The hold-up capacitor continues to supply  $V_{DD}$  until power can be delivered from the auxiliary winding of the main transformer.  $V_{DD}$  is not allowed to drop below 5 V during this startup process. This UVLO hysteresis window ensures that hold-up capacitor properly supplies  $V_{DD}$  during startup.

## Protections

The FAN103 has several self-protection functions, such as Over-Voltage Protection (OVP), Over-Temperature Protection (OTP), and Pulse-by-Pulse Current limit. All the protections are implemented as auto-restart mode. Once an abnormal condition occurs, switching is terminated and the MOSFET remains off, causing  $V_{DD}$  to drop. When  $V_{DD}$  drops to the  $V_{DD}$  turn-off voltage of 5 V, the internal startup circuit is enabled again, then the supply current drawn from HV pin charges the hold-up capacitor. When  $V_{DD}$  reaches the turn-on voltage of 16 V, FAN103 resumes normal operation. In this manner, the auto-restart alternately enables and disables the switching of the MOSFET until the abnormal condition is eliminated (see Figure 26).

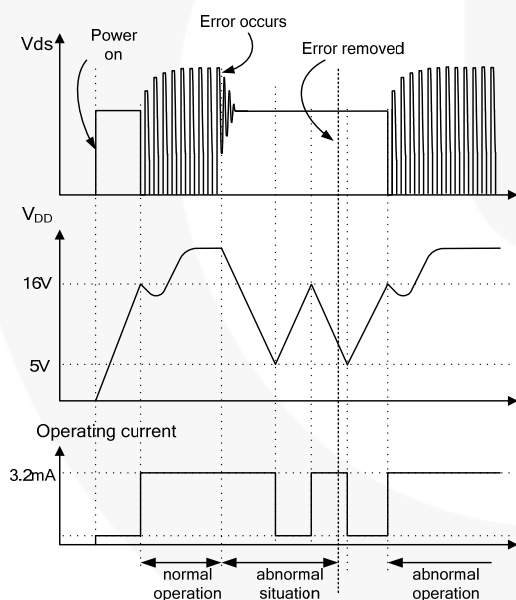


Figure 26. Auto Restart Operation

## $V_{DD}$ Over-Voltage Protection (OVP)

$V_{DD}$  over-voltage protection prevents damage from over-voltage conditions. If the  $V_{DD}$  voltage exceeds 28 V at open-loop feedback condition, OVP is triggered and the PWM switching is disabled. The OVP has a de-bounce time (typically 200  $\mu$ s) to prevent false triggering due to switching noises.

## Over-Temperature Protection (OTP)

The built-in temperature-sensing circuit shuts down PWM output if the junction temperature exceeds 140°C.

## Pulse-by-pulse Current Limit

When the sensing voltage across the current sense resistor exceeds the internal threshold of 0.8 V, the MOSFET is turned off for the remainder of switching cycle. In normal operation, the pulse-by-pulse current limit is not triggered since the peak current is limited by the control loop.

## Leading-Edge Blanking (LEB)

Each time the power MOSFET switches on, a turn-on spike occurs at the sense resistor. To avoid premature termination of the switching pulse, a leading-edge blanking time is built in. Conventional RC filtering can be omitted. During this blanking period, the current-limit comparator is disabled and cannot switch off the gate driver.

## Gate Output

The FAN103 output stage is a fast totem-pole gate driver. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. The output driver is clamped by an internal 15 V Zener diode to protect power MOSFET transistors against undesired over-voltage gate signals.

## Built-in Slope Compensation

The sensed voltage across the current sense resistor is used for current mode control and pulse-by-pulse current limiting. Built-in slope compensation improves stability and prevents sub-harmonic oscillations due to peak-current mode control. The FAN103 has a synchronized, positive-slope ramp built-in at each switching cycle.

## Noise Immunity

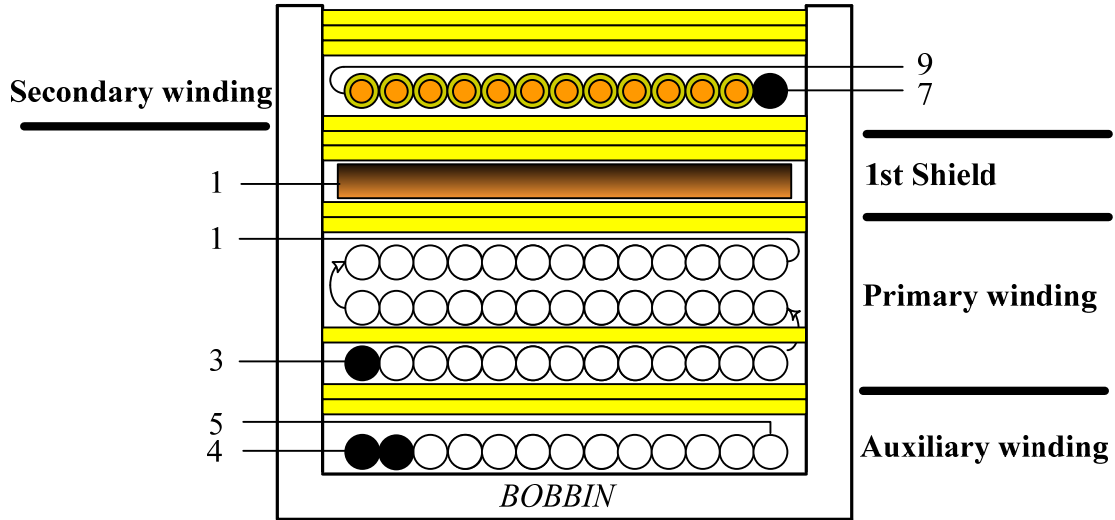
Noise from the current sense or the control signal can cause significant pulse-width jitter, particularly in continuous-conduction mode. While slope compensation helps alleviate these problems, further precautions should still be taken. Good placement and layout practices should be followed. Avoiding long PCB traces and component leads, locating compensation and filter components near the FAN103, and increasing the power MOS gate resistance is advised.



**Typical Application Circuit** (Continued)

**Transformer Specification**

- Core: EE16
- Bobbin: EE16



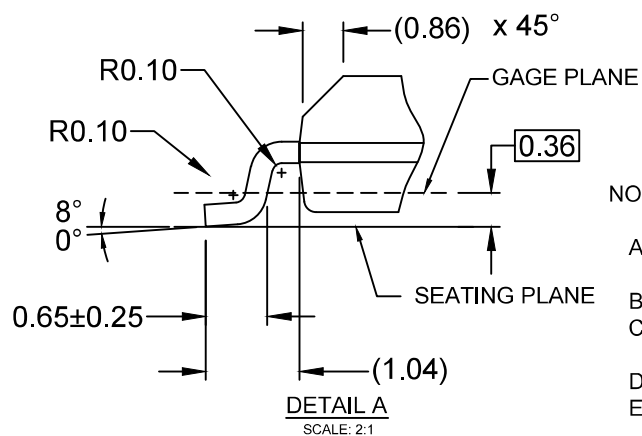
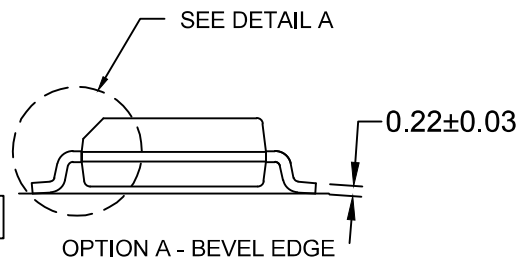
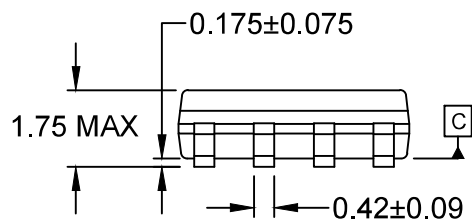
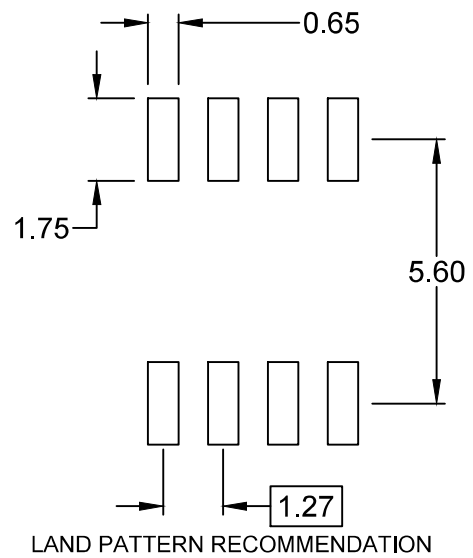
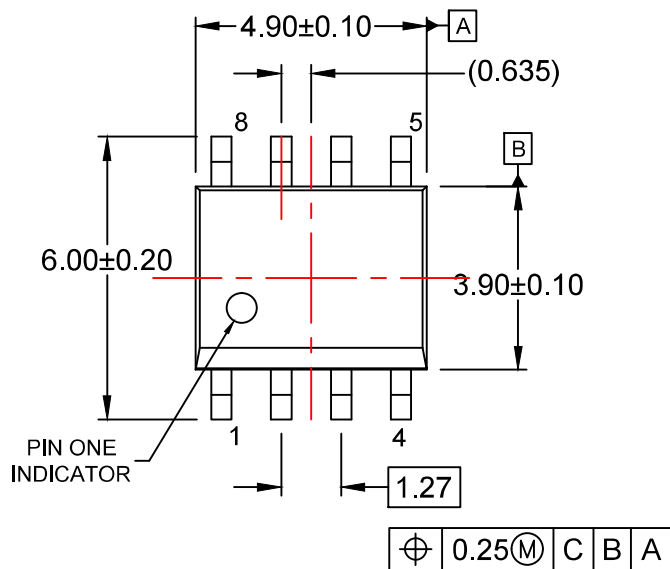
**Figure 29. Bobbin Winding Diagram**

**Notes:**

5. When W4R's winding is reversed winding, it must wind one layer.
6. When W2 is winding, put 1 layer tape after wind first layer.

| NO  | TERMINAL |   | WIRE               | Ts  | INSULATION | BARRIER |         |
|-----|----------|---|--------------------|-----|------------|---------|---------|
|     | S        | F |                    |     | Ts         | Primary | Seconds |
| W1  | 4        | 5 | 2UEW 0.23*2        | 15  | 2          |         |         |
| W2  | 3        | 1 | 2UEW 0.17*1        | 40  | 1          |         |         |
|     |          |   |                    | 40  | 0          |         |         |
|     |          |   |                    | 37  | 2          |         |         |
| W3  | 1        |   | COPPER SHIELD      | 1.2 | 3          |         |         |
| W4R | 7        | 9 | TEX-E 0.6*1        | 9   | 3          |         |         |
|     |          |   | CORE ROUNDING TAPE |     | 3          |         |         |

|                                | Pin   | Specification | Remark                              |
|--------------------------------|-------|---------------|-------------------------------------|
| Primary-Side Inductance        | 1 – 3 | 1.75 mH ± 5%  | 100 kHz, 1 V                        |
| Primary-Side Effective Leakage | 1 – 3 | 80 μH ± 5%    | Short One of the Secondary Windings |



NOTES:

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X175-8M
- E) DRAWING FILENAME: M08Arev16





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