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# FDT86102LZ

## N-Channel PowerTrench® MOSFET

### 100 V, 6.6 A, 28 mΩ

#### Features

- Max  $r_{DS(on)}$  = 28 mΩ at  $V_{GS} = 10$  V,  $I_D = 6.6$  A
- Max  $r_{DS(on)}$  = 38 mΩ at  $V_{GS} = 4.5$  V,  $I_D = 5.5$  A
- HBM ESD protection level > 6 kV typical (Note 4)
- Very low Qg and Qgd compared to competing trench technologies
- Fast switching speed
- 100% UIL Tested
- RoHS Compliant

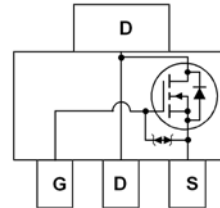
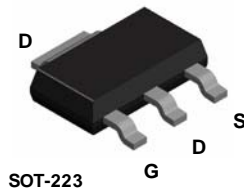


#### General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been especially tailored to minimize the on-state resistance and switching loss. G-S zener has been added to enhance ESD voltage level.

#### Applications

- DC-DC conversion
- Inverter
- Synchronous Rectifier



#### MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	100	V
$V_{GS}$	Gate to Source Voltage	±20	V
$I_D$	Drain Current -Continuous	6.6	A
	-Pulsed	40	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	84	mJ
$P_D$	Power Dissipation $T_A = 25$ °C (Note 1a)	2.2	W
	Power Dissipation $T_A = 25$ °C (Note 1b)	1.0	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

#### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	12	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	55	

#### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
86102LZ	FDT86102LZ	SOT-223	13 "	12 mm	2500 units

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}, V_{GS} = 0\text{ V}$	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		70		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			$\pm 10$	$\mu\text{A}$

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	1.0	1.4	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-6		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 6.6\text{ A}$		22	28	m $\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 5.5\text{ A}$		27	38	
		$V_{GS} = 10\text{ V}, I_D = 6.6\text{ A}, T_J = 125\text{ }^\circ\text{C}$		36	46	
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 6.6\text{ A}$		26		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$		1118	1490	pF
$C_{oss}$	Output Capacitance			181	245	pF
$C_{rss}$	Reverse Transfer Capacitance			7.5	15	pF
$R_g$	Gate Resistance			0.5		$\Omega$

### Switching Characteristics

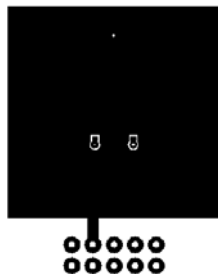
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\text{ V}, I_D = 6.6\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\text{ }\Omega$		6.6	14	ns	
$t_r$	Rise Time			1.9	10	ns	
$t_{d(off)}$	Turn-Off Delay Time			19	31	ns	
$t_f$	Fall Time			2.2	10	ns	
$Q_{g(TOT)}$	Total Gate Charge		$V_{GS} = 0\text{ V to } 10\text{ V}$		17	25	nC
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\text{ V to } 4.5\text{ V}$	$V_{DD} = 50\text{ V},$ $I_D = 6.6\text{ A}$		8.3	12	
$Q_{gs}$	Gate to Source Charge				2.6		nC
$Q_{gd}$	Gate to Drain "Miller" Charge				2.2		nC

### Drain-Source Diode Characteristics

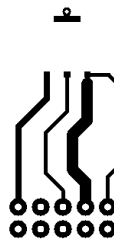
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 6.6\text{ A}$ (Note 2)		0.82	1.3	V
		$V_{GS} = 0\text{ V}, I_S = 1\text{ A}$ (Note 2)		0.68	1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = 6.6\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		40	64	ns
$Q_{rr}$	Reverse Recovery Charge			36	58	nC

#### NOTES:

- $R_{\theta JA}$  is determined with the device mounted on a  $1\text{ in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5\text{ in.}$  board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $55\text{ }^\circ\text{C/W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper



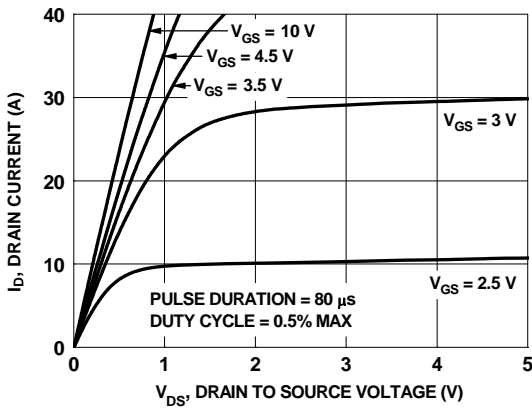
b)  $118\text{ }^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width <  $300\text{ }\mu\text{s}$ , Duty cycle < 2.0 %.

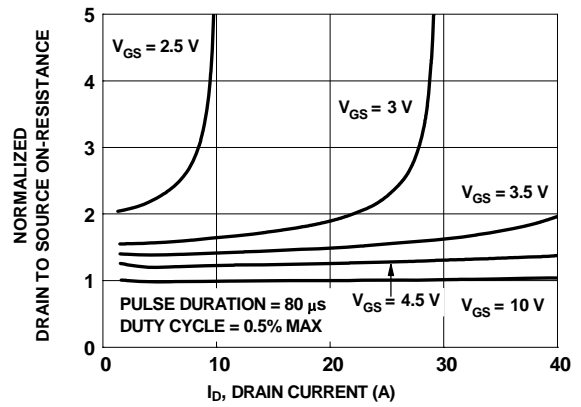
3. Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 1\text{ mH}$ ,  $I_{AS} = 13\text{ A}$ ,  $V_{DD} = 90\text{ V}$ ,  $V_{GS} = 10\text{ V}$ .

4. The diode connected between gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

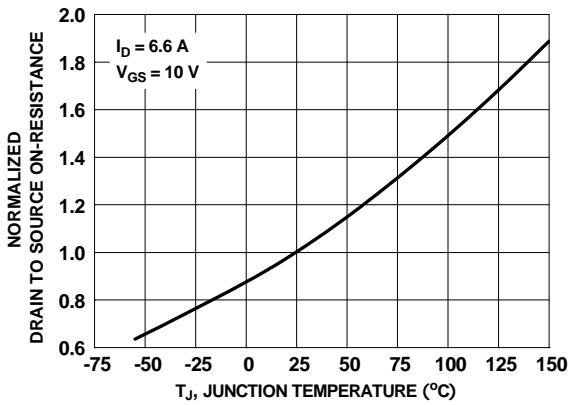
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



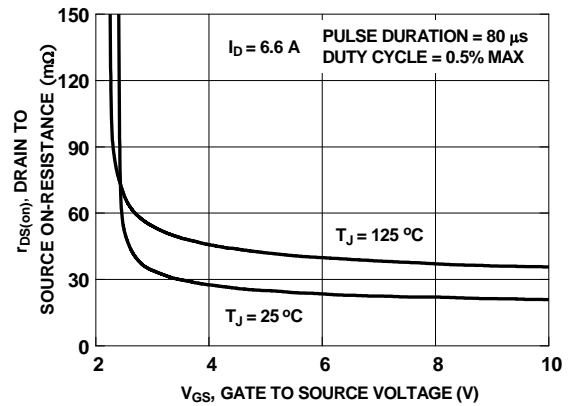
**Figure 1. On-Region Characteristics**



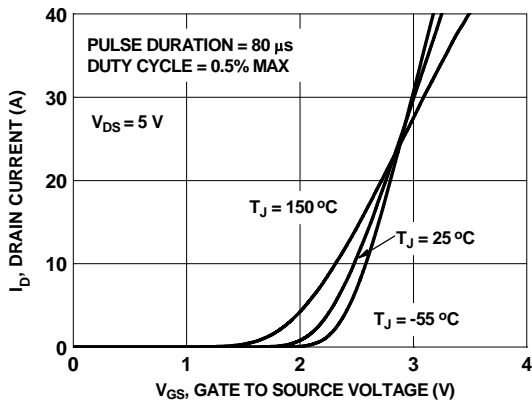
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



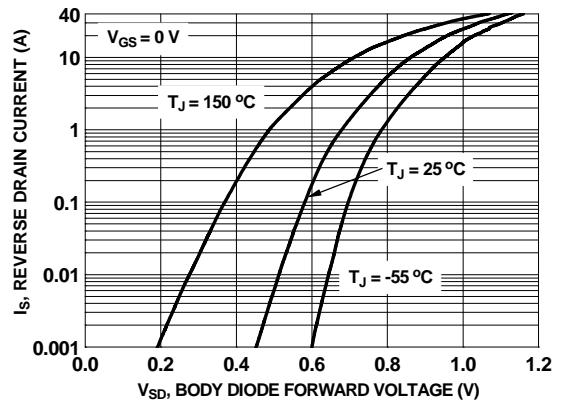
**Figure 3. Normalized On-Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**

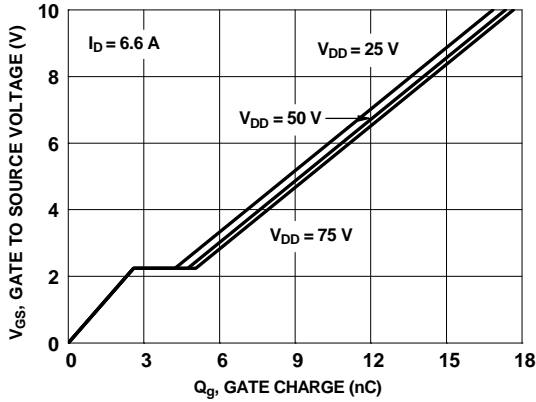


**Figure 5. Transfer Characteristics**

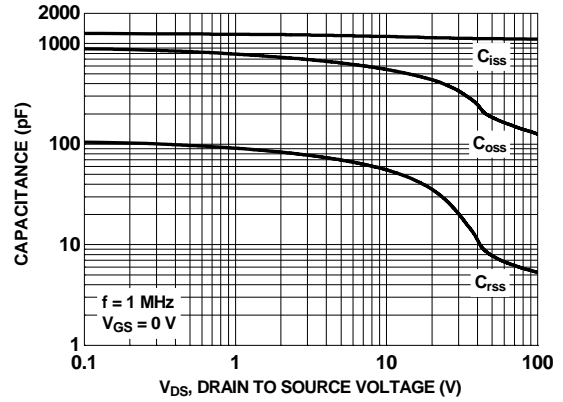


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

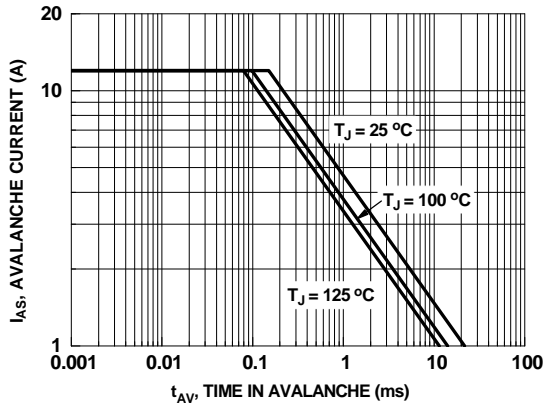
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



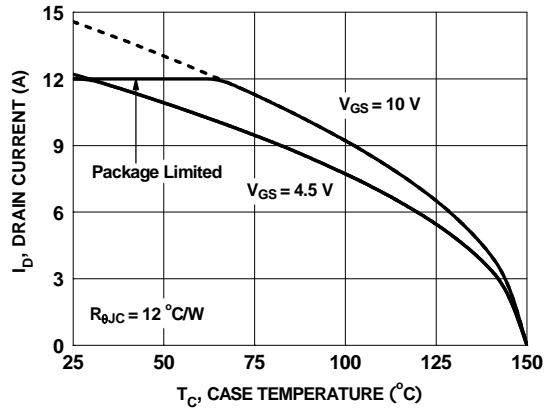
**Figure 7. Gate Charge Characteristics**



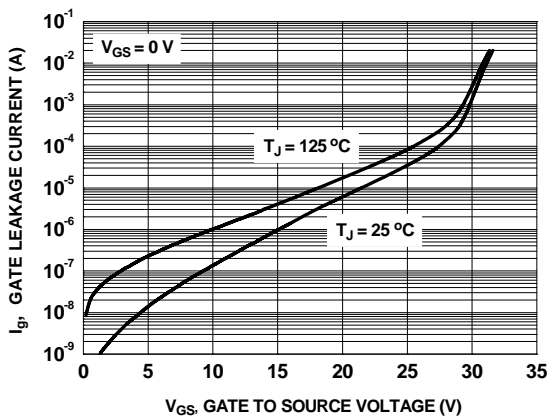
**Figure 8. Capacitance vs Drain to Source Voltage**



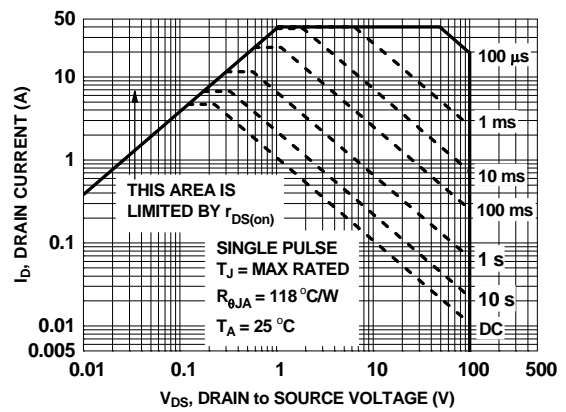
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

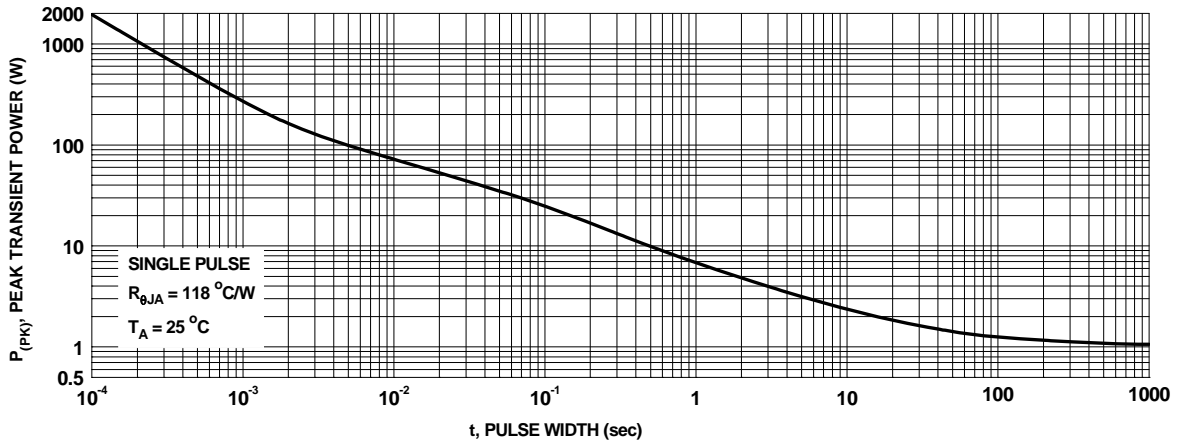


**Figure 11. Gate Leakage Current vs Gate to Source Voltage**

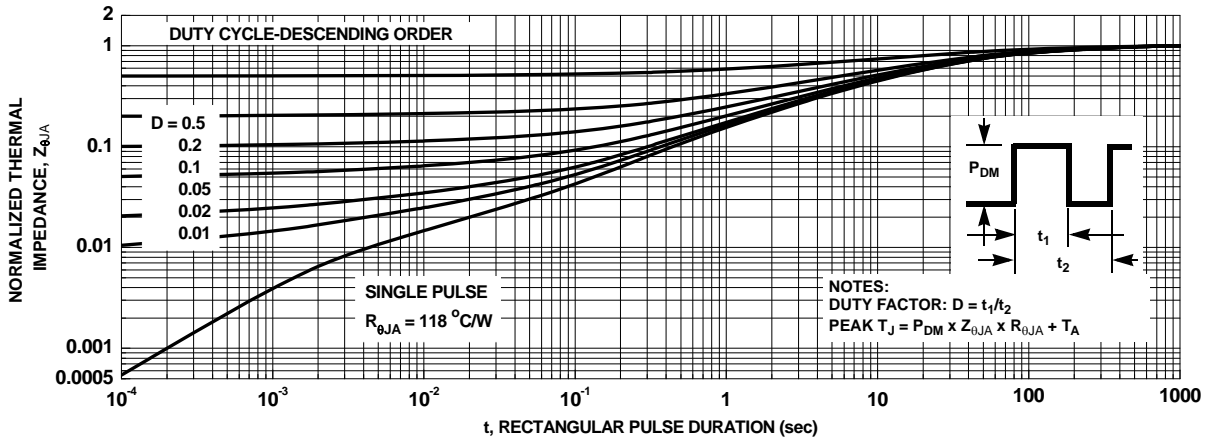


**Figure 12. Forward Bias Safe Operating Area**

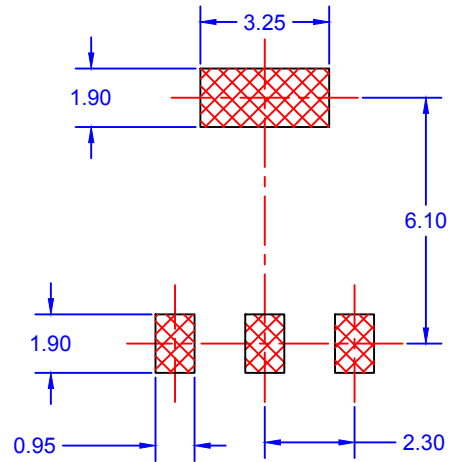
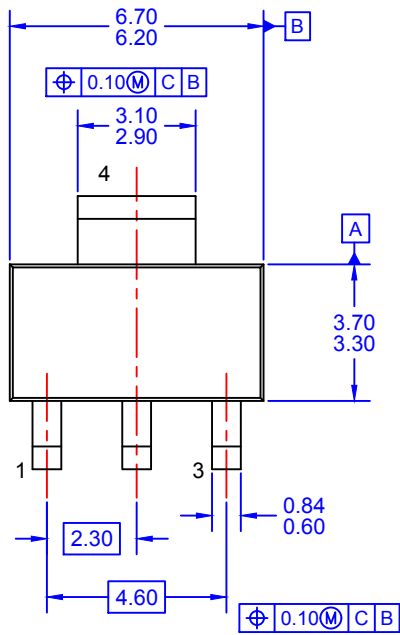
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



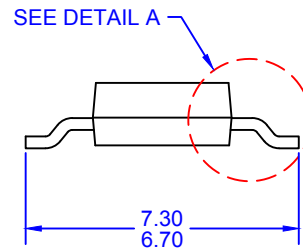
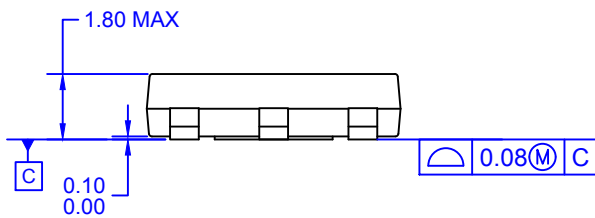
**Figure 13. Single Pulse Maximum Power Dissipation**



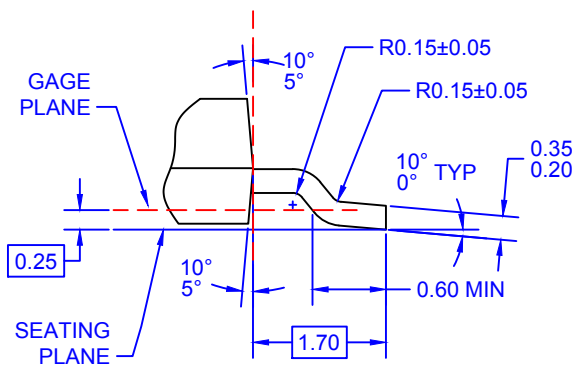
**Figure 14. Junction-to-Ambient Transient Thermal Response Curve**



LAND PATTERN RECOMMENDATION



- NOTES: UNLESS OTHERWISE SPECIFIED  
 A) DRAWING BASED ON JEDEC REGISTRATION TO-261C, VARIATION AA.  
 B) ALL DIMENSIONS ARE IN MILLIMETERS.  
 C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.  
 D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.  
 E) LANDPATTERN NAME: SOT230P700X180-4BN  
 F) DRAWING FILENAME: MKT-MA04AREV3



DETAIL A  
 SCALE: 2:1



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