DIRECT DIGITAL SYNTHESIZER, WAVEFORM GENERATOR

AD9831

FEATURES

3 V/5 V Power Supply
25 MHz Speed
On-Chip SINE Look-Up Table
On-Chip 10-Bit DAC
Parallel Loading
Powerdown Option
72 dB SFDR
125 mW (5 V) Power Consumption
40 mW (3 V) Power Consumption
48-Pin LQFP

APPLICATIONS

DDS Tuning
Digital Demodulation

GENERAL DESCRIPTION

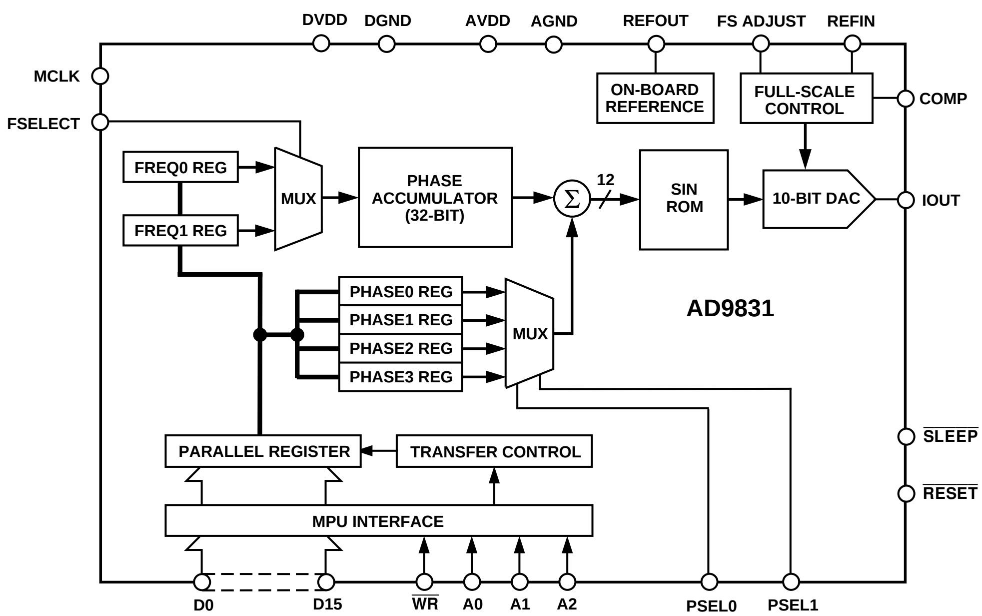
This DDS device is a numerically controlled oscillator employing a phase accumulator, a sine look-up table and a 10-bit D/A converter integrated on a single CMOS chip. Modulation capabilities are provided for phase modulation and frequency modulation.

Clock rates up to 25 MHz are supported. Frequency accuracy can be controlled to one part in 4 billion. Modulation is effected by loading registers through the parallel microprocessor interface.

A powerdown pin allows external control of a powerdown mode. The part is available in a 48-pin LQFP package.

Similar DDS products can be found at http://www.analog.com/DDS.

FUNCTIONAL BLOCK DIAGRAM



REV. B

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AD9831* PRODUCT PAGE QUICK LINKS

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COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Application Notes

- AN-1044: Programming the AD5932 for Frequency Sweep and Single Frequency Outputs
- AN-1248: SPI Interface
- AN-1389: Recommended Rework Procedure for the Lead Frame Chip Scale Package (LFCSP)
- AN-237: Choosing DACs for Direct Digital Synthesis
- AN-280: Mixed Signal Circuit Technologies
- AN-342: Analog Signal-Handling for High Speed and Accuracy
- AN-345: Grounding for Low-and-High-Frequency Circuits
- AN-419: A Discrete, Low Phase Noise, 125 MHz Crystal Oscillator for the AD9850
- AN-423: Amplitude Modulation of the AD9850 Direct Digital Synthesizer
- AN-543: High Quality, All-Digital RF Frequency Modulation Generation with the ADSP-2181 and the AD9850 DDS
- AN-557: An Experimenter's Project:
- AN-587: Synchronizing Multiple AD9850/AD9851 DDS-Based Synthesizers
- AN-605: Synchronizing Multiple AD9852 DDS-Based Synthesizers
- AN-621: Programming the AD9832/AD9835
- AN-632: Provisionary Data Rates Using the AD9951 DDS as an Agile Reference Clock for the ADN2812 Continuous-Rate CDR
- AN-769: Generating Multiple Clock Outputs from the AD9540
- AN-772: A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)
- AN-823: Direct Digital Synthesizers in Clocking Applications Time
- AN-837: DDS-Based Clock Jitter Performance vs. DAC Reconstruction Filter Performance
- AN-843: Measuring a Loudspeaker Impedance Profile Using the AD5933
- AN-847: Measuring a Grounded Impedance Profile Using the AD5933
- AN-851: A WiMax Double Downconversion IF Sampling Receiver Design

- AN-927: Determining if a Spur is Related to the DDS/DAC or to Some Other Source (For Example, Switching Supplies)
- AN-939: Super-Nyquist Operation of the AD9912 Yields a High RF Output Signal
- AN-953: Direct Digital Synthesis (DDS) with a Programmable Modulus

Data Sheet

- AD9831: 25 MHz Parallel Loading DDS With On-Chip 10-Bit DAC Data Sheet

Product Highlight

- Introducing Digital Up/Down Converters: VersaCOMM™ Reconfigurable Digital Converters

Technical Books

- A Technical Tutorial on Digital Signal Synthesis, 1999

TOOLS AND SIMULATIONS

- ADIsimDDS (Direct Digital Synthesis)

REFERENCE MATERIALS

Technical Articles

- 400-MSample DDSs Run On Only +1.8 VDC
- ADI Buys Korean Mobile TV Chip Maker
- Basics of Designing a Digital Radio Receiver (Radio 101)
- DDS Applications
- DDS Circuit Generates Precise PWM Waveforms
- DDS Design
- DDS Device Produces Sawtooth Waveform
- DDS Device Provides Amplitude Modulation
- DDS IC Initiates Synchronized Signals
- DDS IC Plus Frequency-To-Voltage Converter Make Low-Cost DAC
- DDS Simplifies Polar Modulation
- Digital Potentiometers Vary Amplitude In DDS Devices
- Digital Up/Down Converters: VersaCOMM™ White Paper
- Digital Waveform Generator Provides Flexible Frequency Tuning for Sensor Measurement
- Improved DDS Devices Enable Advanced Comm Systems
- Integrated DDS Chip Takes Steps To 2.7 GHz
- Simple Circuit Controls Stepper Motors
- Speedy A/Ds Demand Stable Clocks
- Synchronized Synthesizers Aid Multichannel Systems
- The Year of the Waveform Generator
- Two DDS ICs Implement Amplitude-shift Keying
- Video Portables and Cameras Get HDMI Outputs

DESIGN RESOURCES

- AD9831 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9831 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

AD9831–SPECIFICATIONS[1] (V_{DD} = +3.3 V ± 10%; +5 V ± 10%; AGND = DGND = 0 V; T_A = T_{MIN} to T_{MAX}; REFIN = REFOUT; R_{SET} = 3.9 kΩ; R_{LOAD} = 300 Ω for IOUT unless otherwise noted)

Parameter	AD9831A	Units	Test Conditions/Comments
SIGNAL DAC SPECIFICATIONS			
Resolution	10	Bits	
Update Rate (f_{MAX})	25	MSPS nom	
I_{OUT} Full Scale	4	mA nom	
	5	mA max	
Output Compliance	1.5	V max	
DC Accuracy			
Integral Nonlinearity	±1	LSB typ	
Differential Nonlinearity	±0.5	LSB typ	
DDS SPECIFICATIONS[2]			
Dynamic Specifications			
Signal to Noise Ratio	50	dB min	f_{MCLK} = 25 MHz, f_{OUT} = 1 MHz
Total Harmonic Distortion	–53	dBc max	f_{MCLK} = 25 MHz, f_{OUT} = 1 MHz
Spurious Free Dynamic Range (SFDR)[3]			f_{MCLK} = 6.25 MHz, f_{OUT} = 2.11 MHz
Narrow Band (±50 kHz)	–72	dBc min	5 V Power Supply
	–70	dBc min	3 V Power Supply
Wide Band (±2 MHz)	–50	dBc min	
Clock Feedthrough	–60	dBc typ	
Wake-Up Time[4]	1	ms typ	
Powerdown Option	Yes		
VOLTAGE REFERENCE			
Internal Reference @ +25°C	1.21	Volts typ	
T_{MIN} to T_{MAX}	1.21 ± 7%	Volts min/max	
REFIN Input Impedance	10	MΩ typ	
Reference TC	100	ppm/°C typ	
REFOUT Output Impedance	300	Ω typ	
LOGIC INPUTS			
V_{INH}, Input High Voltage	V_{DD} – 0.9	V min	
V_{INL}, Input Low Voltage	0.9	V max	
I_{INH}, Input Current	10	μA max	
C_{IN}, Input Capacitance	10	pF max	
POWER SUPPLIES			
AVDD	2.97/5.5	V min/V max	
DVDD	2.97/5.5	V min/V max	
I_{AA}	12	mA max	5 V Power Supply
I_{DD}	2.5 + 0.33/MHz	mA typ	5 V Power Supply
I_{AA} + I_{DD}[5]	15	mA max	3 V Power Supply
	24	mA max	5 V Power Supply
Low Power Sleep Mode[6]	1	mA max	1 MΩ Resistor Tied Between REFOUT and AGND

NOTES
[1]Operating temperature range is as follows: A Version: –40°C to +85°C.
[2]100% production tested.
[3]f_{MCLK} = 6.25 MHz, Frequency Word = 5671C71C HEX, f_{OUT} = 2.11 MHz.
[4]See Figure 11. To reduce the wake-up time at low power supplies and low temperature, the use of an external reference is suggested.
[5]Measured with the digital inputs static and equal to 0 V or DVDD.
[6]The Low Power Sleep Mode current is typically 2 mA when a 1 MΩ resistor is not tied between REFOUT and AGND.
The AD9831 is tested with a capacitive load of 50 pF. The part can be operated with higher capacitive loads, but the magnitude of the analog output will be attenuated. For example, a 5 MHz output signal will be attenuated by 3 dB when the load capacitance equals 85 pF.

Specifications subject to change without notice.

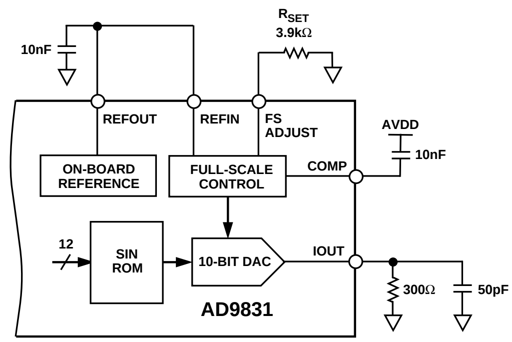


Figure 1. Test Circuit with Which Specifications Are Tested

TIMING CHARACTERISTICS (V_{DD} = +3.3 V ± 10%, +5 V ± 10%; AGND = DGND = 0 V, unless otherwise noted)

Parameter	Limit at T_{MIN} to T_{MAX} (A Version)	Units	Test Conditions/Comments
t_1	40	ns min	MCLK Period
t_2	16	ns min	MCLK High Duration
t_3	16	ns min	MCLK Low Duration
t_4*	8	ns min	$\overline{WR}$ Rising Edge to MCLK Rising Edge
t_{4A}*	8	ns min	$\overline{WR}$ Rising Edge After MCLK Rising Edge
t_5	8	ns min	$\overline{WR}$ Pulse Width
t_6	t_1	ns min	Duration between Consecutive $\overline{WR}$ Pulses
t_7	5	ns min	Data/Address Setup Time
t_8	3	ns min	Data/Address Hold Time
t_9*	8	ns min	FSELECT, PSEL0, PSEL1 Setup Time Before MCLK Rising Edge
t_{9A}*	8	ns min	FSELECT, PSEL0, PSEL1 Setup Time After MCLK Rising Edge
t_{10}	t_1	ns min	$\overline{RESET}$ Pulse Duration

*See Pin Description section.
Guaranteed by design but not production tested.

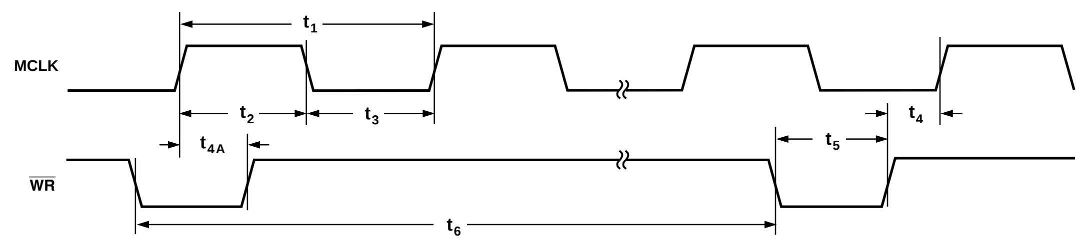


Figure 2. Clock Synchronization Timing

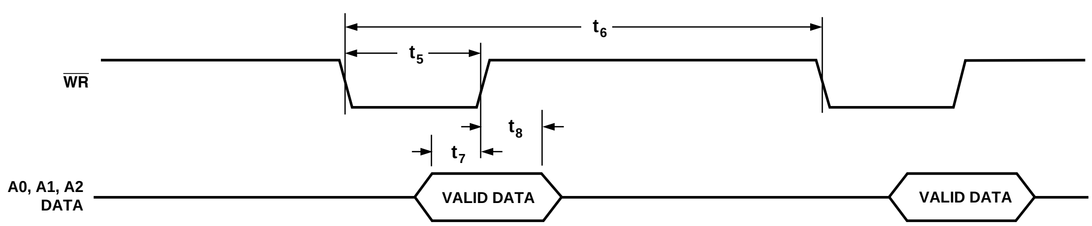


Figure 3. Parallel Timing

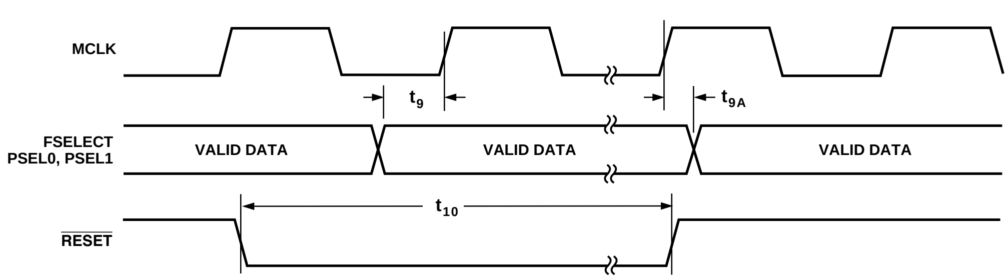


Figure 4. Control Timing

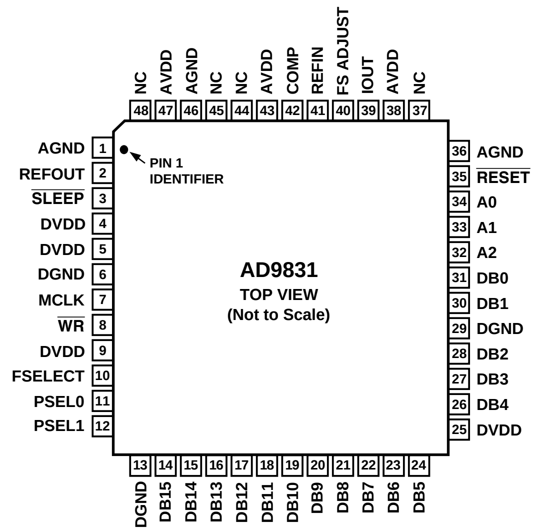
ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

AVDD to AGND . . . . –0.3 V to +7 V
DVDD to DGND . . . . –0.3 V to +7 V
AVDD to DVDD . . . . –0.3 V to +0.3 V
AGND to DGND. . . . . –0.3 V to +0.3 V
Digital I/O Voltage to DGND . . . . . –0.3 V to DVDD + 0.3 V
Analog I/O Voltage to AGND . . . . . –0.3 V to AVDD + 0.3 V
Operating Temperature Range
Industrial (A Version) . . . . –40°C to +85°C
Storage Temperature Range . . . . –65°C to +150°C
Maximum Junction Temperature . . . . +150°C
LQFP θ_{JA} Thermal Impedance . . . . 75°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . +215°C
Infrared (15 sec) . . . . +220°C
ESD Rating . . . . > 4500 V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



NC = NO CONNECT

PIN DESCRIPTION

Mnemonic	Function
POWER SUPPLY	
AVDD	Positive power supply for the analog section. A 0.1 μF decoupling capacitor should be connected between AVDD and AGND. AVDD can have a value of +5 V ± 10% or +3.3 V ± 10%.
AGND	Analog Ground.
DVDD	Positive power supply for the digital section. A 0.1 μF decoupling capacitor should be connected between DVDD and DGND. DVDD can have a value of +5 V ± 10% or +3.3 V ± 10%.
DGND	Digital Ground.
ANALOG SIGNAL AND REFERENCE	
IOUT	Current Output. This is a high impedance current source. A load resistor should be connected between IOUT and AGND.
FS ADJUST	Full-Scale Adjust Control. A resistor (R_{SET}) is connected between this pin and AGND. This determines the magnitude of the full-scale DAC current. The relationship between R_{SET} and the full-scale current is as follows: $IOUT_{FULL\text{-}SCALE} = 12.5 \times V_{REFIN}/R_{SET}$ $V_{REFIN} = 1.21\ V\ nominal,\ R_{SET} = 3.9\ k\Omega\ typical$
REFIN	Voltage Reference Input. The AD9831 can be used with either the on-board reference, which is available from pin REFOUT, or an external reference. The reference to be used is connected to the REFIN pin. The AD9831 accepts a reference of 1.21 V nominal.
REFOUT	Voltage Reference Output. The AD9831 has an on-board reference of value 1.21 V nominal. The reference is made available on the REFOUT pin. This reference is used as the reference to the DAC by connecting REFOUT to REFIN. REFOUT should be decoupled with a 10 nF capacitor to AGND.
COMP	Compensation pin. This is a compensation pin for the internal reference amplifier. A 10 nF decoupling ceramic capacitor should be connected between COMP and AVDD.
DIGITAL INTERFACE AND CONTROL	
MCLK	Digital Clock Input. DDS output frequencies are expressed as a binary fraction of the frequency of MCLK. The output frequency accuracy and phase noise are determined by this clock.
FSELECT	Frequency Select Input. FSELECT controls which frequency register, FREQ0 or FREQ1, is used in the phase accumulator. FSELECT is sampled on the rising MCLK edge. FSELECT needs to be in steady state when an MCLK rising edge occurs. If FSELECT changes value when a rising edge occurs, there is an uncertainty of one MCLK cycle as to when control is transferred to the other frequency register. To avoid any uncertainty, a change on FSELECT should not coincide with an MCLK rising edge.
$\overline{WR}$	Write, Edge-Triggered Digital Input. The $\overline{WR}$ pin is used when writing data to the AD9831. The data is loaded into the AD9831 on the rising edge of the $\overline{WR}$ pulse. This data is then loaded into the destination register on the MCLK rising edge. The $\overline{WR}$ pulse rising edge should not coincide with the MCLK rising edge as there will be an uncertainty of one MCLK cycle regarding the loading of the destination register with the new data. The $\overline{WR}$ rising edge should occur before an MCLK rising edge. The data will then be loaded into the destination register on the MCLK rising edge. Alternatively, the $\overline{WR}$ rising edge can occur after the MCLK rising edge and the destination register will be loaded on the next MCLK rising edge.
D0–D15	Data Bus, Digital Inputs for destination registers.
A0–A2	Address Digital Inputs. These address bits are used to select the destination register to which the digital data is to be written.
PSEL0, PSEL1	Phase Select Input. The AD9831 has four phase registers. These registers can be used to alter the value being input to the SIN ROM. The contents of the phase register can be added to the phase accumulator output, the inputs PSEL0 and PSEL1 selecting the phase register to be used. Like the FSELECT input, PSEL0 and PSEL1 are sampled on the rising MCLK edge. Therefore, these inputs need to be in steady state when an MCLK rising edge occurs or there is an uncertainty of one MCLK cycle as to when control is transferred to the selected phase register.
$\overline{SLEEP}$	Low Power Control, active low digital input. $\overline{SLEEP}$ puts the AD9831 into a low power mode. Internal clocks are disabled and the DAC's current sources and REFOUT are turned off. The AD9831 is re-enabled by taking $\overline{SLEEP}$ high.
$\overline{RESET}$	Reset, active low digital input. $\overline{RESET}$ resets the phase accumulator to zero which corresponds to an analog output of midscale.

TERMINOLOGY

Integral Nonlinearity

This is the maximum deviation of any code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are zero scale, a point 0.5 LSB below the first code transition (000 . . . 00 to 000 . . . 01) and full scale, a point 0.5 LSB above the last code transition (111 . . . 10 to 111 . . . 11). The error is expressed in LSBs.

Differential Nonlinearity

This is the difference between the measured and ideal 1 LSB change between two adjacent codes in the DAC.

Signal to (Noise + Distortion)

Signal to (Noise + Distortion) is measured signal to noise at the output of the DAC. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals up to half the sampling frequency ($f_{MCLK}/2$) but excluding the dc component. Signal to (Noise + Distortion) is dependent on the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical Signal to (Noise + Distortion) ratio for a sine wave input is given by

$$Signal\ to\ (Noise + Distortion) = (6.02N + 1.76)\ \mathrm{dB}$$

where N is the number of bits. Thus, for an ideal 10-bit converter, Signal to (Noise + Distortion) = 61.96 dB.

Total Harmonic Distortion

Total Harmonic Distortion (THD) is the ratio of the rms sum of harmonics to the rms value of the fundamental. For the AD9831, THD is defined as

$$THD = 20 \log \frac{\sqrt{(V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonic.

Output Compliance

The output compliance refers to the maximum voltage which can be generated at the output of the DAC to meet the specifications. When voltages greater than that specified for the output compliance are generated, the AD9831 may not meet the specifications listed in the data sheet.

Spurious Free Dynamic Range

Along with the frequency of interest, harmonics of the fundamental frequency and images of the MCLK frequency are present at the output of a DDS device. The spurious free dynamic range (SFDR) refers to the largest spur or harmonic which is present in the band of interest. The wide band SFDR gives the magnitude of the largest harmonic or spur relative to the magnitude of the fundamental frequency in the bandwidth ±2 MHz about the fundamental frequency. The narrow band SFDR gives the attenuation of the largest spur or harmonic in a bandwidth of ±50 kHz about the fundamental frequency.

Clock Feedthrough

There will be feedthrough from the MCLK input to the analog output. Clock feedthrough refers to the magnitude of the MCLK signal relative to the fundamental frequency in the AD9831's output spectrum.

Table I. Control Registers

Register	Size	Description
FREQ0 REG	32 Bits	Frequency Register 0. This defines the output frequency, when FSELECT = 0, as a fraction of the MCLK frequency.
FREQ1 REG	32 Bits	Frequency Register 1. This defines the output frequency, when FSELECT = 1, as a fraction of the MCLK frequency.
PHASE0 REG	12 Bits	Phase Offset Register 0. When PSEL0 = PSEL1 = 0, the contents of this register are added to the output of the phase accumulator.
PHASE1 REG	12 Bits	Phase Offset Register 1. When PSEL0 = 1 and PSEL1 = 0, the contents of this register are added to the output of the phase accumulator.
PHASE2 REG	12 Bits	Phase Offset Register 2. When PSEL0 = 0 and PSEL1 = 1, the contents of this register are added to the output of the phase accumulator.
PHASE3 REG	12 Bits	Phase Offset Register 3. When PSEL0 = PSEL1 = 1, the contents of this register are added to the output of the phase accumulator.

Table II. Addressing the Control Registers

A2	A1	A0	Destination Register
0	0	0	FREQ0 REG 16 LSBs
0	0	1	FREQ0 REG 16 MSBs
0	1	0	FREQ1 REG 16 LSBs
0	1	1	FREQ1 REG 16 MSBs
1	0	0	PHASE0 REG
1	0	1	PHASE1 REG
1	1	0	PHASE2 REG
1	1	1	PHASE3 REG

Table III. Frequency Register Bits

D15															D0
MSB															LSB

Table IV. Phase Register Bits

D15	D14	D13	D12	D11											D0
X	X	X	X	MSB											LSB

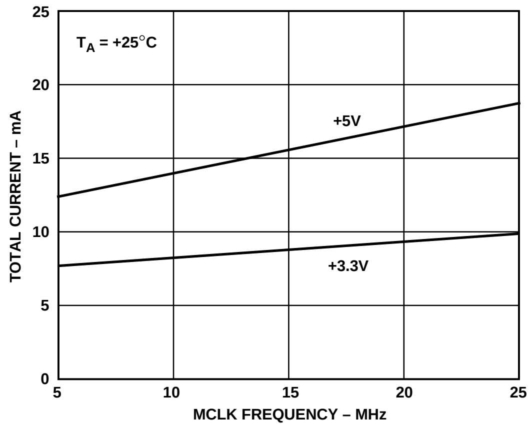


Figure 5. Typical Current Consumption vs. MCLK Frequency

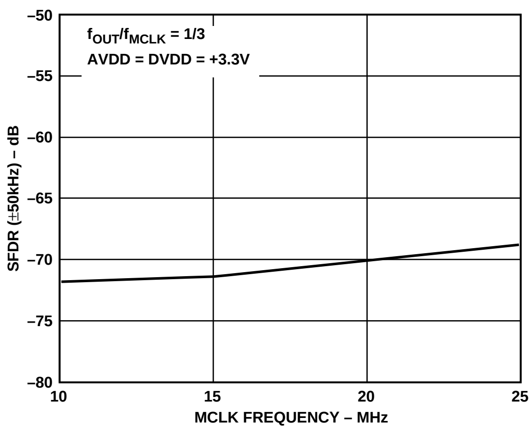


Figure 6. Narrow Band SFDR vs. MCLK Frequency

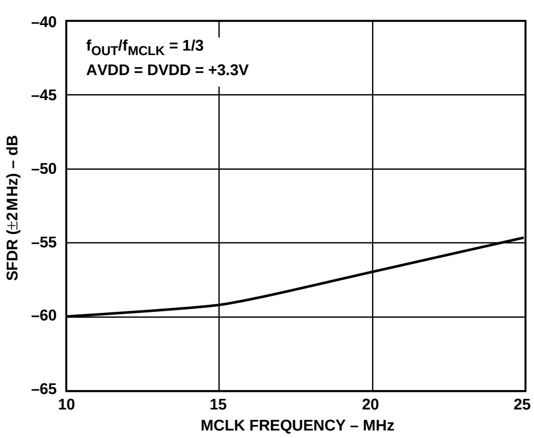


Figure 7. Wide Band SFDR vs. MCLK Frequency

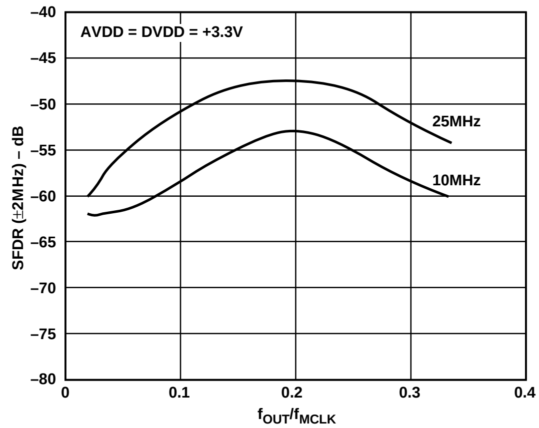


Figure 8. Wide Band SFDR vs. f_{OUT}/f_{MCLK} for Various MCLK Frequencies

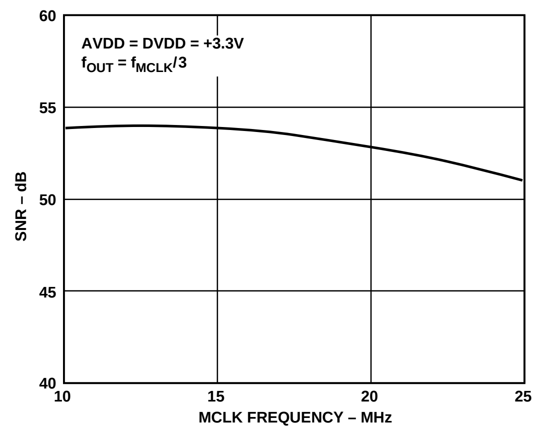


Figure 9. SNR vs. MCLK Frequency

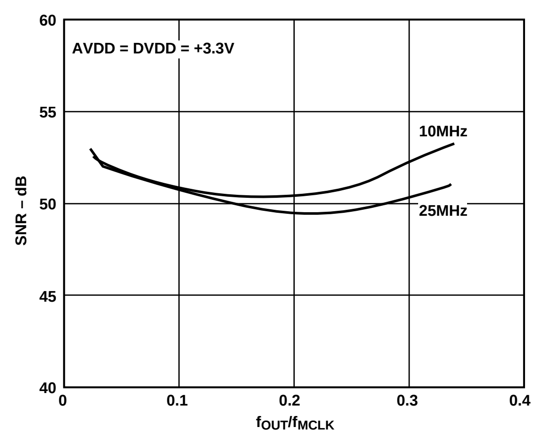


Figure 10. SNR vs. f_{OUT}/f_{MCLK} for Various MCLK Frequencies

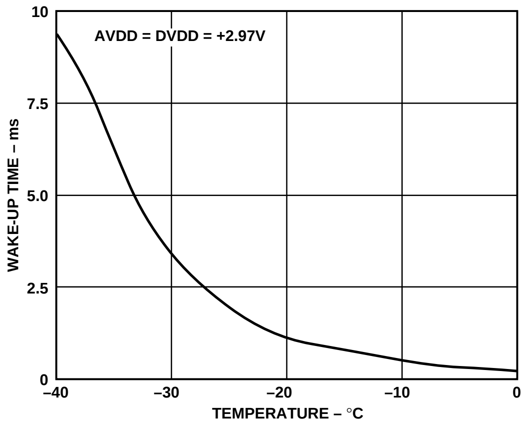


Figure 11. Wake-Up Time vs. Temperature

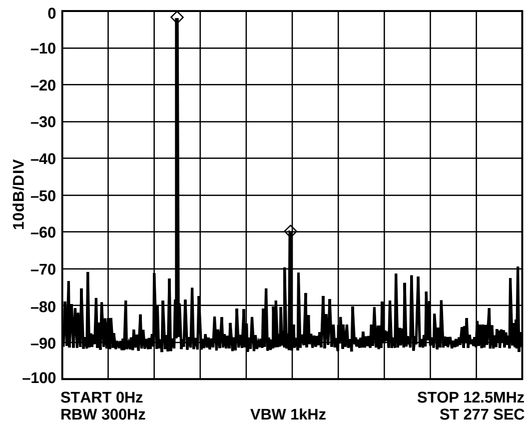


Figure 14. f_{MCLK} = 25 MHz, f_{OUT} = 3.1 MHz, Frequency Word = 1FBE76C9

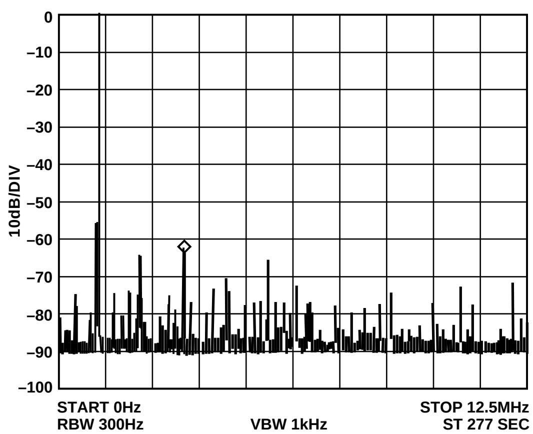


Figure 12. f_{MCLK} = 25 MHz, f_{OUT} = 1.1 MHz, Frequency Word = B439581

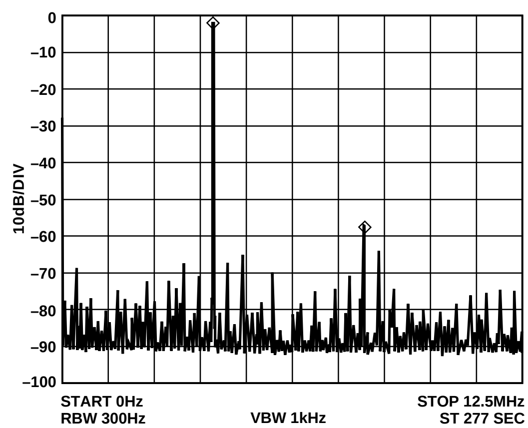


Figure 15. f_{MCLK} = 25 MHz, f_{OUT} = 4.1 MHz, Frequency Word = 29FBE76D

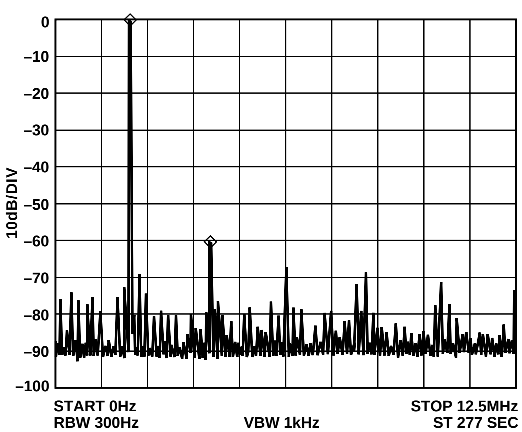


Figure 13. f_{MCLK} = 25 MHz, f_{OUT} = 2.1 MHz, Frequency Word = 15810625

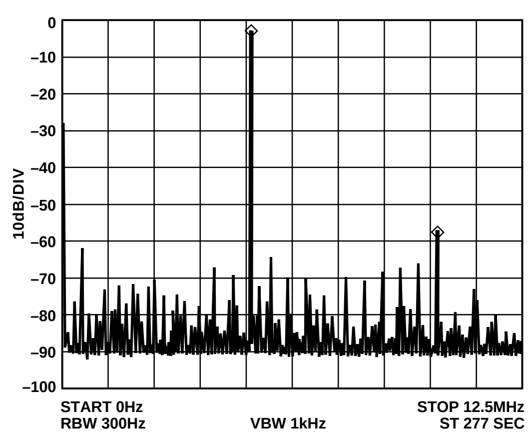


Figure 16. f_{MCLK} = 25 MHz, f_{OUT} = 5.1 MHz, Frequency Word = 34395810

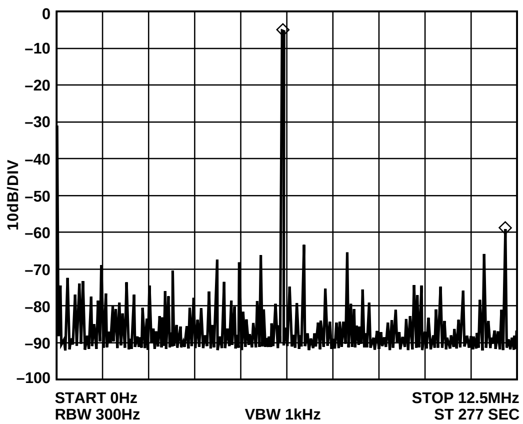


Figure 17. f_{MCLK} = 25 MHz, f_{OUT} = 6.1 MHz, Frequency Word = 3E76C8B4

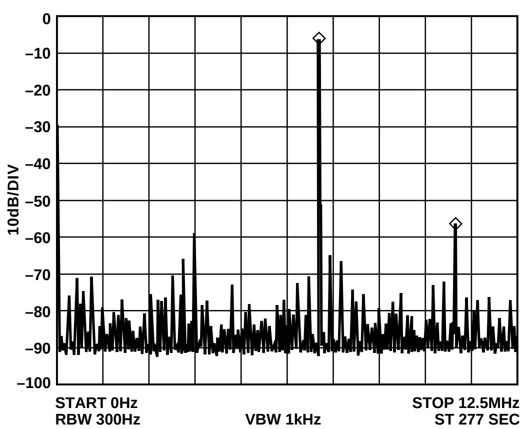


Figure 18. f_{MCLK} = 25 MHz, f_{OUT} = 7.1 MHz, Frequency Word = 48B43958

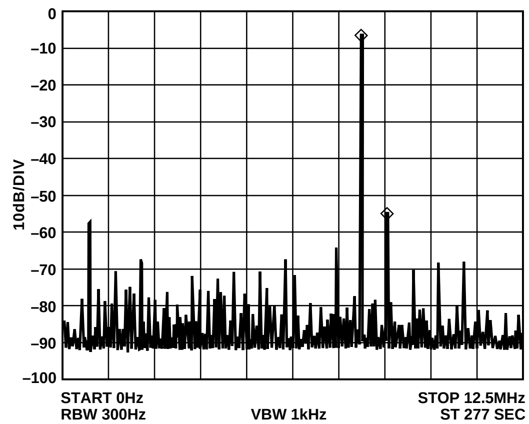


Figure 19. f_{MCLK} = 25 MHz, f_{OUT} = 8.1 MHz, Frequency Word = 52F1A9FC

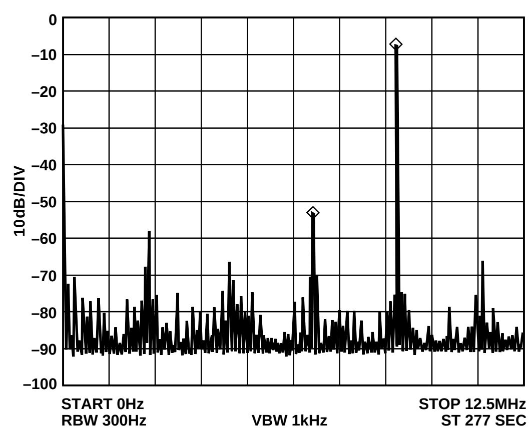


Figure 20. f_{MCLK} = 25 MHz, f_{OUT} = 9.1 MHz, Frequency Word = 5D2F1AA0

CIRCUIT DESCRIPTION

The AD9831 provides an exciting new level of integration for the RF/Communications system designer. The AD9831 combines the Numerical Controlled Oscillator (NCO), SINE Look-Up Table, Frequency and Phase Modulators, and a Digital-to-Analog Converter on a single integrated circuit.

The internal circuitry of the AD9831 consists of three main sections. These are:

Numerical Controlled Oscillator (NCO) + Phase Modulator

SINE Look-Up Table

Digital-to-Analog Converter

The AD9831 is a fully integrated Direct Digital Synthesis (DDS) chip. The chip requires one reference clock, one low precision resistor and eight decoupling capacitors to provide digitally created sine waves up to 12.5 MHz. In addition to the generation of this RF signal, the chip is fully capable of a broad range of simple and complex modulation schemes. These modulation schemes are fully implemented in the digital domain allowing accurate and simple realization of complex modulation algorithms using DSP techniques.

THEORY OF OPERATION

Sine waves are typically thought of in terms of their magnitude form a(t) = sin (ωt). However, these are nonlinear and not easy to generate except through piece wise construction. On the other hand, the angular information is linear in nature. That is, the phase angle rotates through a fixed angle for each unit of time. The angular rate depends on the frequency of the signal by the traditional rate of $\omega = 2\pi f$.

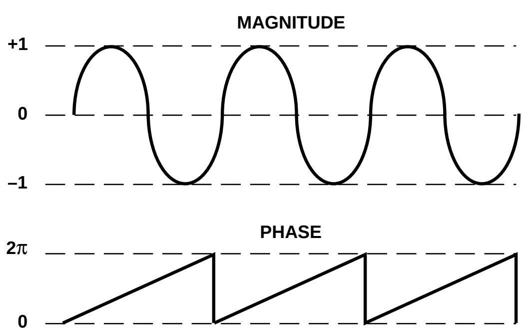


Figure 21. Sine Wave

Knowing that the phase of a sine wave is linear and given a reference interval (clock period), the phase rotation for that period can be determined.

$$\Delta Phase = \omega \delta t$$

Solving for ω

$$\omega = \Delta Phase/\delta t = 2\pi f$$

Solving for f and substituting the reference clock frequency for the reference period ($1/f_{MCLK} = \delta t$)

$$f = \Delta Phase \times f_{MCLK}/2\pi$$

The AD9831 builds the output based on this simple equation. A simple DDS chip can implement this equation with three major subcircuits.

Numerical Controlled Oscillator + Phase Modulator

This consists of two frequency select registers, a phase accumulator and four phase offset registers. The main component of the NCO is a 32-bit phase accumulator which assembles the phase component of the output signal. Continuous time signals have a phase range of 0 to 2π. Outside this range of numbers, the sinusoid functions repeat themselves in a periodic manner. The digital implementation is no different. The accumulator simply scales the range of phase numbers into a multibit digital word. The phase accumulator in the AD9831 is implemented with 32 bits. Therefore, in the AD9831, $2\pi = 2^{32}$. Likewise, the $\Delta Phase$ term is scaled into this range of numbers $0 < \Delta Phase < 2^{32} - 1$. Making these substitutions into the equation above

$$f = \Delta Phase \times f_{MCLK}/2^{32}$$

where $0 < \Delta Phase < 2^{32}$

With a clock signal of 25 MHz and a phase word of 051EB852 hex

$$f = 51EB852 \times 25\ MHz/2^{32} = 0.500000000465\ MHz$$

The input to the phase accumulator (i.e., the phase step) can be selected either from the FREQ0 Register or FREQ1 Register and this is controlled by the FSELECT pin. NCOs inherently generate continuous phase signals, thus avoiding any output discontinuity when switching between frequencies.

Following the NCO, a phase offset can be added to perform phase modulation using the 12-bit PHASE Registers. The contents of this register are added to the most significant bits of the NCO. The AD9831 has four PHASE registers, the resolution of these registers being 2π/4096.

Sine Look-Up Table (LUT)

To make the output useful, the signal must be converted from phase information into a sinusoidal value. Since phase information maps directly into amplitude, a ROM LUT converts the phase information into amplitude. To do this, the digital phase information is used to address a sine ROM LUT. Although the NCO contains a 32-bit phase accumulator, the output of the NCO is truncated to 12 bits. Using the full resolution of the phase accumulator is impractical and unnecessary as this would require a look-up table of 2^{32} entries.

It is necessary only to have sufficient phase resolution in the LUTs such that the dc error of the output waveform is dominated by the quantization error in the DAC. This requires the look-up table to have two more bits of phase resolution than the 10-bit DAC.

Digital-to-Analog Converter

The AD9831 includes a high impedance current source 10-bit DAC, capable of driving a wide range of loads at different speeds. Full-scale output current can be adjusted, for optimum power and external load requirements, through the use of a single external resistor (R_{SET}).

The DAC is configured for single ended operation. The load resistor can be any value required, as long as the full-scale voltage developed across it does not exceed the voltage compliance range. Since full-scale current is controlled by R_{SET}, adjustments to R_{SET} can balance changes made to the load resistor. However, if the DAC full-scale output current is significantly less than 4 mA, the DAC's linearity may degrade.

DSP and MPU Interfacing

The AD9831 has a parallel interface, with 16 bits of data being loaded during each write cycle.

The frequency or phase registers are loaded by asserting the $\overline{WR}$ signal. The destination register for the 16 bit data is selected using the address inputs A0, A1 and A2. The phase registers are 12 bits wide so, only the 12 LSBs need to be valid—the 4 MSBs of the 16 bit word do not have to contain valid data. Data is loaded into the AD9831 by pulsing $\overline{WR}$ low, the data being latched into the AD9831 on the rising edge of $\overline{WR}$. The values of inputs A0, A1 and A2 are also latched into the AD9831 on the $\overline{WR}$ rising edge. The appropriate destination register is updated on the next MCLK rising edge. If the $\overline{WR}$ rising edge coincides with the MCLK rising edge, there is an uncertainty of one MCLK cycle regarding the loading of the destination register—the destination register may be loaded immediately or the destination register may be updated on the next MCLK rising edge. To avoid any uncertainty, the times listed in the specifications should be complied with.

FSELECT, PSEL0 and PSEL1 are sampled on the MCLK rising edge. Again, these inputs should be valid when an MCLK rising edge occurs as there will be an uncertainty of one MCLK cycle introduced otherwise. When these inputs change value, there will be a pipeline delay before control is transferred to the selected register—there will be a pipeline delay before the analog output is controlled by the selected register. There is a similar delay when a new word is written to a register. PSEL0, PSEL1, FSELECT and $\overline{WR}$ have latencies of six MCLK cycles.

The flow chart in Figure 22 shows the operating routine for the AD9831. When the AD9831 is powered up, the part should be reset using $\overline{RESET}$. This will reset the phase accumulator to zero so that the analog output is at midscale. $\overline{RESET}$ does not reset the phase and frequency registers. These registers will contain invalid data and, therefore, should be set to zero by the user.

The registers to be used should be loaded, the analog output being $f_{MCLK}/2^{32} \times$ FREG where FREG is the value loaded into the selected frequency register. This signal will be phase shifted by the amount specified in the selected phase register ($2\pi/4096 \times$ PHASEREG where PHASEREG is the value contained in the selected phase register). When FSELECT, PSEL0 and PSEL1 are programmed, there will be a pipeline delay of approximately 6 MCLK cycles before the analog output reacts to the change on these inputs.

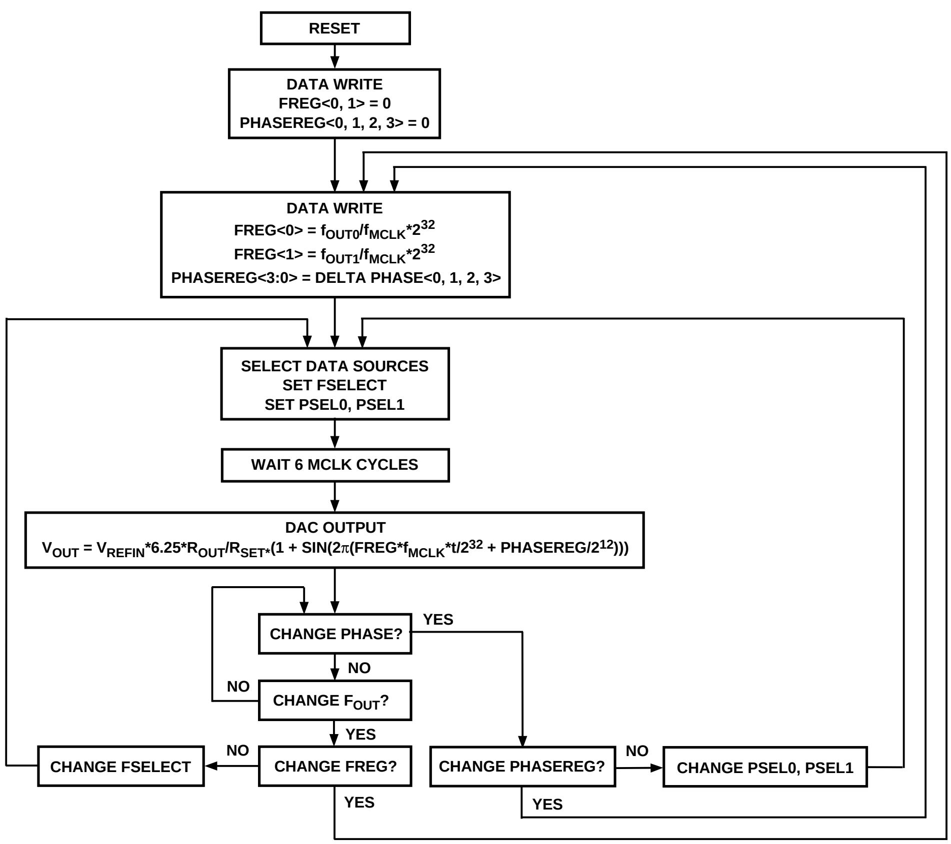


Figure 22. Flow Chart for AD9831 Initialization and Operation

APPLICATIONS

The AD9831 contains functions which make it suitable for modulation applications. The part can be used to perform simple modulation such as FSK. More complex modulation schemes such as GMSK and QPSK can also be implemented using the AD9831. In an FSK application, the two frequency registers of the AD9831 are loaded with different values; one frequency will represent the space frequency while the other will represent the mark frequency. The digital data stream is fed to the FSELECT pin which will cause the AD9831 to modulate the carrier frequency between the two values.

The AD9831 has four phase registers; this enables the part to perform PSK. With phase shift keying, the carrier frequency is phase shifted, the phase being altered by an amount which is related to the bit stream being input to the modulator. The presence of four shift registers eases the interaction needed between the DSP and the AD9831.

The frequency and phase registers can be written to continuously, if required. The maximum update rate equals the frequency of the MCLK. However, if a selected register is loaded with a new word, there will be a delay of 6 MCLK cycles before the analog output will change accordingly.

The AD9831 is also suitable for signal generator applications. With its low current consumption, the part is suitable for applications in which it can be used as a local oscillator. In addition, the part is fully specified for operation with a +3.3 V ± 10% power supply. Therefore, in portable applications where current consumption is an important issue, the AD9831 is perfect.

Grounding and Layout

The printed circuit board that houses the AD9831 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes which can be separated easily. A minimum etch technique is generally best for ground planes as it gives the best shielding. Digital and analog ground planes should only be joined in one place. If the AD9831 is the only device requiring an AGND to DGND connection, then the ground planes should be connected at the AGND and DGND pins of the AD9831. If the AD9831 is in a system where multiple devices require AGND to DGND connections, the connection should be made at one point only, a star ground point that should be established as close as possible to the AD9831.

Avoid running digital lines under the device as these will couple noise onto the die. The analog ground plane should be allowed to run under the AD9831 to avoid noise coupling. The power supply lines to the AD9831 should use as large a track as is possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other sections of the board. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This will reduce the effects of feedthrough through the board. A microstrip technique is by far the best but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes while signals are placed on the other side.

Good decoupling is important. The analog and digital supplies to the AD9831 are independent and separately pinned out to minimize coupling between analog and digital sections of the device. All analog and digital supplies should be decoupled to AGND and DGND respectively with 0.1 μF ceramic capacitors in parallel with 10 μF tantalum capacitors. To achieve the best from the decoupling capacitors, they should be placed as close as possible to the device, ideally right up against the device. In systems where a common supply is used to drive both the AVDD and DVDD of the AD9831, it is recommended that the system's AVDD supply be used. This supply should have the recommended analog supply decoupling between the AVDD pins of the AD9831 and AGND and the recommended digital supply decoupling capacitors between the DVDD pins and DGND.

Evaluation boards are available for the AD9832, the AD9833, and the AD9837, which are similar in functionality to the AD9831. For more information on these parts, visit http://www.analog.com/DDS.

OUTLINE DIMENSIONS

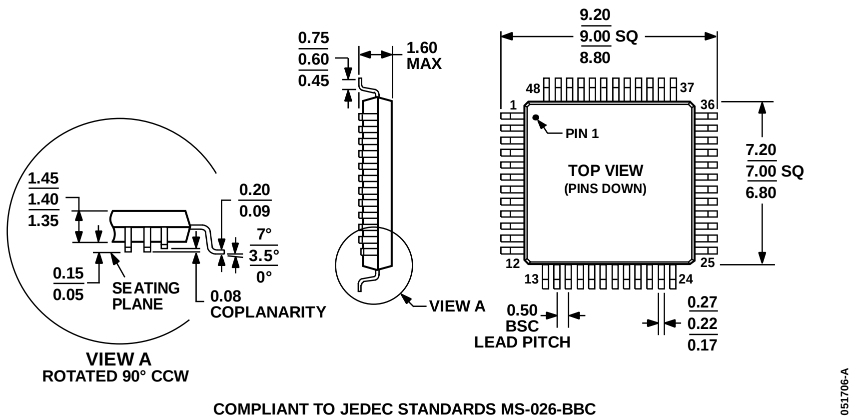


Figure 23. 48-Lead Low Profile Quad Flat Package (LQFP)
(ST-48)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9831ASTZ	–40°C to +85°C	48-Lead Low Profile Quad Flat Package [LQFP]	ST-48
AD9831ASTZ-REEL	–40°C to +85°C	48-Lead Low Profile Quad Flat Package [LQFP]	ST-48

[1] Z = RoHS Compliant Part.

REVISION HISTORY

11/11—Rev. A to Rev. B

Changes to Title and General Description Section 1
Changed TQFP to LQFP Throughout..1
Changes to Grounding and Layout Section.................................12
Deleted AD9831 Evaluation Board, Using the AD9831 Evaluation Board, Prototyping Area, XO vs. External Clock, and Power Supply Sections 13
Deleted Figure 23; Renumbered Sequentially.............................13
Updated Outline Dimensions...13
Changes to Ordering Guide..13
Deleted Figure 24 and Component List Section.........................14

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