

PRODUCT CHANGE NOTIFICATION



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PCN#030217

Subject: Notification of Change for the LTM4675 and LTM4677 μ Module Regulators

Dear Sir/Madam:

Please be advised that Linear Technology Corporation has made enhancements to the electrical specifications of the LTM4675 and LTM4677 μ Module regulators. The improvements to the electrical specifications are listed below:

- 1) **Reduced power up times**
- 2) **Improved on-chip EEPROM robustness**
- 3) **Reduced ADC update period**
- 4) **Reduced TON_MIN**
- 5) **Updated I²C PMBus voltage thresholds compatible with bus power supplies as low as 1.8 volts**

Table 1- Summary of Improvements to the LTM4675 and LTM4677 μ Module Regulators

Parameters	New Version	Old Version
Turn-On Start-Up Time (t_{START})	35ms	60ms
Minimum On-Time ($T_{ON(MIN)}$)	45ns	90ns
NVM Protected by ECC	Yes	No
ADC Telemetry Update Period ($t_{CONVERT-*}$)	90ms	100ms
V_{IL} Logic Thresholds of the Following Pins: SCL, SDA, RUN ₀ , RUN ₁ , GPIO ₀ , GPIO ₁	0.8V	1.4V
V_{IH} Logic Thresholds of the Following Pins: SCL, SDA, RUN ₀ , RUN ₁ , GPIO ₀ , GPIO ₁	1.35V	2.0V

- T_{INIT} , the time required from application of VIN until the part is ready to start sequencing output rails, is reduced from a typical value of 60ms to 35ms. This change is transparent in all applications that require sequencing of multiple power rails using multiple LTC Power System Management (PSM) parts connected in the recommended manner.
- Error Correcting Code (ECC) is added to the internal non-volatile memory to enhance its reliability. This change is transparent to the user and requires no modifications to programming files or system firmware. As a consequence of adding ECC, the area in the EEPROM available for fault log is reduced to 4 events. The read length of 147 bytes remains the same but the fifth and sixth events are a repeat of the fourth event if the part is reset. However, when reading the fault log from RAM, all 6 events of cyclical data are available.
- The ADC update period, $T_{CONVERT}$, is reduced from 100ms to 90ms, providing more timely telemetry of all monitored parameters.
- TON_MIN is reduced from nominally 90ns to 45ns to support large step down ratios at relatively high switching frequencies.
- I²C thresholds are reduced to support PMBus communication with other ICs using I/O interface supplies as low as 1.8 volts. The V_{IL} and V_{IH} specifications for the SDA, SCL, RUN0, RUN1, GPIO0 and GPIO1 pins are reduced from 1.4V and 2.0V, respectively, to 0.8V and 1.35V. The LTM4675 and LTM4677 are fully compliant with PMBus 1.2. For more details, please refer to PMBus 1.2 revisions on the PMBus website <http://pmbus.org/Specifications/OlderSpecifications> and the SMBus Specification Version 2.0 at <http://smbus.org/specs/smbus20.pdf>.

Changes to the product datasheet electrical characteristics tables are appended to this notice.

The only change to the PWM characteristics is the reduction in TON_MIN. These die-level changes to the modules' control IC were qualified by performing module-level characterization over the full operating junction temperature range and through rigorous engineering evaluation across a broad range of application conditions. The revised control IC has successfully completed 1000 hours burn-in.

The new devices can be identified with the PMBus MFR_SPECIAL_ID command code reporting a value of 0x47XY where 'Y' is a hex value of 0x8-0xF and 'X' is a hex value 0xA for LTM4675 and 0xB for LTM4677. The affected part numbers are listed below.

List of affected part numbers:

LTM4675EY#PBF
LTM4675IY#PBF
LTM4675IY

LTM4677EY#PBF
LTM4677IY#PBF
LTM4677IY

Linear Technology will accept requests for revised samples within 30 days of the date of this notification. If we don't hear back from your company within this 30 day period, we will assume acceptance of this Change Notice by May 02, 2017. After this time, Linear Technology may not be able to accommodate customer requests to receive older product. Samples of the revised module are available now and production product built using the new control IC will be shipped no sooner than May 02, 2017.

Should you have any further questions, please feel free to contact your local Linear Technology sales person or you may contact me at 408-432-1900 ext. 2077, or by E-mail JASON.HU@LINEAR.COM.

Sincerely,

Jason Hu
Quality Assurance Engineer

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SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN}	Input DC Voltage	Test Circuit 1 Test Circuit 2; $V_{IN_OFF} < V_{IN_ON} = 4.25\text{V}$	● 5.75 ● 4.5		17 5.75	V
V_{OUTn}	Range of Output Voltage Regulation	V_{OUT0} Differentially Sensed on V_{OSNS0+}/V_{OSNS0-} Pin-Pair; V_{OUT1} Differentially Sensed on V_{OSNS1+}/V_{OSNS1-} Pin-Pair; Commanded by Serial Bus or with Resistors Present at Start-Up on $V_{OUTnCFG}$ and/or $V_{TRIMnCFG}$	● 0.5 ● 0.5		5.5 5.5	V
$V_{OUTn(DC)}$	Output Voltage, Total Variation with Line and Load	(Note 5) V_{OUTn} Low Range (MFR_PWM_MODE _n [1] = 1 _b), FREQUENCY_SWITCH = 425kHz) Digital Servo Engaged (MFR_PWM_MODE _n [6] = 1 _b) Digital Servo Disengaged (MFR_PWM_MODE _n [6] = 0 _b)	● 0.995 ● 0.985	1.000 1.000	1.005 1.015	V
Input Specifications						
$I_{INRUSH(VIN)}$	Input Inrush Current at Start-Up	Test Circuit 1, $V_{OUTn} = 1\text{V}$, $V_{IN} = 12\text{V}$; No Load Besides Capacitors; $\text{TON_RISE}_n = 3\text{ms}$		400		mA
$I_{Q(SVIN)}$	Input Supply Bias Current	Forced Continuous Mode, MFR_PWM_MODE _n [0] = 1 _b $\text{RUN}_n = 5\text{V}$, $\text{RUN}_{1-n} = 0\text{V}$ Shutdown, $\text{RUN}_0 = \text{RUN}_1 = 0\text{V}$		40 20		mA mA
$I_S(VINn,PSM)$	Input Supply Current in Pulse-Skipping Mode Operation	Pulse-Skipping Mode, MFR_PWM_MODE _n [0] = 0 _b , $I_{OUTn} = 100\text{mA}$		20		mA
$I_S(VINn,FCM)$	Input Supply Current in Forced-Continuous Mode Operation	Forced Continuous Mode, MFR_PWM_MODE _n [0] = 1 _b $I_{OUTn} = 100\text{mA}$ $I_{OUTn} = 9\text{A}$		40 927		mA mA
$I_S(VINn,SHUTDOWN)$	Input Supply Current in Shutdown	Shutdown, $\text{RUN}_n = 0\text{V}$		50		μA
Output Specifications						
I_{OUTn}	Output Continuous Current Range	(Note 6)		0	9	A
$\frac{\Delta V_{OUTn(LINE)}}{V_{OUTn}}$	Line Regulation Accuracy	Digital Servo Engaged (MFR_PWM_MODE _n [6] = 1 _b) Digital Servo Disengaged (MFR_PWM_MODE _n [6] = 0 _b) S_{VIN} and V_{INn} Electrically Shorted Together and INTV _{CC} Open Circuit; $I_{OUTn} = 0\text{A}$, $5.75\text{V} \leq V_{IN} \leq 17\text{V}$, V_{OUT} Low Range (MFR_PWM_MODE _n [1] = 1 _b) FREQUENCY_SWITCH = 425kHz (Referenced to 12V _{IN}) (Note 5)	●	0.03 0.03	±0.2	% %/V
$\frac{\Delta V_{OUTn(LOAD)}}{V_{OUTn}}$	Load Regulation Accuracy	Digital Servo Engaged (MFR_PWM_MODE _n [6] = 1 _b) Digital Servo Disengaged (MFR_PWM_MODE _n [6] = 0 _b) $0\text{A} \leq I_{OUTn} \leq 9\text{A}$, V_{OUT} Low Range, (MFR_PWM_MODE _n [1] = 1 _b) FREQUENCY_SWITCH = 425kHz (Note 5)	●	0.03 0.2	0.5	% %
$V_{OUTn(AC)}$	Output Voltage Ripple			10		mVp-p
f_S (Each Channel)	V_{OUTn} Ripple Frequency	FREQUENCY_SWITCH Set to 500kHz (0xFBE8)	●	462.5	500 537.5	kHz
$\Delta V_{OUTn(START)}$	Turn-On Overshoot	$\text{TON_RISE}_n = 3\text{ms}$ (Note 12)		8		mV
t_{START}	Turn-On Start-Up Time	Time from V_{IN} Toggling from 0V to 12V to Rising Edge of GPIO _n , $\text{TON_DELAY}_n = 0\text{ms}$, $\text{TON_RISE}_n = 3\text{ms}$, MFR_GPIO_PROPAGATE _n = 0x0100, MFR_GPIO_RESPONSE _n = 0x0000	●		60 70	ms



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SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$t_{\text{DELAY}}(\text{0ms})$	Turn-On Delay Time	Time from First Rising Edge of RUN_n to Rising Edge of $\overline{\text{GPIO}}_n$. TON_DELAY _n = 0ms, TON_RISE _n = 3ms, MFR_GPIO_PROPAGATE _n = 0x0100, MFR_GPIO_RESPONSE _n = 0x0000. V_{IN} Having Been Established for at Least 70ms	● 2.75	3.1	3.5	ms
$\Delta V_{\text{OUT}_n}(\text{LS})$	Peak Output Voltage Deviation for Dynamic Load Step	Load: 0A to 4.5A and 4.5A to 0A at 4.5A/ μs , Figure 60 Circuit, $V_{\text{OUT}_n} = 1\text{V}$, $V_{IN} = 12\text{V}$ (Note 12)		50		mV
t_{SETTLE}	Settling Time for Dynamic Load Step	Load: 0A to 4.5A and 4.5A to 0A at 4.5A/ μs , Figure 60 Circuit, $V_{\text{OUT}_n} = 1\text{V}$, $V_{IN} = 12\text{V}$ (Note 12)		35		μs
$I_{\text{OUT}_n}(\text{OCL_PK})$	Output Current Limit, Peak	Cycle-by-Cycle Inductor Peak Current Limit Inception		15.8		A
$I_{\text{OUT}_n}(\text{OCL_AVG})$	Output Current Limit, Time Averaged	Time-Averaged Output Inductor Current Limit Inception Threshold, Commanded by IOUT_OC_FAULT_LIMIT _n (Note 12)		10.8A; See I _{O-RB-ACC} Specification (Output Current Readback Accuracy)		
Control Section						
$V_{\text{FB}0}$	Channel 0 Feedback Input Common Mode Range	$V_{\text{OSNS}0^-}$ Valid Input Range (Referred to SGND) $V_{\text{OSNS}0^+}$ Valid Input Range (Referred to SGND)	●	-0.1	0.3	V
$V_{\text{FB}1}$	Channel 1 Feedback Input Common Mode Range	SGND Valid Input Range (Referred to GND) $V_{\text{OSNS}1}$ Valid Input Range (Referred to SGND)	●	-0.3	0.3	V
$V_{\text{OUT-RNG}0}$	Full-Scale Command Voltage, Range 0	(Notes 7, 15) V_{OUT_n} Commanded to 5.500V, MFR_PWM_MODE _n [1] = 0 _b Resolution LSB Step Size		5.422	5.576	V Bits mV
$V_{\text{OUT-RNG}1}$	Full-Scale Command Voltage, Range 1	(Notes 7, 15) V_{OUT_n} Commanded to 2.750V, MFR_PWM_MODE _n [1] = 1 _b Resolution LSB Step Size		2.711	2.788	V Bits mV
$R_{\text{VSENSE}0^+}$	$V_{\text{OSNS}0^+}$ Impedance to SGND	$0.05\text{V} \leq V_{\text{OSNS}0^+} - V_{\text{SGND}} \leq 5.5\text{V}$		41		k Ω
$R_{\text{VSENSE}1}$	$V_{\text{OSNS}1}$ Impedance to SGND	$0.05\text{V} \leq V_{\text{OSNS}1} - V_{\text{SGND}} \leq 5.5\text{V}$		37		k Ω
$t_{\text{ON}(\text{MIN})}$	Minimum On-Time	(Note 8)		90		ns
Analog OV/UV (Overvoltage/Undervoltage) Output Voltage Supervisor Comparators (VOUT_OV/UV_FAULT_LIMIT and VOUT_OV/UV_WARN_LIMIT Monitors)						
$N_{\text{OV/UV_COMP}}$	Resolution, Output Voltage Supervisors	(Note 15)		8		Bits
$V_{\text{OV-RNG}}$	Output OV Comparator Threshold Detection Range	(Note 15) High Range Scale, MFR_PWM_MODE _n [1] = 0 _b Low Range Scale, MFR_PWM_MODE _n [1] = 1 _b		1	5.6	V
$V_{\text{OU-STP}}$	Output OV and UV Comparator Threshold Programming LSB Step Size	(Note 15) High Range Scale, MFR_PWM_MODE _n [1] = 0 _b Low Range Scale, MFR_PWM_MODE _n [1] = 1 _b		22	11	mV mV

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SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$t_{\text{CONVERT-VO-RB}}$	Output Voltage Readback Update Rate	MFR_ADC_CONTROL=0x00 (Notes 9, 15)		-100		ms
		MFR_ADC_CONTROL=0x0D (Notes 9, 15)		27		ms
		MFR_ADC_CONTROL=0x05 or 0x09 (Notes 9, 15)		8		ms
Input Voltage (SV_{IN}) Readback (READ_VIN)						
$N_{\text{SVIN-RB}}$	Input Voltage Readback Resolution and LSB Step Size	(Notes 10, 15)		10		Bits
				15.625		mV
$SV_{IN-F/S}$	Input Voltage Full-Scale Digitizable Range	(Notes 11, 15)		38.91		V
$SV_{IN-RB-ACC}$	Input Voltage Readback Accuracy	READ_VIN , $4.5\text{V} \leq SV_{IN} \leq 17\text{V}$	●	Within $\pm 2\%$ of Reading		
$t_{\text{CONVERT-SVIN-RB}}$	Input Voltage Readback Update Rate	MFR_ADC_CONTROL=0x00 (Notes 9, 15)		-100		ms
		MFR_ADC_CONTROL=0x01 (Notes 9, 15)		8		ms
Channels 0 and 1 Output Current (READ_IOUT_n), Duty Cycle (READ_DUTY_CYCLE_n), and Computed Input Current (MFR_READ_IIN_n) Readback						
$N_{\text{IO-RB}}$	Output Current Readback Resolution and LSB Step Size	(Notes 10, 12)		10		Bits
				15.6		mA
IO-F/S , II-F/S	Output Current Full-Scale Digitizable Range and Input Current Range of Calculation	(Note 12)		± 40		A
IO-RB-ACC	Output Current, Readback Accuracy	READ_IOUT_n , Channels 0 and 1, $0 \leq \text{IOUT}_n \leq 9\text{A}$, Forced-Continuous Mode, $\text{MFR_PWM_MODE}_n[1:0] = 10_b$	●	Within 225mA of Reading		
IO-RB(9A)	Full Load Output Current Readback	$\text{IOUT}_n = 9\text{A}$ (Note 12). See Histograms in Typical Performance Characteristics		9		A
$N_{\text{II-RB}}$	Computed Input Current, Readback Resolution and LSB Step Size	(Notes 10, 12)		10		Bits
				1.95		mA
II-RB-ACC	Computed Input Current, Readback Accuracy, Neglecting ISVIN	MFR_READ_IIN_n , Channels 0 and 1, $0 \leq \text{IOUT}_n \leq 9\text{A}$, Forced-Continuous Mode, $\text{MFR_PWM_MODE}_n[1:0] = 10_b$, $\text{MFR_IIN_OFFSET}_n = 0\text{mA}$	●	Within 140mA of Reading		
$t_{\text{CONVERT-IO-RB}}$	Output Current Readback Update Rate	MFR_ADC_CONTROL=0x00 (Notes 9, 15)		-100		ms
		MFR_ADC_CONTROL=0x0D (Notes 9, 15)		27		ms
		MFR_ADC_CONTROL=0x06 or 0x0A (Notes 9, 15)		8		ms
$t_{\text{CONVERT-II-RB}}$	Computed Input Current, Readback Update Rate	$\text{MFR_ADC_CONTROL} = 0x00$ (Notes 9, 15)		-100		ms
$N_{\text{DUTY-RB}}$	Resolution, Duty Cycle Readback	(Notes 10, 15)		10		Bits
$D_{\text{RB-ACC}}$	Duty Cycle TUE	READ_DUTY_CYCLE_n , 16.3% Duty Cycle (Note 15)			± 3	%
$t_{\text{CONVERT-DUTY-RB}}$	Duty Cycle Readback Update Rate	$\text{MFR_ADC_CONTROL} = 0x00$ (Notes 9, 15)		-100		ms
Temperature Readback for Channel 0, Channel 1, and Controller (Respectively: $\text{READ_TEMPERATURE}_{10}$, $\text{READ_TEMPERATURE}_{11}$, and $\text{READ_TEMPERATURE}_2$)						
$T_{\text{RES-RB}}$	Temperature Readback Resolution	Channel 0, Channel 1, and Controller (Note 15)		0.0625		$^\circ\text{C}$
$T_{\text{RB-CH-ACC(72mV)}}$	Channel Temperature TUE, Switching Action Off	Channels 0 and 1, PWM Inactive, $\text{RUN}_n = 0\text{V}$, $\Delta V_{\text{TSM}} = 72\text{mV}$	●	Within $\pm 3^\circ\text{C}$ of Reading		

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SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$T_{RB-CH-ACC(ON)}$	Channel Temperature TUE, Switching Action On	READ_TEMPERATURE_1 _n , Channels 0 and 1, PWM Active, $RUN_n = 5\text{V}$ (Note 12)	Within $\pm 3^\circ\text{C}$ of Reading			
$T_{RB-CTRL-ACC(ON)}$	Control IC Die Temperature TUE, Switching Action On	READ_TEMPERATURE_2, PWM Active, $RUN_0 = RUN_1 = 5\text{V}$ (Note 12)	Within $\pm 1^\circ\text{C}$ of Reading			
$t_{\text{CONVERT-TEMP-RB}}$	Temperature Readback Update Rate	MFR_ADC_CONTROL=0x00 (Notes 9, 15) MFR_ADC_CONTROL=0x06 or 0x0A (Notes 9, 15)		90 100 8		ms ms
INTV_{CC} Regulator						
V_{INTVCC}	Internal V_{CC} Voltage No Load	$6\text{V} \leq V_{IN} \leq 17\text{V}$	4.8	5	5.2	V
$\frac{\Delta V_{INTVCC(LOAD)}}{V_{INTVCC}}$	INTV _{CC} Load Regulation	$0\text{mA} \leq I_{INTVCC} \leq 50\text{mA}$		0.5	± 2	%
V_{DD33} Regulator						
V_{VDD33}	Internal V_{DD33} Voltage		3.2	3.3	3.4	V
$I_{LIM(VDD33)}$	V_{DD33} Current Limit	V_{DD33} Electrically Short-Circuited to GND		70		mA
V_{VDD33_OV}	V_{DD33} Overvoltage Threshold	(Note 15)		3.5		V
V_{VDD33_UV}	V_{DD33} Undervoltage Threshold	(Note 15)		3.1		V
V_{DD25} Regulator						
V_{VDD25}	Internal V_{DD25} Voltage			2.5		V
$I_{LIM(VDD25)}$	V_{DD25} Current Limit	V_{DD25} Electrically Short-Circuited to GND		50		mA
Oscillator and Phase-Locked Loop (PLL)						
f_{OSC}	Oscillator Frequency Accuracy	FREQUENCY_SWITCH = 500kHz (0xFBE8) $250\text{kHz} \leq \text{FREQUENCY_SWITCH} \leq 1\text{MHz}$ (Note 15)	●		± 7.5 ± 7.5	% %
f_{SYNC}	PLL SYNC Capture Range	(Note 16)	●	225	1100	kHz
$V_{\text{TH,SYNC}}$	SYNC Input Threshold	V_{SYNC} Rising (Note 15) V_{SYNC} Falling (Note 15)		1.5 1		V V
$V_{\text{OL,SYNC}}$	SYNC Low Output Voltage	$I_{\text{SYNC}} = 3\text{mA}$	●	0.3	0.4	V
I_{SYNC}	SYNC Leakage Current in Frequency Slave Mode	$0\text{V} \leq V_{\text{SYNC}} \leq 3.6\text{V}$ MFR_CONFIG_ALL[4]=1 _b	●		± 5	μA
$\theta_{\text{SYNC-}\theta 0}$	SYNC-to-Channel 0 Phase Relationship, Lag from Falling Edge of Sync to Rising Edge of Top MOSFET (MT0) Gate	(Note 15) MFR_PWM_CONFIG[2:0] = 000 _b , 01X _b MFR_PWM_CONFIG[2:0] = 101 _b MFR_PWM_CONFIG[2:0] = 001 _b MFR_PWM_CONFIG[2:0] = 1X0 _b		0 60 90 120		Deg Deg Deg Deg
$\theta_{\text{SYNC-}\theta 1}$	SYNC-to-Channel 1 Phase Relationship, Lag from Falling Edge of Sync to Rising Edge of Top MOSFET (MT1) Gate	(Note 15) MFR_PWM_CONFIG[2:0] = 011 _b MFR_PWM_CONFIG[2:0] = 000 _b MFR_PWM_CONFIG[2:0] = 010 _b , 10X _b MFR_PWM_CONFIG[2:0] = 001 _b MFR_PWM_CONFIG[2:0] = 110 _b		120 180 240 270 300		Deg Deg Deg Deg Deg

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SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
EEPROM Characteristics						
Endurance	(Note 13)	$0^\circ\text{C} \leq T_J \leq 85^\circ\text{C}$ During EEPROM Write Operations (Note 3)	●	10,000		Cycles
Retention	(Note 13)	$T_J < T_{J(\text{MAX})}$, with Most Recent EEPROM Write Operation Having Occurred at $0^\circ\text{C} \leq T_J \leq 85^\circ\text{C}$ (Note 3)	●	10		Years
Mass_Write	Mass Write Operation Time	Execution of STORE_USER_ALL Command, $0^\circ\text{C} \leq T_J \leq 85^\circ\text{C}$ (ATE-Tested at $T_J = 25^\circ\text{C}$) (Notes 3, 13)		440	4100	ms
Digital I/Os						
V_{IH}	Input High Threshold Voltage	SCL, SDA, RUN_n , \overline{GPIO}_n (Note 15) SHARE_CLK, WP (Note 15)		2.0 1.8		V V
V_{IL}	Input Low Threshold Voltage	SCL, SDA, RUN_n , \overline{GPIO}_n (Note 15) SHARE_CLK, WP (Note 15)			0.6	V V
V_{HYST}	Input Hysteresis	SCL, SDA (Note 15)		80		mV
V_{OL}	Output Low Voltage	SCL, SDA, ALERT, RUN_n , \overline{GPIO}_n , SHARE_CLK: $I_{SINK} = 3\text{mA}$	●	0.3	0.4	V
I_{OL}	Input Leakage Current	SDA, SCL, ALERT, RUN_n : $0\text{V} \leq V_{PIN} \leq 5.5\text{V}$ \overline{GPIO}_n and SHARE_CLK: $0\text{V} \leq V_{PIN} \leq 3.6\text{V}$	● ●		± 5 ± 2	μA μA
t_{FILTER}	Input Digital Filtering	RUN_n (Note 15) \overline{GPIO}_n (Note 15)		10 3		μs μs
C_{PIN}	Input Capacitance	SCL, SDA, RUN_n , \overline{GPIO}_n , SHARE_CLK, WP (Note 15)			10	pF
PMBus Interface Timing Characteristics						
f_{SMB}	Serial Bus Operating Frequency	(Note 15)		10	400	kHz
t_{BUF}	Bus Free Time Between Stop and Start	(Note 15)		1.3		μs
$t_{HD,STA}$	Hold Time After Repeated Start Condition	Time Period After Which First Clock Is Generated (Note 15)		0.6		μs
$t_{SU,STA}$	Repeated Start Condition Setup Time	(Note 15)		0.6		μs
$t_{SU,STO}$	Stop Condition Setup Time	(Note 15)		0.6		μs
$t_{HD,DAT}$	Data Hold Time	Receiving Data (Note 15) Transmitting Data (Note 15)		0 0.3	0.9	μs μs
$t_{SU,DAT}$	Data Setup Time	Receiving Data (Note 15)		0.1		μs
$t_{TIMEOUT_SMB}$	Stuck PMBus Timer Timeout	Measured from the Last PMBus Start Event: Block Reads, MFR_CONFIG_ALL[3]=0 _b (Note 15) Non-Block Reads, MFR_CONFIG_ALL[3]=0 _b (Note 15) MFR_CONFIG_ALL[3]=1 _b (Note 15)		150 32 250		ms ms ms
t_{LOW}	Serial Clock Low Period	(Note 15)		1.3	10000	μs
t_{HIGH}	Serial Clock High Period	(Note 15)		0.6		μs

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SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN}	Input DC Voltage	Test Circuit 1	● 5.75		16	V
		Test Circuit 2; $V_{IN_OFF} < V_{IN_ON} = 4.25\text{V}$	● 4.5		5.75	V
V_{OUTn}	Range of Output Voltage Regulation	V_{OUT0} Differentially Sensed on V_{OSNS0+}/V_{OSNS0-} Pin-Pair;	● 0.5		1.8	V
		V_{OUT1} Differentially Sensed on V_{OSNS1+}/V_{OSNS1-} Pin-Pair; Commanded by Serial Bus or with Resistors Present at Start-Up on $V_{OUTnCFG}$ and/or $V_{TRIMnCFG}$	● 0.5		1.8	V
$V_{OUTn(DC)}$	Output Voltage, Total Variation with Line and Load	Digital Servo Engaged ($\text{MFR_PWM_MODE}_n[6] = 1_b$)	● 0.995	1.000	1.005	V
		Digital Servo Disengaged ($\text{MFR_PWM_MODE}_n[6] = 0_b$) V_{OUTn} Commanded to 1.000V, V_{OUTn} Low Range ($\text{MFR_PWM_MODE}_n[1] = 1_b$) (Note 5)	● 0.985	1.000	1.015	V

Input Specifications

$I_{INRUSH(VIN)}$	Input Inrush Current at Start-Up	Test Circuit 1, $V_{OUTn} = 1\text{V}$, $V_{IN} = 12\text{V}$; No Load Besides Capacitors; $\text{TON_RISE}_n = 3\text{ms}$		400		mA
$I_{Q(SVIN)}$	Input Supply Bias Current	Forced Continuous Mode, $\text{MFR_PWM_MODE}_n[0] = 1_b$ $\text{RUN}_n = 5\text{V}$, $\text{RUN}_{1-n} = 0\text{V}$ Shutdown, $\text{RUN}_0 = \text{RUN}_1 = 0\text{V}$		40		mA
$I_{S(VINn,PSM)}$	Input Supply Current in Pulse-Skipping Mode Operation	Pulse-Skipping Mode, $\text{MFR_PWM_MODE}_n[0] = 0_b$, $I_{OUTn} = 100\text{mA}$		20		mA
$I_{S(VINn,FCM)}$	Input Supply Current in Forced-Continuous Mode Operation	Forced Continuous Mode, $\text{MFR_PWM_MODE}_n[0] = 1_b$ $I_{OUTn} = 100\text{mA}$ $I_{OUTn} = 18\text{A}$		35	1.9	mA A
$I_{S(VINn,SHUTDOWN)}$	Input Supply Current in Shutdown	Shutdown, $\text{RUN}_n = 0\text{V}$		50		μA

Output Specifications

I_{OUTn}	Output Continuous Current Range	(Note 6)		0	18	A	
$\frac{\Delta V_{OUTn(LINE)}}{V_{OUTn}}$	Line Regulation Accuracy	Digital Servo Engaged ($\text{MFR_PWM_MODE}_n[6] = 1_b$)	●	0.03		%/V	
		Digital Servo Disengaged ($\text{MFR_PWM_MODE}_n[6] = 0_b$) S_{VIN} and V_{INn} Electrically Shorted Together and INTV_{CC} Open Circuit; $I_{OUTn} = 0\text{A}$, $5.75\text{V} \leq V_{IN} \leq 16\text{V}$, V_{OUT} Low Range ($\text{MFR_PWM_MODE}_n[1] = 1_b$), $\text{FREQUENCY_SWITCH} = 350\text{kHz}$ (Note 5)	●	0.03	± 0.2	%/V	
$\frac{\Delta V_{OUTn(LOAD)}}{V_{OUTn}}$	Load Regulation Accuracy	Digital Servo Engaged ($\text{MFR_PWM_MODE}_n[6] = 1_b$)	●	0.03		%	
		Digital Servo Disengaged ($\text{MFR_PWM_MODE}_n[6] = 0_b$) $0\text{A} \leq I_{OUTn} \leq 18\text{A}$, V_{OUT} Low Range, ($\text{MFR_PWM_MODE}_n[1] = 1_b$) (Note 5)	●	0.2	0.5	%	
$V_{OUTn(AC)}$	Output Voltage Ripple			10		mV _{p-p}	
f_S (Each Channel)	V_{OUTn} Ripple Frequency	FREQUENCY_SWITCH Set to 500kHz (0xFBE8)	●	462.5	500	537.5	kHz
$\Delta V_{OUTn(START)}$	Turn-On Overshoot	$\text{TON_RISE}_n = 3\text{ms}$ (Note 12)			8		mV
t_{START}	Turn-On Start-Up Time	Time from V_{IN} Toggling from 0V to 12V to Rising Edge of GPIO_n . $\text{TON_DELAY}_n = 0\text{ms}$, $\text{TON_RISE}_n = 3\text{ms}$, $\text{MFR_GPIO_PROPAGATE}_n = 0x0100$, $\text{MFR_GPIO_RESPONSE}_n = 0x0000$	●		60	70	ms

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SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$t_{\text{DELAY}(0\text{ms})}$	Turn-On Delay Time	Time from First Rising Edge of RUN_n to Rising Edge of $\overline{\text{GPIO}}_n$. ● $\text{TON_DELAY}_n = 0\text{ms}$, $\text{TON_RISE}_n = 3\text{ms}$, $\text{MFR_GPIO_PROPAGATE}_n = 0x0100$, $\text{MFR_GPIO_RESPONSE}_n = 0x0000$. V_{IN} Having Been Established for at Least 70ms	2.75	3.1	3.5	ms
$\Delta V_{\text{OUTn}}(\text{LS})$	Peak Output Voltage Deviation for Dynamic Load Step	Load: 0A to 9A and 9A to 0A at $9\text{A}/\mu\text{s}$, Figure 56 Circuit, $V_{\text{OUTn}} = 1\text{V}$, $V_{IN} = 12\text{V}$ (Note 12)		50		mV
t_{SETTLE}	Settling Time for Dynamic Load Step	Load: 0A to 9A and 9A to 0A at $9\text{A}/\mu\text{s}$, Figure 56 Circuit, $V_{\text{OUTn}} = 1\text{V}$, $V_{IN} = 12\text{V}$ (Note 12)		35		μs
$I_{\text{OUTn}}(\text{OCL_PK})$	Output Current Limit, Peak	Cycle-by-Cycle Inductor Peak Current Limit Inception		25		A
$I_{\text{OUTn}}(\text{OCL_AVG})$	Output Current Limit, Time Averaged	Time-Averaged Output Inductor Current Limit Inception Threshold, Commanded by $I_{\text{OUT_OC_FAULT_LIMIT}}_n$ (Note 12)		20A; See $I_{\text{O-RB-ACC}}$ Specification (Output Current Readback Accuracy)		
Control Section						
$V_{\text{FBM}0}$	Channel 0 Feedback Input Common Mode Range	$V_{\text{OSNS}0^-}$ Valid Input Range (Referred to SGND) $V_{\text{OSNS}0^+}$ Valid Input Range (Referred to SGND)	●	-0.1	0.3	V
$V_{\text{FBM}1}$	Channel 1 Feedback Input Common Mode Range	SGND Valid Input Range (Referred to GND) $V_{\text{OSNS}1}$ Valid Input Range (Referred to SGND)	●	-0.3	0.3	V
$V_{\text{OUT-RNG}1}$	Full-Scale Command Voltage, Range 1	(Notes 7, 15) V_{OUTn} Commanded to 2.750V , $\text{MFR_PWM_MODE}_n[1] = 1_b$ Resolution LSB Step Size		2.711	2.788	V
$R_{\text{VSENSE}0^+}$	$V_{\text{OSNS}0^+}$ Impedance to SGND	$0.05\text{V} \leq V_{\text{OSNS}0^+} - V_{\text{SGND}} \leq 1.8\text{V}$		41		$\text{k}\Omega$
$R_{\text{VSENSE}1}$	$V_{\text{OSNS}1}$ Impedance to SGND	$0.05\text{V} \leq V_{\text{OSNS}1} - V_{\text{SGND}} \leq 1.8\text{V}$		37		$\text{k}\Omega$
$t_{\text{ON(MIN)}}$	Minimum On-Time	(Note 8)		90		ns
Analog OV/UV (Overvoltage/Undervoltage) Output Voltage Supervisor Comparators ($V_{\text{OUT_OV/UV_FAULT_LIMIT}}$ and $V_{\text{OUT_OV/UV_WARN_LIMIT}}$ Monitors)						
$N_{\text{OV/UV_COMP}}$	Resolution, Output Voltage Supervisors	(Note 15)		8		Bits
$V_{\text{OV-RNG}}$	Output OV Comparator Threshold Detection Range	(Note 15) High Range Scale, $\text{MFR_PWM_MODE}_n[1] = 0_b$ Low Range Scale, $\text{MFR_PWM_MODE}_n[1] = 1_b$		1	5.6	V
$V_{\text{OU-STP}}$	Output OV and UV Comparator Threshold Programming LSB Step Size	(Note 15) High Range Scale, $\text{MFR_PWM_MODE}_n[1] = 0_b$ Low Range Scale, $\text{MFR_PWM_MODE}_n[1] = 1_b$		22	11	mV

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SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OV-ACC}	Output OV Comparator Threshold Accuracy	(See Note 14) $1\text{V} \leq V_{VOSNS0^+} - V_{VOSNS0^-} \leq 1.8\text{V}$, MFR_PWM_MODE ₀ [1] = 1 _b ● $0.5\text{V} \leq V_{VOSNS0^+} - V_{VOSNS0^-} < 1\text{V}$, MFR_PWM_MODE ₀ [1] = 1 _b ● $1.5\text{V} \leq V_{VSENSE1} - V_{SGND} \leq 1.8\text{V}$, MFR_PWM_MODE ₁ [1] = 1 _b ● $0.5\text{V} \leq V_{VSENSE1} - V_{SGND} < 1.5\text{V}$, MFR_PWM_MODE ₁ [1] = 1 _b ●			±2 ±20	% mV
V_{UV-RNG}	Output UV Comparator Threshold Detection Range	(Note 15) High Range Scale, MFR_PWM_MODE _n [1] = 0 _b Low Range Scale, MFR_PWM_MODE _n [1] = 1 _b	1 0.5		5.4 2.7	V V
V_{UV-ACC}	Output UV Comparator Threshold Accuracy	(See Note 14) $1\text{V} \leq V_{VSENSE0^+} - V_{VSENSE0^-} \leq 1.8\text{V}$, MFR_PWM_MODE ₀ [1] = 1 _b ● $0.5\text{V} \leq V_{VSENSE0^+} - V_{VSENSE0^-} < 1\text{V}$, MFR_PWM_MODE ₀ [1] = 1 _b ● $1.5\text{V} \leq V_{VOSNS1} - V_{SGND} \leq 1.8\text{V}$, MFR_PWM_MODE ₁ [1] = 1 _b ● $0.5\text{V} \leq V_{VOSNS1} - V_{SGND} < 1.5\text{V}$, MFR_PWM_MODE ₁ [1] = 1 _b ●			±2 ±20	% mV
$t_{PROP-OV}$	Output OV Comparator Response Times	Overdrive to 10% Above Programmed Threshold			35	μs
$t_{PROP-UV}$	Output UV Comparator Response Times	Underdrive to 10% Below Programmed Threshold			50	μs
Analog OV/UV SV_{IN} Input Voltage Supervisor Comparators (Threshold Detectors for V_{IN_ON} and V_{IN_OFF})						
$N_{SVIN-OV/UV-COMP}$	SV_{IN} OV/UV Comparator Threshold-Programming Resolution	(Note 15)		8		Bits
$SV_{IN-OU-RANGE}$	SV_{IN} OV/UV Comparator Threshold-Programming Range		●	4.5	18	V
$SV_{IN-OU-STP}$	SV_{IN} OV/UV Comparator Threshold-Programming LSB Step Size	(Note 15)		82		mV
$SV_{IN-OU-ACC}$	SV_{IN} OV/UV Comparator Threshold Accuracy	$9\text{V} < SV_{IN} \leq 16\text{V}$ $4.5\text{V} \leq SV_{IN} \leq 9\text{V}$	● ●		±2.5 ±225	% mV
$t_{PROP-SVIN-HIGH-VIN}$	SV_{IN} OV/UV Comparator Response Time, High V_{IN} Operating Configuration	Test Circuit 1, and: $V_{IN_ON} = 9\text{V}$; SV_{IN} Driven from 8.775V to 9.225V $V_{IN_OFF} = 9\text{V}$; SV_{IN} Driven from 9.225V to 8.775V	● ●		35 35	μs μs
$t_{PROP-SVIN-LOW-VIN}$	SV_{IN} OV/UV Comparator Response Time, Low V_{IN} Operating Configuration	Test Circuit 2, and: $V_{IN_ON} = 4.5\text{V}$; SV_{IN} Driven from 4.225V to 4.725V $V_{IN_OFF} = 4.5\text{V}$; SV_{IN} Driven from 4.725V to 4.225V	● ●		35 35	μs μs
Channels 0 and 1 Output Voltage Readback (READ_VOUT_n)						
N_{VO-RB}	Output Voltage Readback Resolution and LSB Step Size	(Note 15)		16 244		Bits μV
V_{O-FS}	Output Voltage Full-Scale Digitizable Range	$V_{RUN,n} = 0\text{V}$ (Notes 7, 15)		8		V
$V_{O-RB-ACC}$	Output Voltage Readback Accuracy	Channel 0: $1\text{V} \leq V_{VOSNS0^+} - V_{VOSNS0^-} \leq 1.8\text{V}$ Channel 0: $0.6\text{V} \leq V_{VOSNS0^+} - V_{VOSNS0^-} < 1\text{V}$ Channel 1: $1\text{V} \leq V_{VOSNS1} - V_{SGND} \leq 1.8\text{V}$ Channel 1: $0.6\text{V} \leq V_{VOSNS1} - V_{SGND} < 1\text{V}$	● ● ● ●		Within ±0.5% of Reading Within ±5mV of Reading Within ±0.5% of Reading Within ±5mV of Reading	
$t_{CONVERT-VO-RB}$	Output Voltage Readback Update Rate	MFR_ADC_CONTROL = 0x00 (Notes 9, 15) MFR_ADC_CONTROL = 0x00 (Notes 9, 15) MFR_ADC_CONTROL = 0x05 or 0x09 (Notes 9, 15)			100 27 8	ms ms ms

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SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage (SV_{IN}) Readback (READ_VIN)						
$N_{SVIN-RB}$	Input Voltage Readback Resolution and LSB Step Size	(Notes 10, 15)		10 15.625		Bits mV
$SV_{IN-F/S}$	Input Voltage Full-Scale Digitizable Range	(Notes 11, 15)		38.91		V
$SV_{IN-RB-ACC}$	Input Voltage Readback Accuracy	READ_VIN , $4.5\text{V} \leq SV_{IN} \leq 16\text{V}$	●	Within $\pm 2\%$ of Reading		90
$t_{\text{CONVERT-SVIN-RB}}$	Input Voltage Readback Update Rate	$\text{MFR_ADC_CONTROL} = 0 \times 00$ (Notes 9, 15) $\text{MFR_ADC_CONTROL} = 0 \times 01$ (Notes 9, 15)		100 8		ms ms
Channels 0 and 1 Output Current (READ_IOUT_n), Duty Cycle (READ_DUTY_CYCLE_n), and Computed Input Current (MFR_READ_IIN_n) Readback						
N_{IO-RB}	Output Current Readback Resolution and LSB Step Size	(Notes 10, 12)		10 15.6		Bits mA
$I_{O-F/S}$, $I_{I-F/S}$	Output Current Full-Scale Digitizable Range and Input Current Range of Calculation	(Note 12)		± 40		A
$I_{O-RB-ACC}$	Output Current, Readback Accuracy	READ_IOUT_n , Channels 0 and 1, $0 \leq I_{OUTn} \leq 10\text{A}$, Forced-Continuous Mode, $\text{MFR_PWM_MODE}_n[1:0] = 10_b$	●	Within 250mA of Reading		
$I_{O-RB(18A)}$	Full Load Output Current Readback	$I_{OUTn} = 18\text{A}$ (Note 12). See Histograms in Typical Performance Characteristics		18		A
N_{II-RB}	Computed Input Current, Readback Resolution and LSB Step Size	(Notes 10, 12)		10 1.95		Bits mA
$I_{I-RB-ACC}$	Computed Input Current, Readback Accuracy, Neglecting I_{SVIN}	MFR_READ_IIN_n , Channels 0 and 1, $0 \leq I_{OUTn} \leq 10\text{A}$, Forced-Continuous Mode, $\text{MFR_PWM_MODE}_n[1:0] = 10_b$, $\text{MFR_IIN_OFFSET}_n = 0\text{mA}$	●	Within 150mA of Reading		90
$t_{\text{CONVERT-IO-RB}}$	Output Current Readback Update Rate	$\text{MFR_ADC_CONTROL} = 0 \times 00$ (Notes 9, 15) $\text{MFR_ADC_CONTROL} = 0 \times 00$ (Notes 9, 15) $\text{MFR_ADC_CONTROL} = 0 \times 05$ or 0×09 (Notes 9, 15)		100 27 8		ms ms ms
$t_{\text{CONVERT-II-RB}}$	Computed Input Current, Readback Update Rate	(Notes 9, 15) $\text{MFR_ADC_CONTROL} = 0 \times 00$		100		ms
$N_{DUTY-RB}$	Resolution, Duty Cycle Readback	(Notes 10, 15)		10		Bits
D_{RB-ACC}	Duty Cycle TUE	READ_DUTY_CYCLE_n , 16.3% Duty Cycle (Note 15)			± 3	%
$t_{\text{CONVERT-DUTY-RB}}$	Duty Cycle Readback Update Rate	(Notes 9, 15) $\text{MFR_ADC_CONTROL} = 0 \times 00$		100		ms
Temperature Readback for Channel 0, Channel 1, and Controller (Respectively: $\text{READ_TEMPERATURE}_{10}$, $\text{READ_TEMPERATURE}_{11}$, and $\text{READ_TEMPERATURE}_2$)						
T_{RES-RB}	Temperature Readback Resolution	Channel 0, Channel 1, and Controller (Note 15)		0.0625		$^\circ\text{C}$
$T_{RB-CH-ACC(72\text{mV})}$	Channel Temperature TUE, Switching Action Off	Channels 0 and 1, PWM Inactive, $\text{RUN}_n = 0\text{V}$, $\Delta V_{TSNSna} = 72\text{mV}$	●	Within $\pm 3^\circ\text{C}$ of Reading		
$T_{RB-CH-ACC(0\text{N})}$	Channel Temperature TUE, Switching Action On	$\text{READ_TEMPERATURE}_{1n}$, Channels 0 and 1, PWM Active, $\text{RUN}_n = 5\text{V}$ (Note 12)		Within $\pm 3^\circ\text{C}$ of Reading		

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SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$T_{RB-CTRL-ACC(ON)}$	Control IC Die Temperature TUE, Switching Action On	READ_TEMPERATURE_2, PWM Active, $RUN_0 = RUN_1 = 5\text{V}$ (Note 12)	Within $\pm 1^\circ\text{C}$ of Reading			
$t_{CONVERT-TEMP-RB}$	Temperature Readback Update Rate	MFR_ADC_CONTROL = 0x00 (Notes 9, 15) MFR_ADC_CONTROL = 0x06 or 0x0A (Notes 9, 15)		100 8		ms ms
INTV_{CC} Regulator						
V_{INTVCC}	Internal V_{CC} Voltage No Load	$6\text{V} \leq V_{IN} \leq 16\text{V}$	4.8	5	5.2	V
$\frac{\Delta V_{INTVCC(LOAD)}}{V_{INTVCC}}$	INTV _{CC} Load Regulation	$0\text{mA} \leq I_{INTVCC} \leq 50\text{mA}$		0.5	± 2	%
V_{DD33} Regulator						
V_{DD33}	Internal V_{DD33} Voltage		3.2	3.3	3.4	V
$I_{LIM(VDD33)}$	V_{DD33} Current Limit	V_{DD33} Electrically Short-Circuited to GND		70		mA
V_{DD33_OV}	V_{DD33} Overvoltage Threshold	(Note 15)		3.5		V
V_{DD33_UV}	V_{DD33} Undervoltage Threshold	(Note 15)		3.1		V
V_{DD25} Regulator						
V_{DD25}	Internal V_{DD25} Voltage			2.5		V
$I_{LIM(VDD25)}$	V_{DD25} Current Limit	V_{DD25} Electrically Short-Circuited to GND		50		mA
Oscillator and Phase-Locked Loop (PLL)						
f_{OSC}	Oscillator Frequency Accuracy	FREQUENCY_SWITCH = 500kHz (0xFBE8) $250\text{kHz} \leq \text{FREQUENCY_SWITCH} \leq 750\text{kHz}$ (Note 15)	●		± 7.5 ± 7.5	% %
f_{SYNC}	PLL SYNC Capture Range	FREQUENCY_SWITCH Set to Frequency Slave Mode (0x0000); SYNC Driven by External Clock; $1.8V_{OUT}$	●	225	800	kHz
$V_{TH,SYNC}$	SYNC Input Threshold	V_{SYNC} Rising (Note 15) V_{SYNC} Falling (Note 15)		1.5 1		V V
$V_{OL,SYNC}$	SYNC Low Output Voltage	$I_{SYNC} = 3\text{mA}$	●	0.3	0.4	V
I_{SYNC}	SYNC Leakage Current in Frequency Slave Mode	$0\text{V} \leq V_{SYNC} \leq 3.6\text{V}$ MFR_CONFIG_ALL[4]=1 _b	●		± 5	μA
$\theta_{SYNC-00}$	SYNC-to-Channel 0 Phase Relationship, Lag from Falling Edge of Sync to Rising Edge of Top MOSFET (MT0) Gate	(Note 15) MFR_PWM_CONFIG[2:0] = 000 _b , 01X _b MFR_PWM_CONFIG[2:0] = 101 _b MFR_PWM_CONFIG[2:0] = 001 _b MFR_PWM_CONFIG[2:0] = 1X0 _b		0 60 90 120		Deg Deg Deg Deg
$\theta_{SYNC-01}$	SYNC-to-Channel 1 Phase Relationship, Lag from Falling Edge of Sync to Rising Edge of Top MOSFET (MT1) Gate	(Note 15) MFR_PWM_CONFIG[2:0] = 011 _b MFR_PWM_CONFIG[2:0] = 000 _b MFR_PWM_CONFIG[2:0] = 010 _b , 10X _b MFR_PWM_CONFIG[2:0] = 001 _b MFR_PWM_CONFIG[2:0] = 110 _b		120 180 240 270 300		Deg Deg Deg Deg Deg

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ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2). Specified as each individual output channel (Note 4). $T_A = 25^\circ\text{C}$, $V_{IN} = 12\text{V}$, $RUN_n = 5\text{V}$, $\text{FREQUENCY_SWITCH} = 500\text{kHz}$ and V_{OUT_n} commanded to 1.000V unless otherwise noted. Configured with factory-default EEPROM settings and per Test Circuit 1, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
EEPROM Characteristics						
Endurance	(Note 13)	$0^\circ\text{C} \leq T_J \leq 85^\circ\text{C}$ During EEPROM Write Operations (Note 3)	●	10,000		Cycles
Retention	(Note 13)	$T_J < T_{J(\text{MAX})}$, with Most Recent EEPROM Write Operation Having Occurred at $0^\circ\text{C} \leq T_J \leq 85^\circ\text{C}$ (Note 3)	●	10		Years
Mass_Write	Mass Write Operation Time	Execution of STORE_USER_ALL Command, $0^\circ\text{C} \leq T_J \leq 85^\circ\text{C}$ (ATE-Tested at $T_J = 25^\circ\text{C}$) (Notes 3, 13)		440	4100	ms
Digital I/Os						
V_{IH}	Input High Threshold Voltage	SCL, SDA, RUN_n , \overline{GPIO}_n (Note 15) SHARE_CLK, WP (Note 15)		2.0 1.8		V
V_{IL}	Input Low Threshold Voltage	SCL, SDA, RUN_n , \overline{GPIO}_n (Note 15) SHARE_CLK, WP (Note 15)			1.4 0.6	V
V_{HYST}	Input Hysteresis	SCL, SDA (Note 15)		80		mV
V_{OL}	Output Low Voltage	SCL, SDA, ALERT, RUN_n , \overline{GPIO}_n , SHARE_CLK: $I_{SINK} = 3\text{mA}$	●	0.3	0.4	V
I_{OL}	Input Leakage Current	SDA, SCL, ALERT, RUN_n : $0\text{V} \leq V_{PIN} \leq 5.5\text{V}$ \overline{GPIO}_n and SHARE_CLK: $0\text{V} \leq V_{PIN} \leq 3.6\text{V}$	●		± 5 ± 2	μA μA
t_{FILTER}	Input Digital Filtering	RUN_n (Note 15) \overline{GPIO}_n (Note 15)		10 3		μs μs
C_{PIN}	Input Capacitance	SCL, SDA, RUN_n , \overline{GPIO}_n , SHARE_CLK, WP (Note 15)			10	pF
PMBus Interface Timing Characteristics						
f_{SMB}	Serial Bus Operating Frequency	(Note 15)		10	400	kHz
t_{BUF}	Bus Free Time Between Stop and Start	(Note 15)		1.3		μs
$t_{HD,STA}$	Hold Time After Repeated Start Condition	Time Period After Which First Clock Is Generated (Note 15)		0.6		μs
$t_{SU,STA}$	Repeated Start Condition Setup Time	(Note 15)		0.6		μs
$t_{SU,STO}$	Stop Condition Setup Time	(Note 15)		0.6		μs
$t_{HD,DAT}$	Data Hold Time	Receiving Data (Note 15) Transmitting Data (Note 15)		0 0.3	0.9	μs μs
$t_{SU,DAT}$	Data Setup Time	Receiving Data (Note 15)		0.1		μs
$t_{TIMEOUT_SMB}$	Stuck PMBus Timer Timeout	Measured from the Last PMBus Start Event: Block Reads MFR_CONFIG_ALL[3] = 0 _b (Note 15) Non-Block Reads MFR_CONFIG_ALL[3] = 0 _b (Note 15) MFR_CONFIG_ALL[3] = 1 _b (Note 15)		150 32 250		ms ms ms
t_{LOW}	Serial Clock Low Period	(Note 15)		1.3	10000	μs
t_{HIGH}	Serial Clock High Period	(Note 15)		0.6		μs

Note 1: Stresses beyond those listing under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating conditions for extended periods may affect device reliability and lifetime.

Note 2: The LTM4677 is tested under pulsed-load conditions such that $T_J = T_A$. The LTM4677E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications

over the -40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4677I is guaranteed to meet specifications over the full -40°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

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For more information www.linear.com/LTM4677

END.