

EiceDRIVER™

High voltage gate driver IC

Evaluation Board

Application Note

EVAL-2EDL23N06PJ

Application Note

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Warnings



The described board is an evaluation board dedicated for laboratory environment only. It operates at high voltages. This board must be operated by qualified, skilled personnel familiar with all applicable safety standards.

1 Introduction

The gate driver evaluation board EVAL-2EDL23N06PJ was developed to show the functionalities and key features of the Infineon COOLMOS™ gate driver 2EDL23N06PJ in resonant zero voltage turn-on half-bridge applications. The board EVAL-2EDL23N06PJ is therefore **not recommended by default** for hard switched operation which leads to hard body diode commutation and hence excessive diode as well as COOLMOS™ losses. Such operation may result to damage of power switches and possibly other circuit components!

The board is available from Infineon in sampling quantities. The properties of this part are described in the datasheet chapter of this document, whereas the remaining paragraphs provide information intended to enable the customer to copy, modify and qualify the design for production, according to their own specific requirements.

The design of the EVAL-2EDL23N06PJ was performed with respect to the environmental conditions described in this document. The design was tested as described in this document, but not qualified regarding manufacturing, lifetime or over the full ambient operating conditions.

The boards provided by Infineon are subjected to functional testing only.

Due to their purpose Evaluation Boards are not subjected to the same procedures regarding Returned Material Analysis (RMA), Process Change Notification (PCN) and Product Discontinuation (PD) as regular products. These Evaluation Boards are used for development support only and should not be used as reference design for volume production.

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2 Design features

2.1 Main features

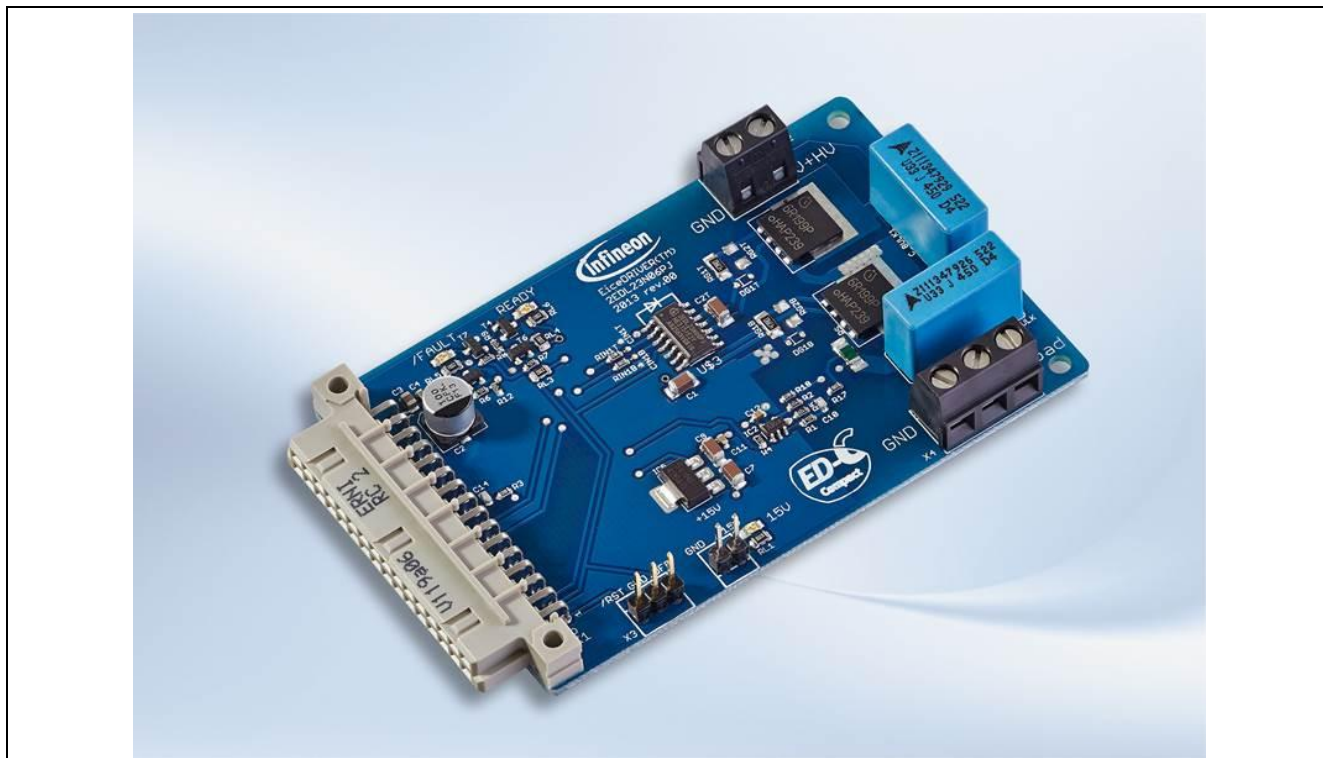


Figure 1 Top view of the EVAL-2EDL23N06PJ

The EVAL-2EDL23N06PJ contains a single Infineon 2EDL23N06PJ half-bridge gate driver and two Infineon COOLMOS™ switches.

The evaluation board provides the following main features

- Short circuit protection by shunt measurement incl. status LED (/FAULT) and latch
- Current measurement with operational amplifier
- Undervoltage lockout
- Bootstrap functionality for high side switch by using an internal ultra-fast bootstrap diode
- Deadtime and interlock function integrated in the EiceDRIVER™.
- Connector for 15V supply, Reset, High voltage supply, external load
- Onboard voltage regulator for 5V supply
- Status LED for 15V supply, /FAULT state
- Split DC link capacitor

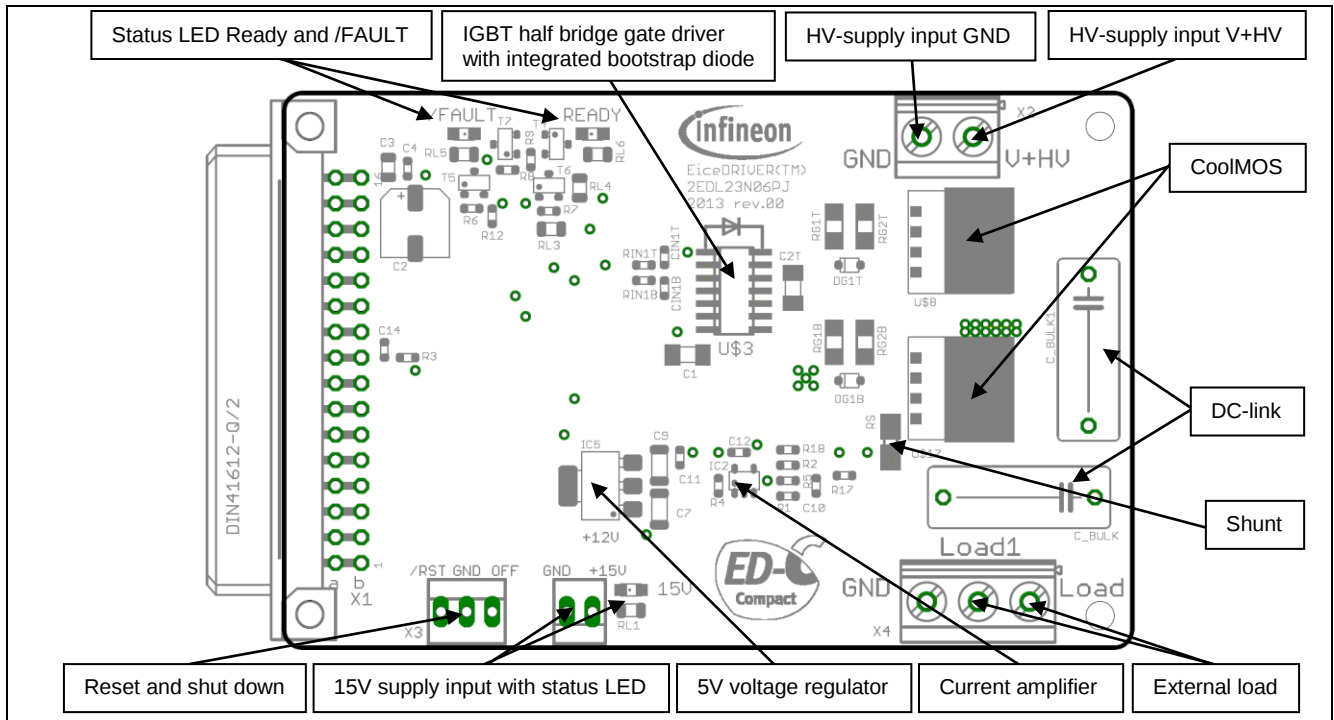


Figure 2 Overview functionalities on top-side

2.2 Board specifications

All values are specified at an ambient temperature of $T_A = 25^\circ\text{C}$

Table 1 Board specifications

Parameter	Description	Typ.	min	max	Unit
V_{DD}	15V voltage supply	15	10	17.5	V
V_{DC}	High voltage supply	300	-	450	V
$I_{Out,pk}$	Single pulse peak output current	-	-	20	A
$I_{Out,rms}$	RMS output current	-	-	4	A
f_p	Switching frequency	40	-	200	kHz

2.3 Pin assignment

Table 2 Pin assignment

Connector name	Pin no.	Pin name	Description
RESET	Left terminal	/RST	same as X1-B1
	Middle terminal	GND	same as X1-A16
	Right terminal	OFF	same as X1-B2

+15V (VDD)	Right terminal	+15V	positive 15V supply
	Left terminal	GND	

X1	A16	GND	reference for 15V supply and input signals
	B1	/RST	input – 0V to reset circuit
	B2	/FLT	output over current; OC, 0..15V
	B7	IN_T	non-inverting input high side COOLMOS™; 0V off; 5V on
	B8	IN_B	non-inverting input low side COOLMOS™; 0V off; 5V on
	B16	+5V	positive 5V supply generated from 15V

*see Figure 22 for connector pin numbering

GND			reference for high voltage supply (internally connected to GND)
V+HV			positive high voltage supply
Load			Output HV half bridge (related to GND_HV) for connecting a test load
Load1			Output DC link center point for connecting a test load for resonant zero-voltage turn-on operation

3 Electrical features

3.1 Supply voltages +5V and +15V

The supply voltage for the driver output (+15V VDD) has to be supplied externally over the dedicated connector. The digital 5V supply voltage is generated internally by an Infineon voltage regulator. The evaluation board does not provide an overvoltage supply monitoring. The user has to ensure therefore that the voltages are in the correct range. The availability of the supply voltage +15V is visible over the green status LED.

The high-side gate driver is supplied via the integrated ultra-fast bootstrap diode of the 2EDL23N06PJ. To ensure that the bootstrap capacitor is charged before the high side COOLMOS™ is switched on, the low side COOLMOS™ has to be switched on for a dedicated time of several milliseconds.

3.2 Undervoltage lockout

The +15V supply VDD is monitored by the 2EDL23N06PJ. In case of an undervoltage the driver output is switched off. The thresholds for the low side as well as for the high side are typically $V_{CCUV+} = 9.1\text{ V}$ (positive going) and $V_{CCUV-} = 8.3\text{ V}$ (negative going). The undervoltage lockout state of the input section is indicated by the /FAULT LED.

3.3 Short circuit detection

The 2EDL23N06PJ provides integrated short circuit detection by measuring the voltage drop over a 20mΩ shunt. The shunt is connected as shown in Figure 3 (left). If the current reaches a value of typ. 22.5A a short circuit is detected, and the gate driver outputs are switched off. This status is reported by the /FAULT LED. The /FAULT event is latched by the flip-flop according to Figure 3 (right) and must be reset by activating the reset contactor.

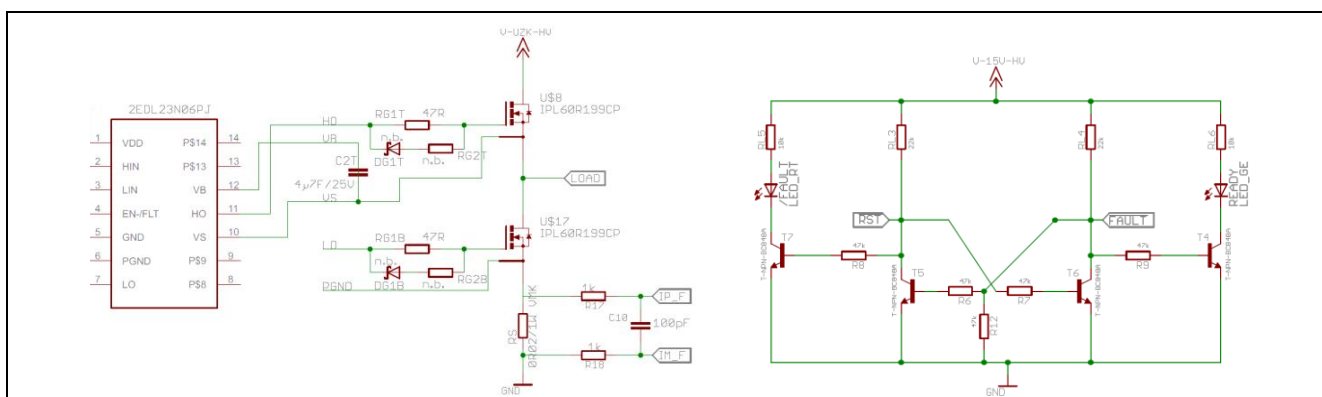


Figure 3 Shunt interface to Opamp and flip-flop latch circuit.

Figure 4 shows the signals of the bottom side driver and COOLMOS™ switch during an overcurrent condition. The delay between over current event and output switch off is about 2.2 μs. The FAULT status is latched by an internal logic and must be reset by switching the RESET Signal to ground

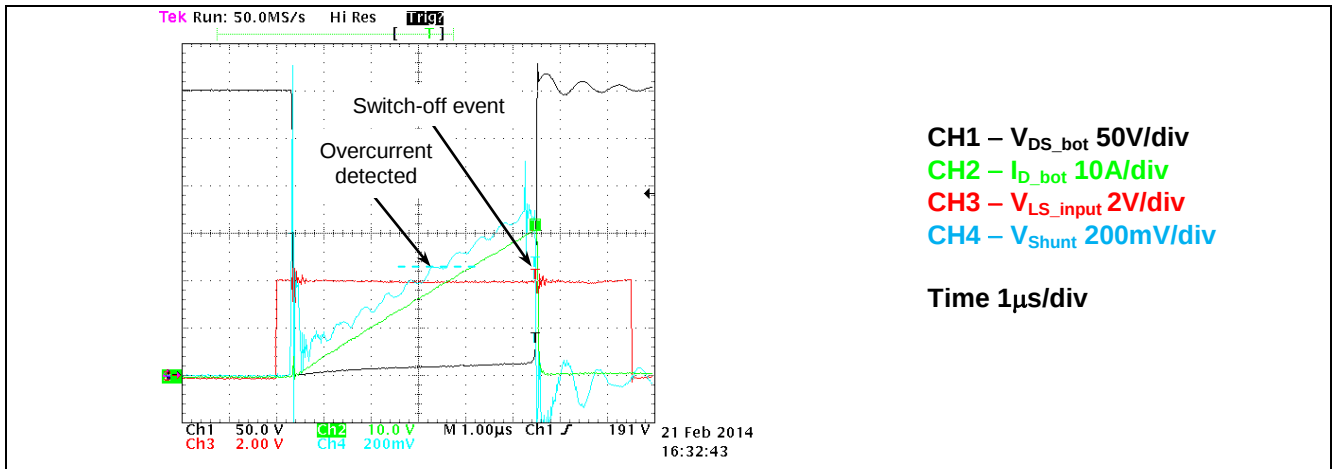


Figure 4 Overcurrent detection signals (current measured by Rogowski coil)

3.4 Current amplifier

The EVAL-2EDL23N06PJ provides an operational amplifier which amplifies the voltage drop over the shunt with a gain of 10. The amplified voltage is available for the user at connector X1 pins A9 and B9. The amplified voltage is calculated with $V = I_{shunt} \times R_{shunt} \times 10$. Due to inherent component tolerances, the amplifier output should be calibrated in case of using it for a critical current control. It should also be noted that the current amplifier output shows the current of the low side COOLMOS™ switch only. This fact should be considered in case if using the current amplifier output in the higher level control system. Example of load current waveforms and current amplifier output is shown in Figure 6.

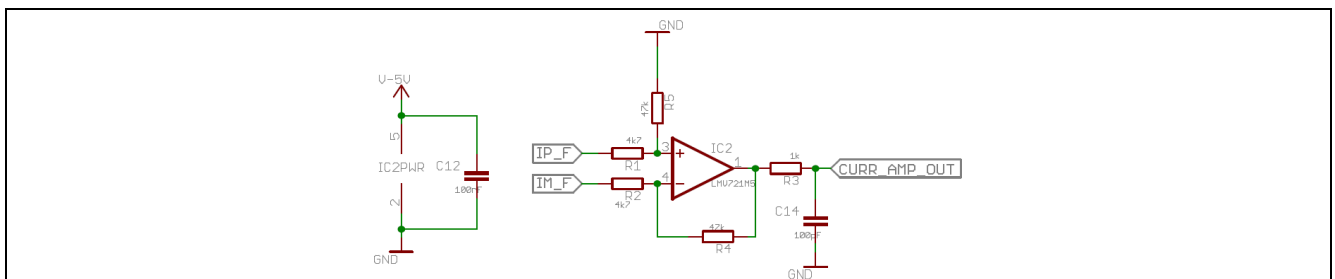


Figure 5 Current amplifier

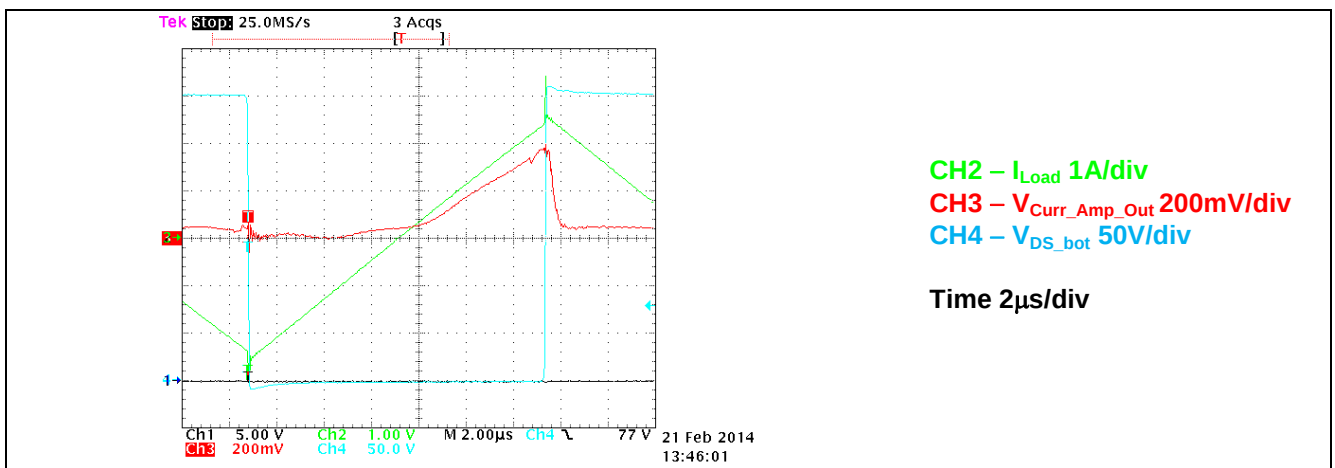


Figure 6 Current amplifier output with collector current (current measured by Rogowski coil)

3.5 Deadtime and interlock function

The IC provides a hardware fixed deadtime of typically 75ns. An additional interlock function prevents the two outputs from being activated simultaneously. If necessary, a higher deadtime can be generated by the input signals LIN and HIN when hardware deadtime does not block shoot-through. The hardware deadtime is a basic item to avoid deep shoot through. The general recommendation for dead time is to be approx. 1 μ s.

3.6 COOLMOS™ turn - on / off

The switching characteristic of the COOLMOS™ is defined by the gate resistors RG1B, RG1T, RG2B and RG2T according to Figure 7. The resistor values are selected in order to avoid parasitic dv/dt-triggered turn-on. There is the possibility to adapt the switching characteristic to specific applications or to different COOLMOS™ devices by changing the values of RG1B and RG1T. The use of RG2B and RG2T together with DG1B and DG1T makes it possible to change the on-switching and off-switching slopes of the COOLMOS™ independent of each other. In case of using the diodes DG1B and DG1T, please make sure to select an appropriate Schottky diode with sufficient pulse current capability.

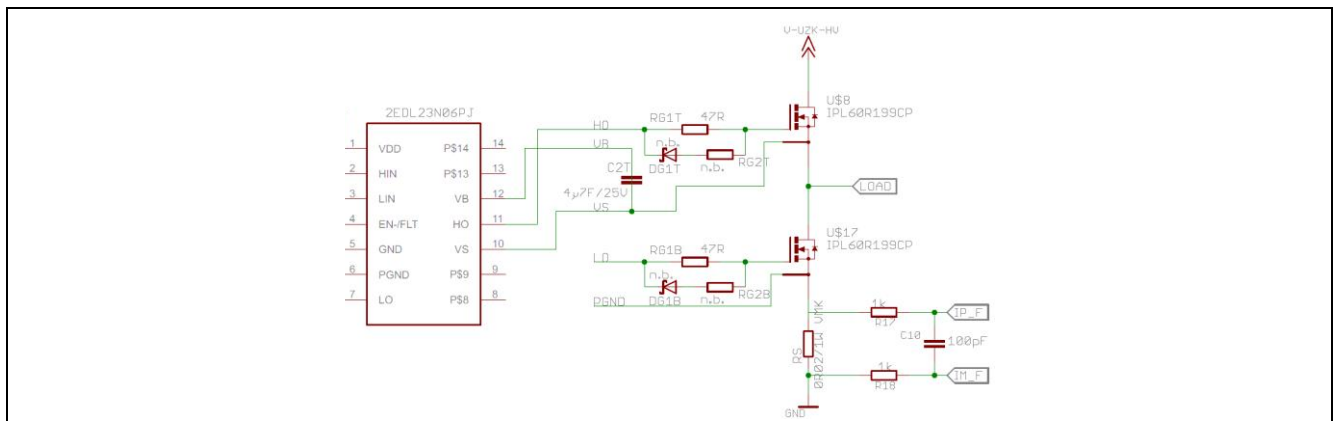


Figure 7 EiceDRIVER™ 2EDL23N06PJ gate circuit

Figure 8 and Figure 9 show typical switching transients for the high side and the low side COOLMOS™ devices.

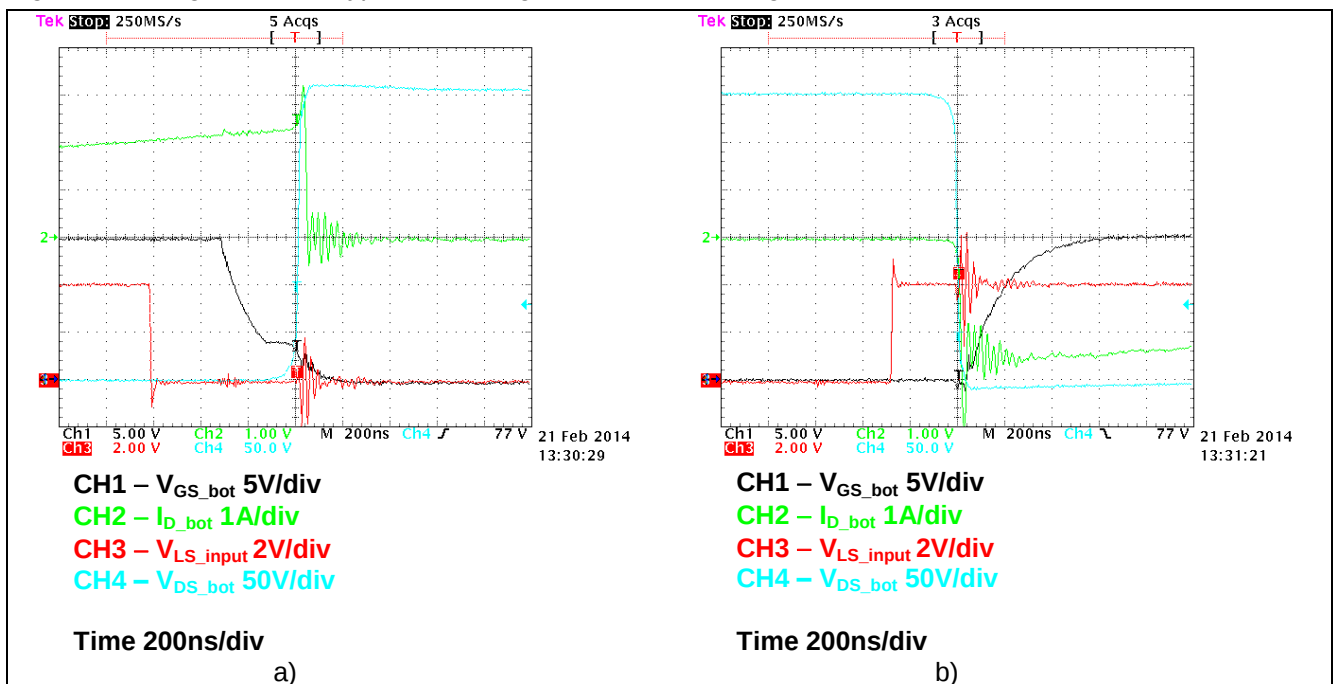
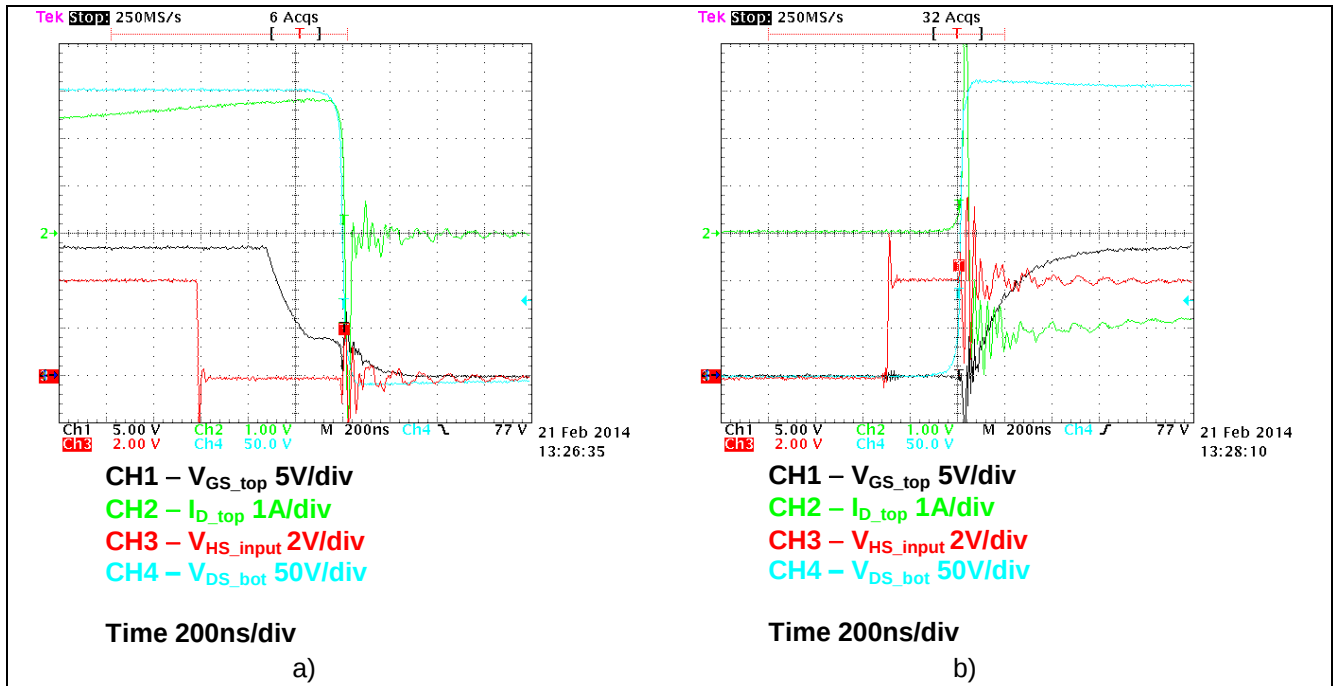


Figure 8 Switching transient of low side COOLMOS™; a) turn-off, b) turn-on; (current measured by Rogowski coil)



3.7 Input PWM-Signals

There is the possibility to use low pass filters inside the PWM input signals to avoid an undesired turn-on of the COOLMOS™ by disturbances. This feature is not used in this evaluation board, but there is the possibility to test it by changing the resistors RIN1T, RIN1B and the capacitors CIN1T, CIN1B. Only the resistors RIN1T and RIN1B are assembled according to Figure 10.

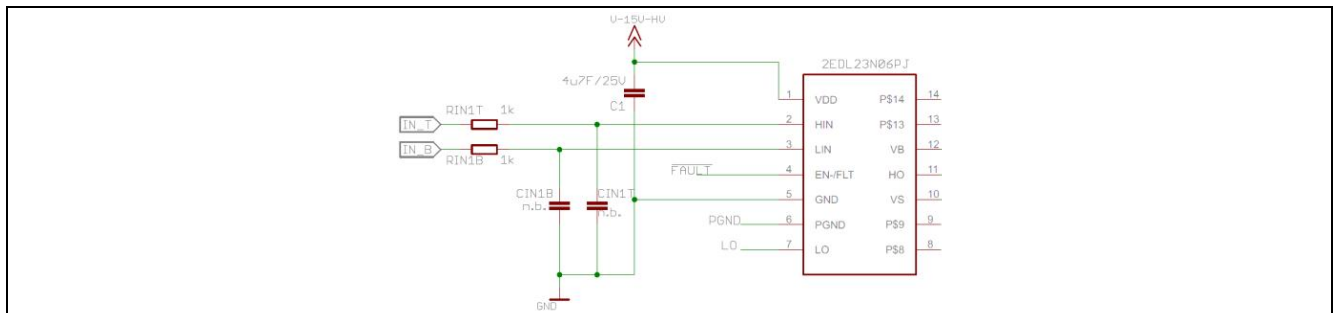


Figure 10 2EDL23N06PJ gate driver input

3.8 DC-Link capacitors

Due to the available space, there is only a small DC-Link capacitors of 2 x 330nF in series available according to Figure 13. A bigger DC-Link capacitance has to be connected externally to the connectors V+HV and GND_HV to cancel wiring inductances between voltage source and test board.

3.9 Connection of inductive load for non repetitive single pulse measurements

The test board is designed for resonant operation of the half-bridge. The inductive resonant tank is to be connected as shown in Figure 11.

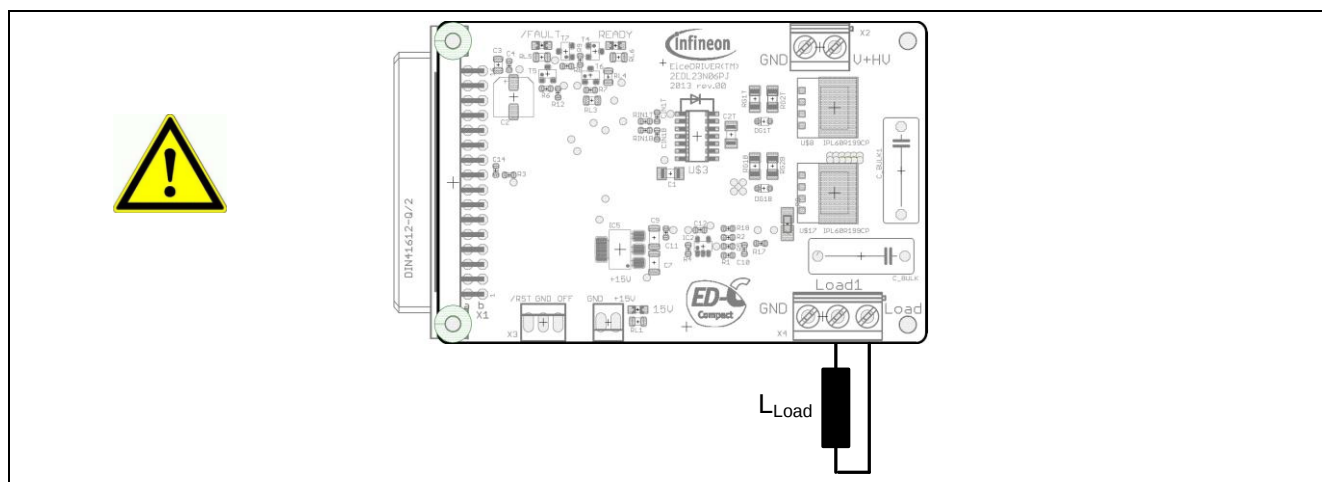


Figure 11 Connection of inductive load

A connection of the load to the screw terminal GND of X2/X4 and terminal LOAD of X4 is possible as well. Such connection can be used for single pulse measurements. **However please note, there is a risk of hard body diode commutation when using the load connection between GND and LOAD (valid for load connection between V+HV and Load as well)! This may damage the MOSFET transistors. The board is not designed to support multi pulse operation in this configuration!**

3.10 Example for resonant operation

The board is designed to support resonant operation under zero voltage switching turn-on conditions (ZVS). A load which is connected according to Figure 11 will result in a symmetric triangular load current shape as shown in Figure 12. The load circuit only draws reactive power and does not draw any real power. However, the half bridge switches must process the reactive power being drawn and therefore one can investigate the behavior of the 2EDL23N60PJ EiceDRIVER™ IC including the effects of the power transistors. Table 3 lists various circuit parameters proposed for operation of the resonant circuit. The resulting waveforms using these parameters are shown in Figure 12.

Table 3 Proposal of operating conditions

Parameter	Component	Value
switching frequency f_p	—	100 kHz
duty cycle d	—	49%
dead time DT	—	500 ns
Resonant load inductor	L_{Load}	800 μ H
Resonant load capacitor	C_{Bulk1} , C_{Bulk1}	330 nF
DC bus voltage V_{DC}	—	320 V
peak inductor current I_{pk}	—	1 A

Electrical features

The relation between various design parameters is described by Eqn. (1) where I_{pk} is the target peak current during operation, f_p is the switching frequency, L_{Load} is the load inductance and V_{DC} is the applied DC bus voltage.

$$I_{pk} = \frac{V_{DC}}{L_{Load}} \cdot \frac{1}{8f_p} = \frac{320\text{ V}}{800\text{ }\mu\text{H}} \cdot \frac{1}{8 \cdot 100\text{ kHz}} = 0.5\text{ A} \quad (1)$$

Please note, that the inductance saturation must be absolutely avoided. The saturation can lead to extremely high circuit currents, which may overload and consequently damage the power transistors. The use of air coils without any magnetic core is therefore recommended.

Eqn. (1) can be also used in order to calculate the needed load inductance in case that the switching frequency f_p and the target peak current I_{pk} are known. In this case Eqn. (1) changes to:

$$L_{Load} = \frac{V_{DC}}{I_{pk}} \cdot \frac{1}{8f_p} \quad (2)$$

The load current is symmetric around 0 axis without any DC component.

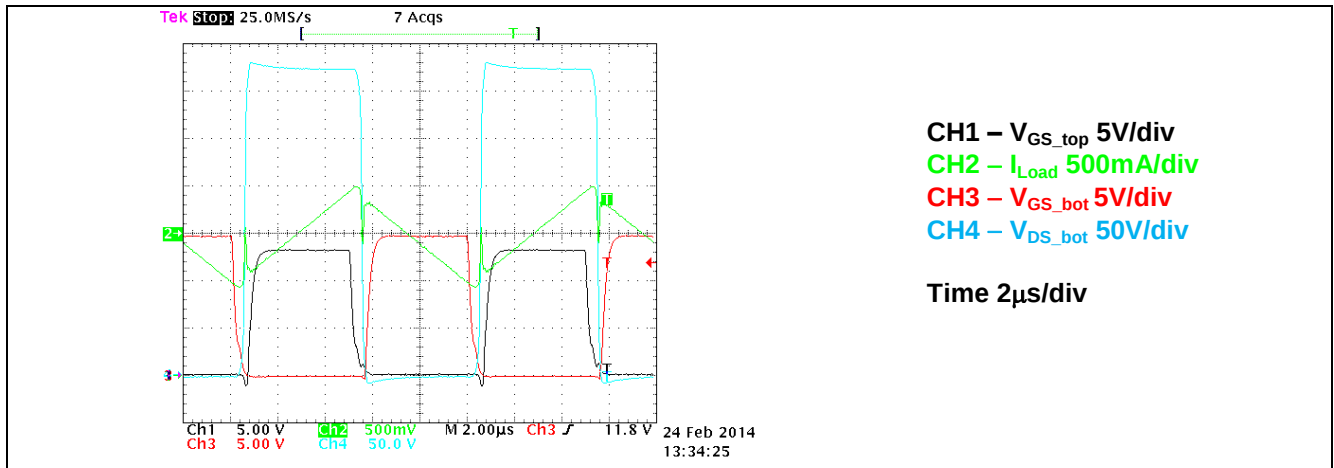


Figure 12 Load current shape in operation with load connected as shown in Figure 11

4 Board design details

4.1 Schematic



Figure 13 HV supply input (left) and DC-Link connection (right)

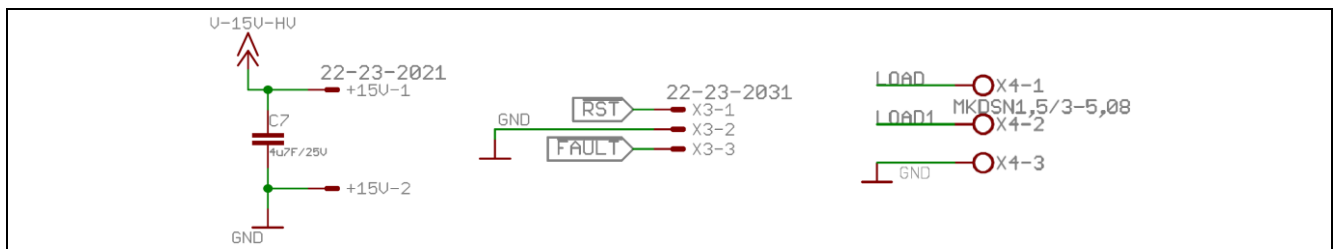


Figure 14 LV Supply and Reset Input and connector X4

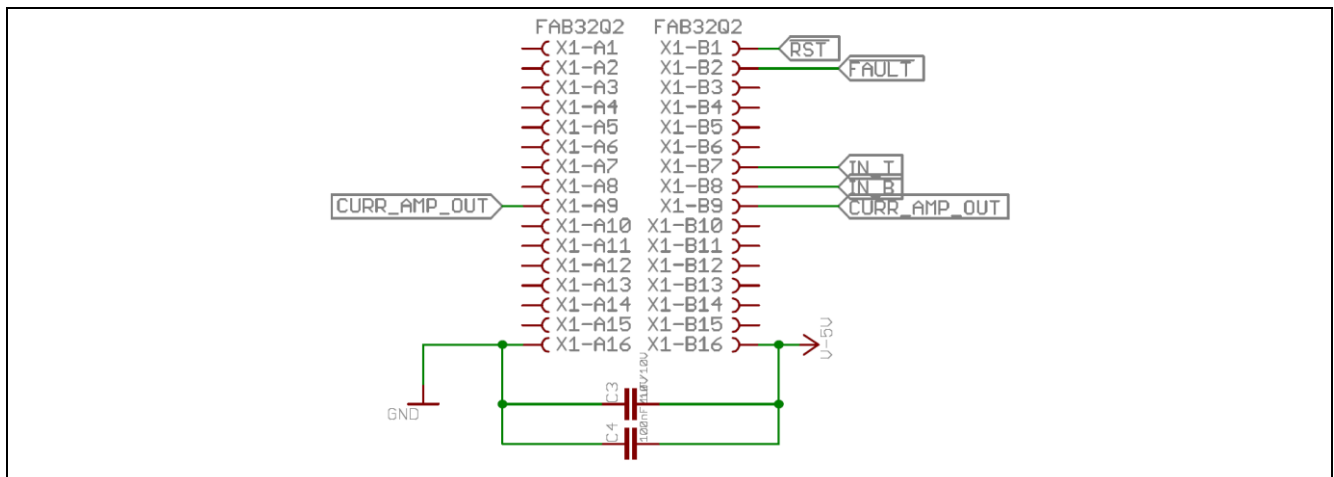


Figure 15 Connector X1

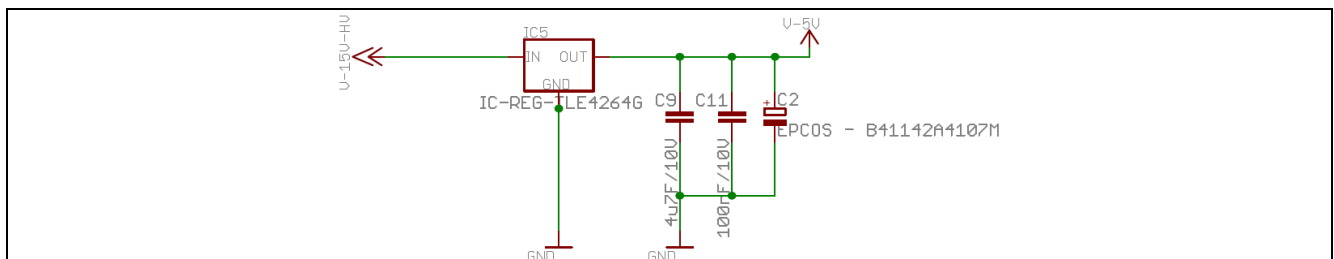


Figure 16 +5V linear regulator

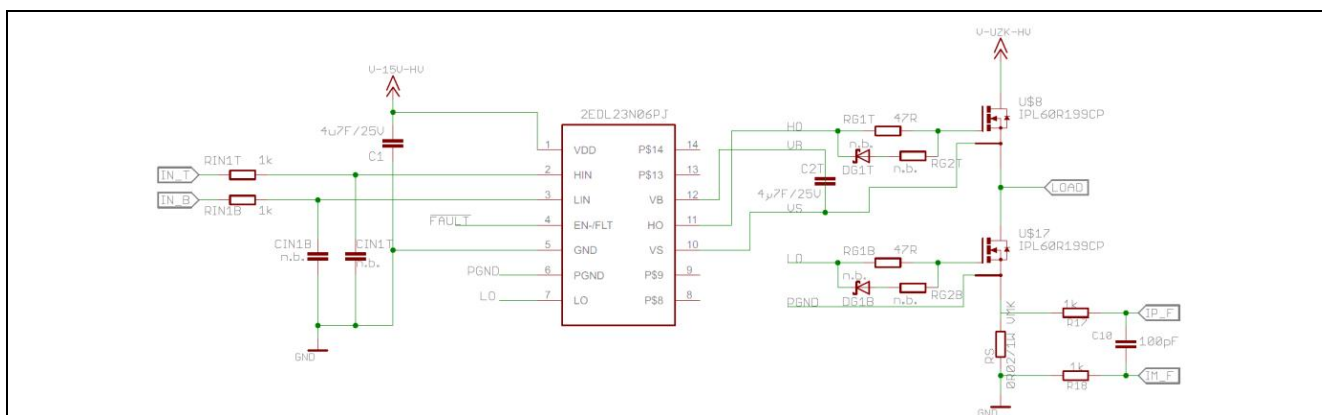


Figure 17 Infineon driver 2EDL23N06PJ with shunt measurement

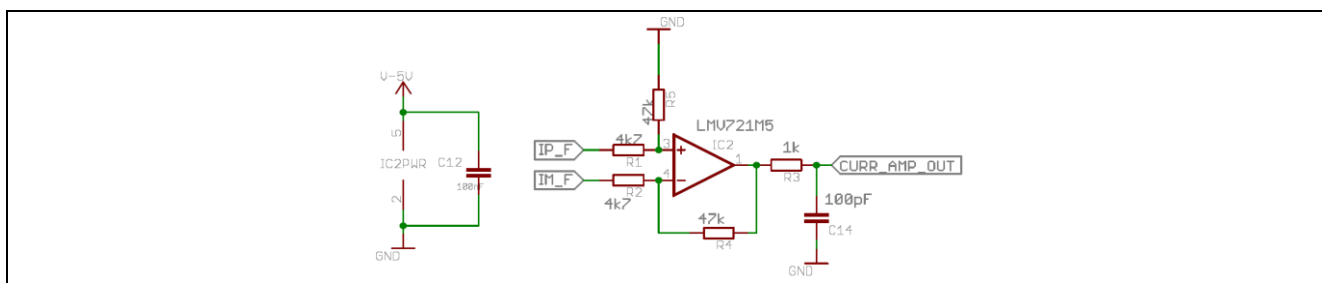


Figure 18 Current amplifier

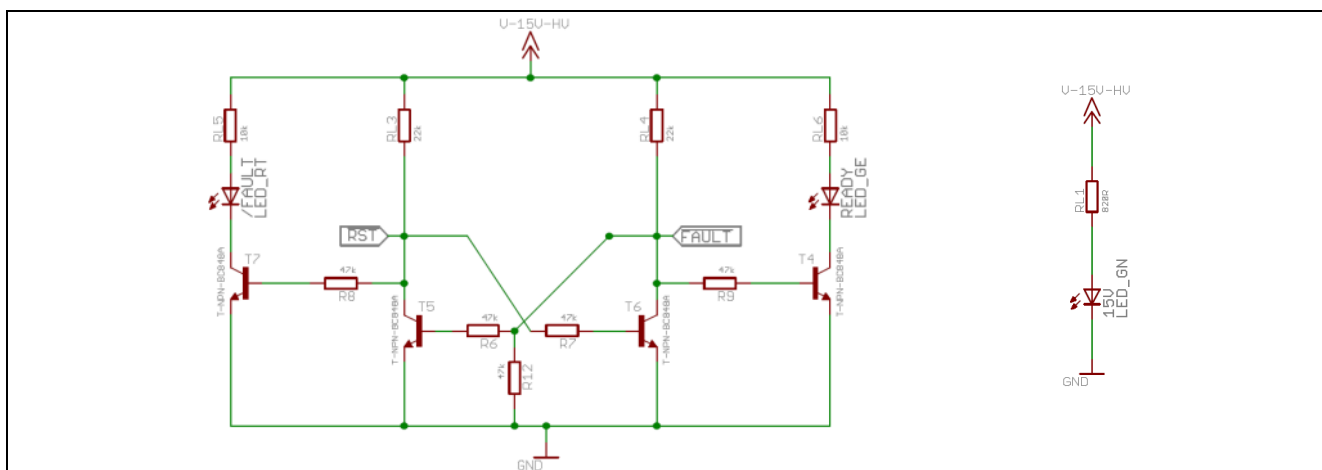


Figure 19 LEDs, FAULT and over current logic

4.2 Layout

4.2.1 Layout top layer

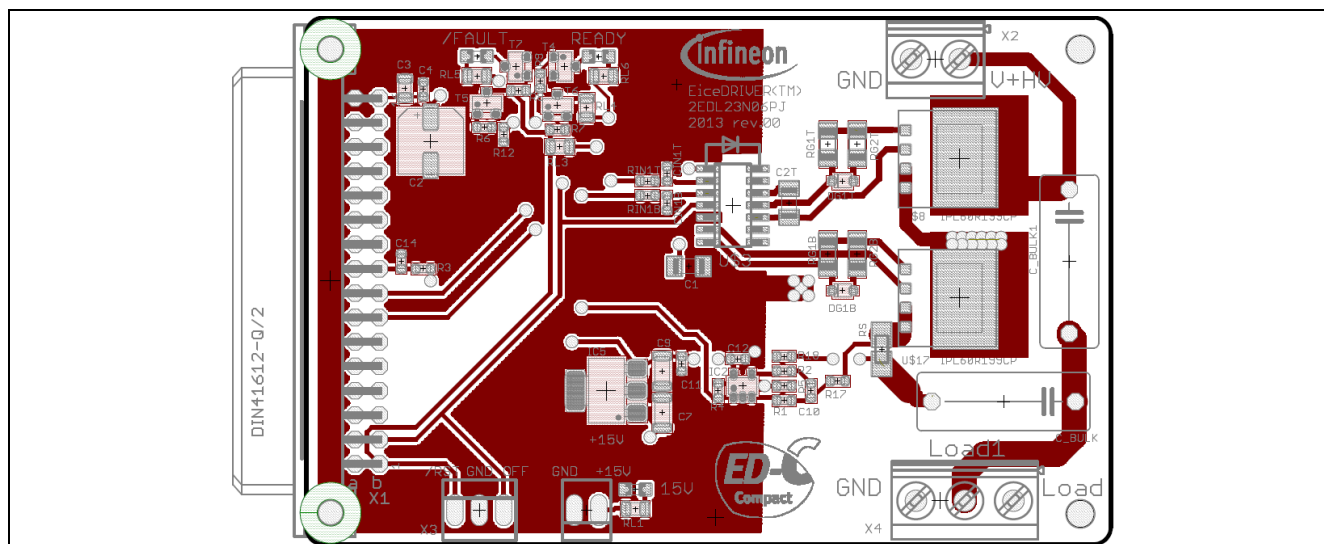


Figure 20 Layout top of the EVAL-2EDL23N06PJ

4.2.2 Layout bottom layer

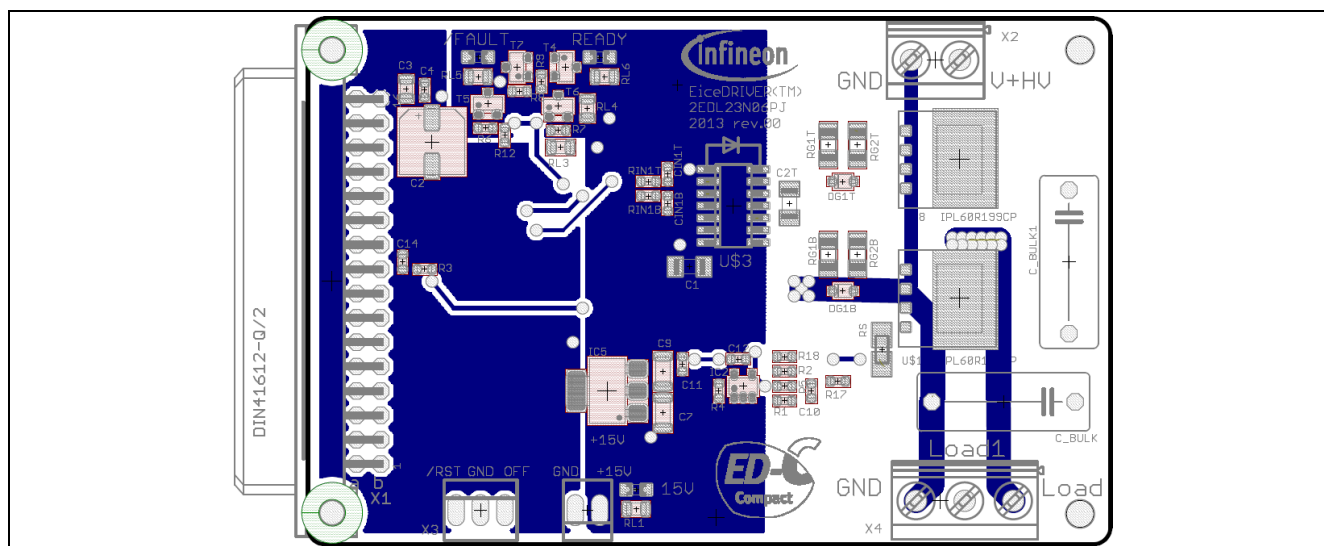


Figure 21 Layout bottom of the EVAL-2EDL23N06PJ

4.2.3 Layout top place

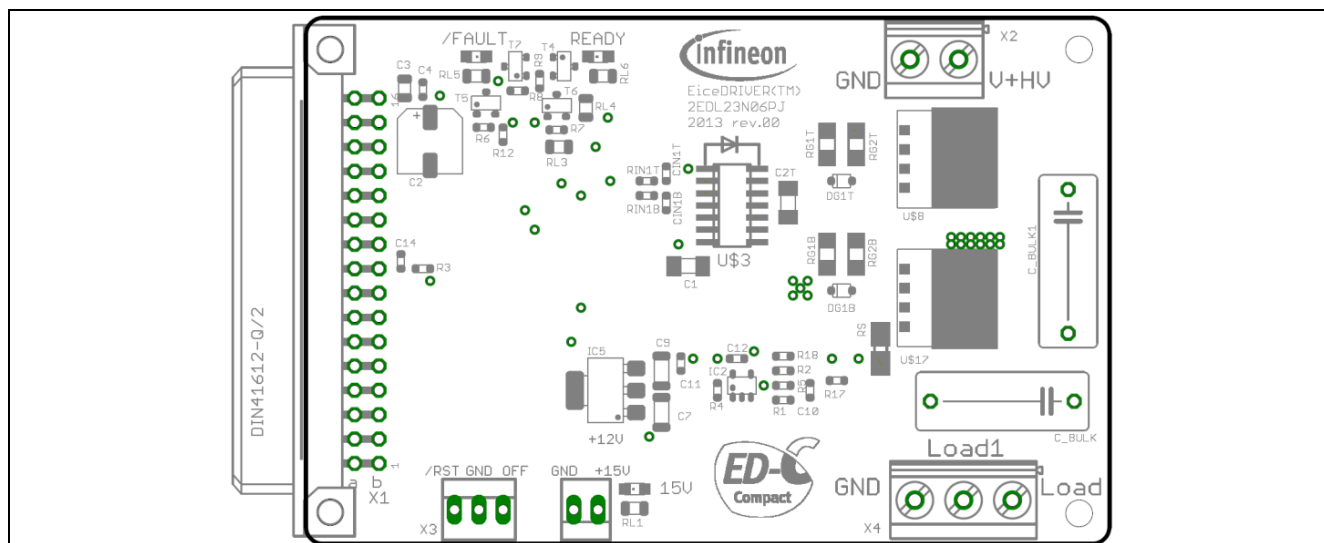


Figure 22 Top place view of the EVAL-2EDL23N06PJ

4.3 Bill of material

Part	Value	Package
C_BULK,C_BULK1	330nF, 450V	C-EU150-064X183
C1	4u7F/25V	C-EUC1206K
C10, C14	100pF	C-0603
C12	100nF	C-0603
C2	EEEFK1C101P 100µF/16V	SMD-C6.3x7.7
C2T	4µ7F/25V	C-1206
C3	1uF/10V	C-0805
C4, C11	100nF/10V	C-0603
C5, C6, C8, C13	nicht bestückt	C-EUC1206K
C7	4u7F/25V	C-1206
C9	4u7F/10V	C-1206
IC2	LMV721M5	IC-OP-TSV991AILT
IC5	IC-REG-TLE4264G	SOT223
R1, R2	4k7	R-0603
R3, R17, R18, RIN1B, RIN1T	1k	R-0603
R4, R5, R6, R7, R8, R9, R12	47k	R-0603
READY	LED_GE	LEDCHIPLED_0805
RG1B, RG1T	47R	R-EU_R1206
RL1	820R	R-0805
RL3, RL4	22k	R-0805
RL5, RL6	10k	R-0805
RS	0R02/1W	SMT-REF
T4, T5, T6, T7	T-NPN-BC848A	T-NPN-BC848A
U\$3	2EDL23N06PJ	2EDL_SO14-2_3A
U\$8, U\$17	IPL60R199CP	COOLMOS_THINKPAK
X1	FAB32Q2	FAB32Q2
X2	MKDSN1,5/2-5,08	MKDSN1,5/2-5,08
X3	22-23-2031	22-23-2031
X4	MKDSN1,5/3-5,08	MKDSN1,5/3-5,08

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