650V CoolMOS™ C6/E6

Features and Benefits of 650V CoolMOS™ C6/E6

Application Note

About this document

Scope and purpose

This application note describes the characteristics and features of 650 V CoolMOS™ C6 and E6 and how it differentiates from earlier CoolMOS™ technology. In addition, key parameters of the device which are critical in achieving the desired efficiency and reliability of the application are discussed in details. Moreover, the evaluation result in PFC stage application is also presented to provide an overview of the efficiency benefit of CoolMOS™ C6 and E6.

Intended audience

This document provides designers a guideline on how to use the device in a wide array of applications from low to high power to attain an efficient and robust solution with minimum design effort and improved overall cost.

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1 Introduction

With fifth Superjunction generation CoolMOS™ C6 Infineon Technologies has set a standard in the market for high voltage MOSFETs. After launching the 600 V class in 2009, C6 technology is now also available in 650 V. CoolMOS™ C6 technology implements a combination of ultra-low $R_{DS(on)}$, high ruggedness and fast but well controlled switching speed. The application measurements show very good light load efficiency in comparison to our own devices and competitor parts, a fault tolerant behavior in abnormal conditions such as turn-on on a conducting body diode and a well controlled switching characteristic especially in peak current conditions such as load steps, start-up and AC cycle drop out etc. Last but not least the cost associated with the production of a given $R_{DS(on)}$ was reduced, allowing us to offer lower prices compared to previous CoolMOS™ generations.

CoolMOS™ C6 comes with an integrated gate resistor in order to achieve self-limiting di/dt and dv/dt characteristics. This is especially important for consumer applications such as adapters for notebooks and printers, where easy implementation and lowest noise levels are key requirements.

To allow for maximum flexibility in design-in, the technology platform is also offered with reduced integrated gate resistor for a part of the offered $R_{DS(on)}$ range, promoted as CoolMOS™ E6 series. This we consider particularly important for applications where highest efficiency and power density are key requirements.

In summary, the combination of 650 V CoolMOS™ C6 and E6 series is capable to fulfill the needs of a very wide range of applications comprising fields such as computing, lighting, industrial, and consumer.

This document is particularly showing results of application measurements and application relevant measurements for 650 V CoolMOS™ C6 and E6 in comparison to 650 V CoolMOS™ C3.

For a general introduction of the CoolMOS™ C6 technology together with a comparison to other CoolMOS technologies, please refer to the application note CoolMOS™ C6 - Mastering the Art of Slowness available on our homepage.

2 Technology Characteristics of CoolMOS™ C6 and E6 650V

CoolMOS™ C6 and E6 products are well balanced modern Superjunction high-voltage MOSFETs with the following **characteristics**:

- Fast but well controlled switching speed
- Very low energy stored in output capacitance
- High ruggedness in hard commutation of the body diode
- Low gate current requirements

This gives the application **benefits** like:

- Compact and very efficient designs
- Fast and easy design-in, less care for peak current conditions such as during start-up, load jump, AC cycle drop out etc.
- Very good light load efficiency in hard turn on applications
- If low Q_{rr} is not key requirement, no need for more expensive fast body diode types
- No need for high current gate drivers, better system cost and more choice

2.1 Key Parameters

Table 1 shows a comparison of key characteristics as published in the datasheet.

Table 1 Key feature comparison of CoolMOS™ C3 versus C6 and E6 series

Specification	Symbol	SPP15N65C3	IPP65R280C6	IPP65R280E6
On-state resistance, maximum rating, 25 °C	$R_{DS(on)}$	280 mΩ	280 mΩ	280 mΩ
Drain current rating	I_D	15 A	13.8 A	13.8 A
Pulse current rating	$I_{D,pulse}$	45 A	39 A	39 A
Typical Gate - Drain charge	Q_{gd}	29 nC	24 nC	24nC
Total Gate charge	Q_g	63 nC	45 nC	45 nC
Energy stored in output capacitance @400V	E_{OSS}	5.7 µJ	3.7 µJ	3.7 µJ
Thermal resistance, junction-case	$R_{thJC,max}$	0.8 K/W	1.2 K/W	1.2 K/W
Body diode, reverse recovery charge	Q_{rr}	8 µC	3.6 µC	3.6 µC
Body diode, di/dt	di_F/dt	400 A/µs[1]	500 A/µs	500 A/µs
Body diode, dv/dt	dv/dt	15 V/ns[1]	15 V/ns	15 V/ns
Gate resistance	R_G	1.4 Ω	12.5 Ω	7.0 Ω

The target for CoolMOS™ C6 is to provide fast but controlled switching and a good compatibility with layouts, where source inductances have not been brought to the absolute minimum. The basic idea is to provide a high voltage MOSFET, which is significantly fast at normal operation conditions and very limited

[1] Not specified in datasheet

overshoot in di/dt or dv/dt at high peak current conditions. With its outstanding behavior during hard commutation of the body diode CoolMOS™ C6 and E6 is very well suited for resonant applications.

2.2 The difference between CoolMOS™ C6 and E6: Integrated Gate Resistor

CoolMOS™ C6 comes with an integrated gate resistor in order to achieve self-limiting di/dt and dv/dt characteristics. This integrated R_G allows fast turn on and turn off at normal operating current conditions but limits the di/dt and dv/dt in case of peak current conditions. The values of integrated R_G scales inversely with the gate charge respectively device capacitances.

A part of the portfolio is available with reduced integrated gate resistor in order to support applications where highest efficiency and power density are key requirements. These devices represent the CoolMOS™ E6 series.

The following values have been chosen for CoolMOS™ C6 and E6 series:

Type	C6 R_G [Ω]	E6 R_G [Ω]
IPx65R600x6	17.5	10.5
IPx65R380x6	17.0	7.5
IPx65R280x6	12.5	7.0
IPx65R190x6	8.5	6.0

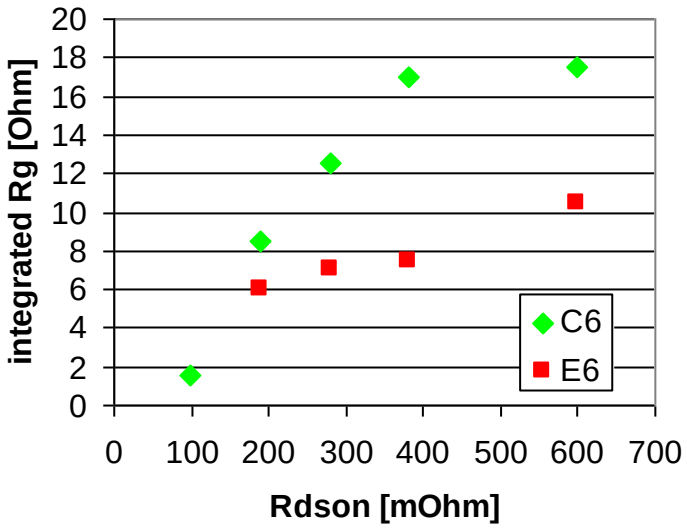

Figure 1 Integrated Gate resistor for CoolMOS™ C6 versus E6 series

Please note that the C6 devices with $R_{DS(on)}$ values below 99 mΩ come with very low integrated gate resistances. Low $R_{DS(on)}$ values require larger silicon area and thus exhibit larger device capacitances. For those parts it is not necessary additionally limit the di/dt and dv/dt values. Low ohmic C6 parts are therefore ideally suited for applications with highest efficiency requirements, like e.g. solar inverters.

Due to low gate charge plus integrated gate resistors the gate current is relatively low; hence the use of low cost gate drivers is possible. In case of e.g. the 190 mΩ C6 part the 8.5 Ω integrated R_G limits the gate current to less than 2A even when switching with 0 Ω external R_G from 0 to 15 V. During the Miller phase the gate current will typically be even less than 1 A. In combination with a relatively low total gate charge the losses dissipated in the driver are considerably lower as well.

We encourage using very small external gate resistors especially for the C6 technology to achieve optimum efficiency across a wide range of load conditions.

2.3 Switching Characteristics

2.3.1 Switching Speed

Figure 1 and Figure 2 show a technology comparison of C3 versus C6 and E6 for di/dt and dv/dt both during turn on and turn off at currents of 3.3 A and 13.8 A respectively. All measured parts have a maximum on-state resistance of 280 mΩ, the used gate resistance is 3.4 Ω.

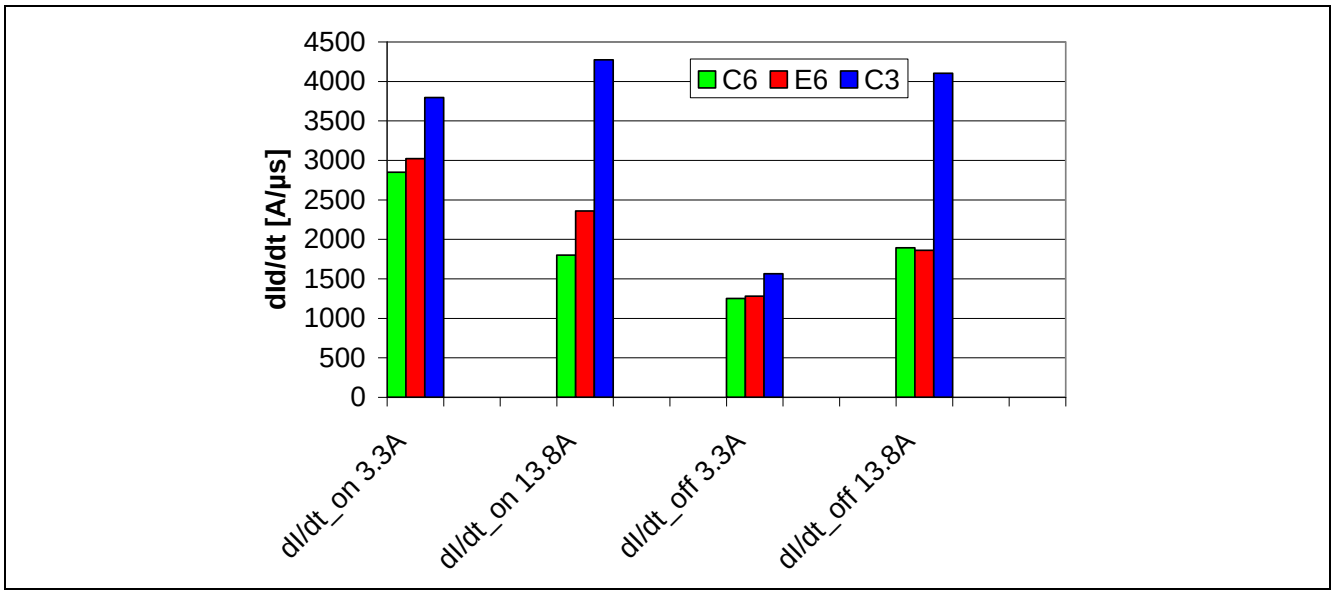

Figure 2 Comparison of switching characteristic, di/dt at turn on and turn off for 3.3 A and 13.8 A respectively, 280 mΩ types, R_G=3.4 Ω, V_G=13 V, T_j=125°C

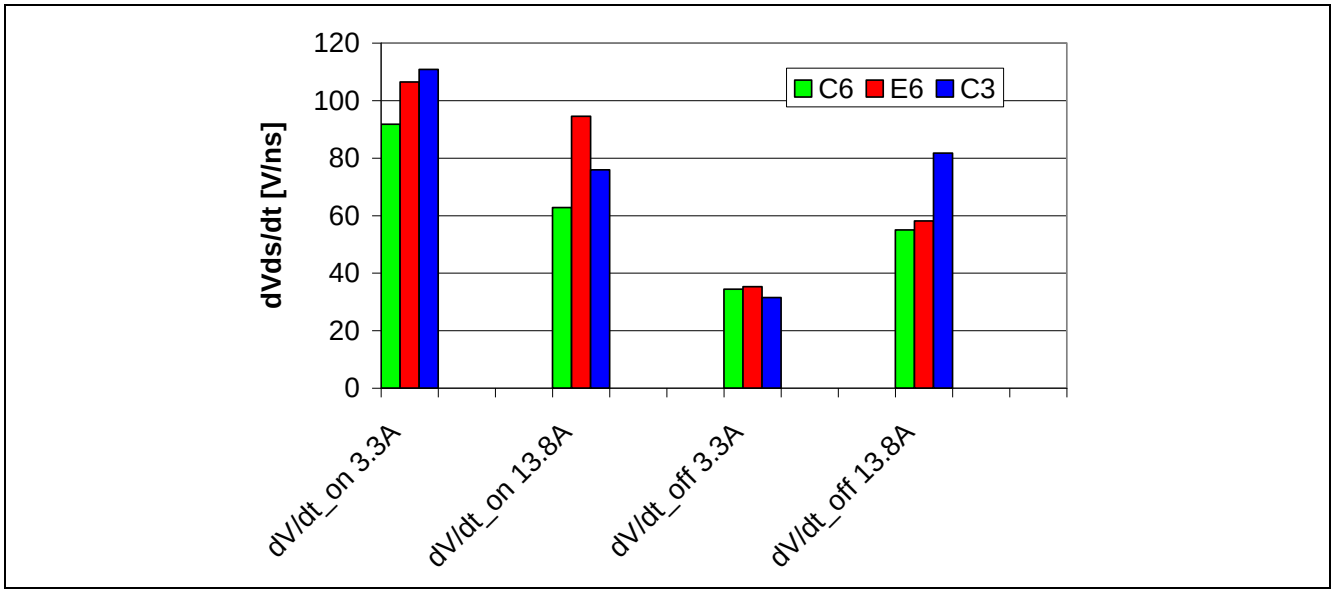

Figure 3 Comparison of switching characteristic, dv/dt at turn on and turn off for 3.3 A and 13.8 A respectively, 280 mΩ types, R_G=3.4 Ω, V_G=13 V, T_j=125°C

Figure 2 and Figure 3 show di/dt and dv/dt results of a measurement with very low gate resistance at normal operating currents as well as high currents (even above nominal DC current) to demonstrate the nicely controlled switching behavior even under non-standard operating conditions.

CoolMOS™ C6 and E6 show relatively low values of di/dt during turn off. During turn-on di/dt values are significantly lower than for CoolMOS™ C3. For C6 and E6 there is no increase in di/dt during turn on (in this measurement even a decrease of di/dt for higher currents was detected) and only an increase to moderate values in di/dt during turn off when the current changes from 3.3 A to 13.8 A. This enhances design safety in peak current conditions such as AC cycle drop out, start up or load jumps as the di/dt is likely above the range of normal operation conditions. Therefore the likelihood of unwanted oscillations or dangerous gate spikes is significantly suppressed.

For those who might consider the di/dt values at turn off rather low, please remember that di/dt values of 500 A/µs and a source inductance of 10 nH only will already yield a voltage drop of 5 V, which will bring the MOSFET already for short time into the Miller plateau via inductively induced turn on. As both the TO-220 and TO-247 package have parasitic source inductances of 5nH already there is little room for layout routing to stay below 10 nH. In other words with conventional packages such as TO-220 or TO-247 there is little to no benefit from higher switching speeds than 800 to 1000 A/µs. The self limitation of di/dt being implemented in CoolMOS™ C6 and E6 does therefore not hurt efficiency wise but brings safety in peak current conditions and helps with the use of the part in non-ideal layout environments.

Looking at dv/dt, the device is able to achieve very fast turn on and turn off transients to provide low turn on and turn off losses. At high currents (peak current conditions) the dv/dt values are limited compared to C3, allowing to stay within the datasheet specification with comparably low external R_G values and thus not reducing switching speed in normal operating conditions. The dv/dt values are in general close to what CoolMOS™ C3 would yield under identical conditions, thus facilitating the change of designs from C3 into C6/E6 to participate in the best-in-class offerings, improved E_{OSS} and gate charge characteristics and last but not least attractive price structure of the more modern CoolMOS™ class. Furthermore CoolMOS™ C6 and E6 do not show extremely high dv/dt values at turn off under peak current conditions, as untamed Superjunction devices naturally tend to do due to ever decreasing output capacitance. The device offers therefore well controlled switching behavior with significantly suppressed tendency to unwanted ringing and gate spikes.

Figure 2 and Figure 3 clearly demonstrate the design-in flexibility that is offered with the additional E6 series which is offered with reduced integrated gate resistor, allowing for highest efficiency and power density. Customers are able to choose the device that matches their optimum trade-off between lowest losses and ease of use.

2.3.2 Switching Waveforms and Noise Considerations

In Figure 4 the measured switching waveforms of the device are shown for a typical PFC stage exhibiting 7.2 pF capacitive coupling between gate and drain on the PCB circuit. This parasitic capacitance can be the source for noise on the switching waveforms. In new layouts designers should take care to minimize this external gate to drain capacitance to enable highest performance of MOSFETs. Gate waveforms (in magenta) are shown for increasing drain current (in turquoise). Conditions applied at the device are V_{DS}=400 V (shown in green) and V_G=15 V. The current is increased during every pulse up to saturation current. All devices were measured with an external gate resistance of only 0.5 Ω, to visualize the clear difference of switching behavior between devices. The magnified waveform shows the gate turn-on of the last pulse before saturation, i.e. at very high currents of up to 60 A. C6, with the highest integrated R_G, shows an excellent switching waveform, no gate spikes are visible up to four times nominal current. The noise level to be expected from CoolMOS™ C6 also in terms of EMI can be expected to be very low. Also the variant with

reduced internal gate resistance, CoolMOS™ E6, shows very good switching waveforms, with even lower noise level than the previous generation CoolMOS™ C3.

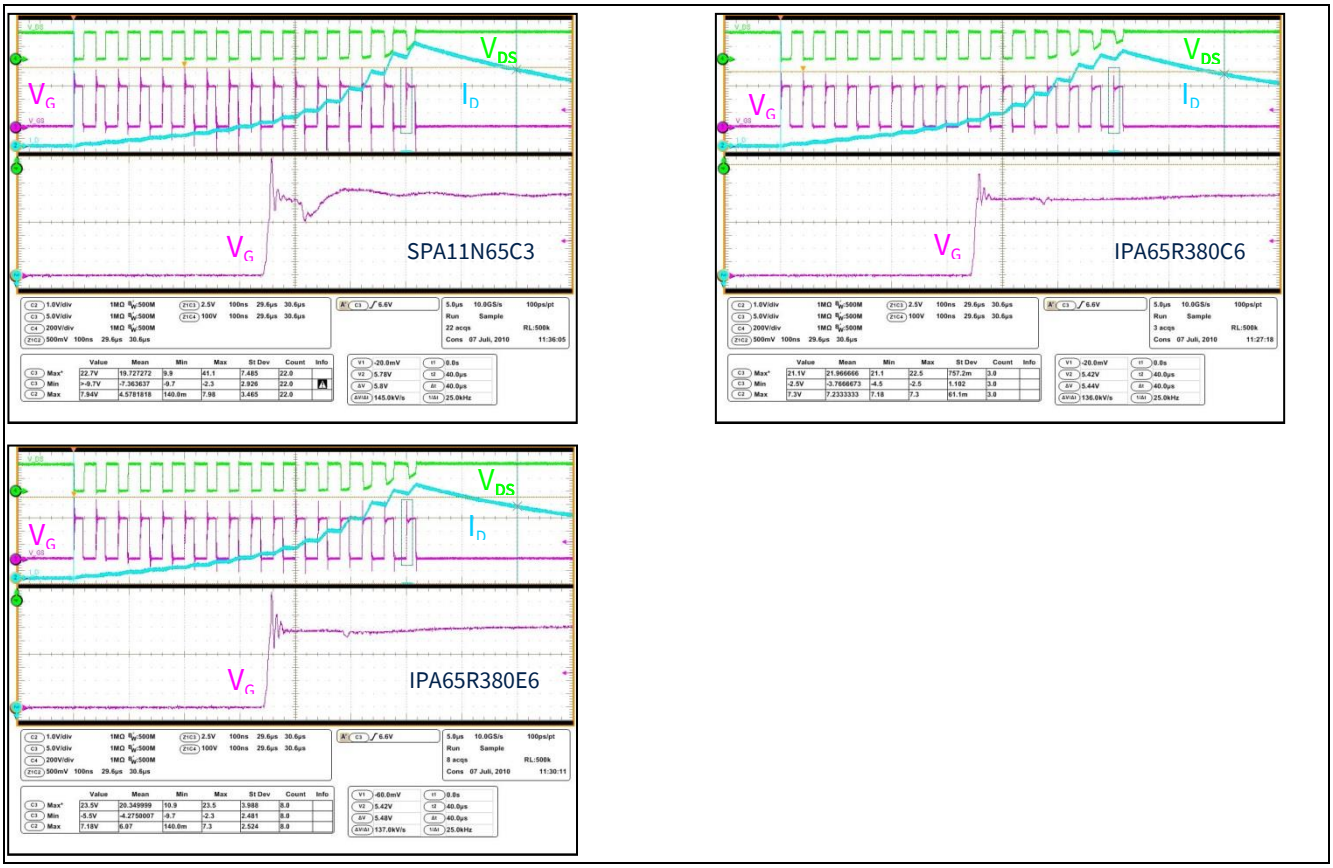

Figure 4 Measured switching waveforms during current ramp up in a CCM PFC stage exhibiting a $C_{gd,ext}$ of 7.2 pF for 380mΩ devices of CoolMOS™ C3, C6 and E6 with $R_{G,ext}$=0.5 Ω

The waveforms show that the integration of a high enough gate resistance allows to easily design-in modern superjunction devices in applications that have high parasitics inherent to the layout. This way the benefit of lowest device capacitances can be fully used without sacrificing ease of use of the device.

In order not to sacrifice efficiency, please make sure the external gate resistance is reduced compared to previously used MOSFETs (please refer to table 2 for internal R_G values).

Despite all measures taken from a device design point of view to suppress gate spikes Infineon Technologies recommends the layout suggestions and gate driver setup as e.g. described in the application note CoolMOS™ CP. The use of ferrite beads on the gate is generally recommended for paralleled devices.

2.4 Device Capacitances,

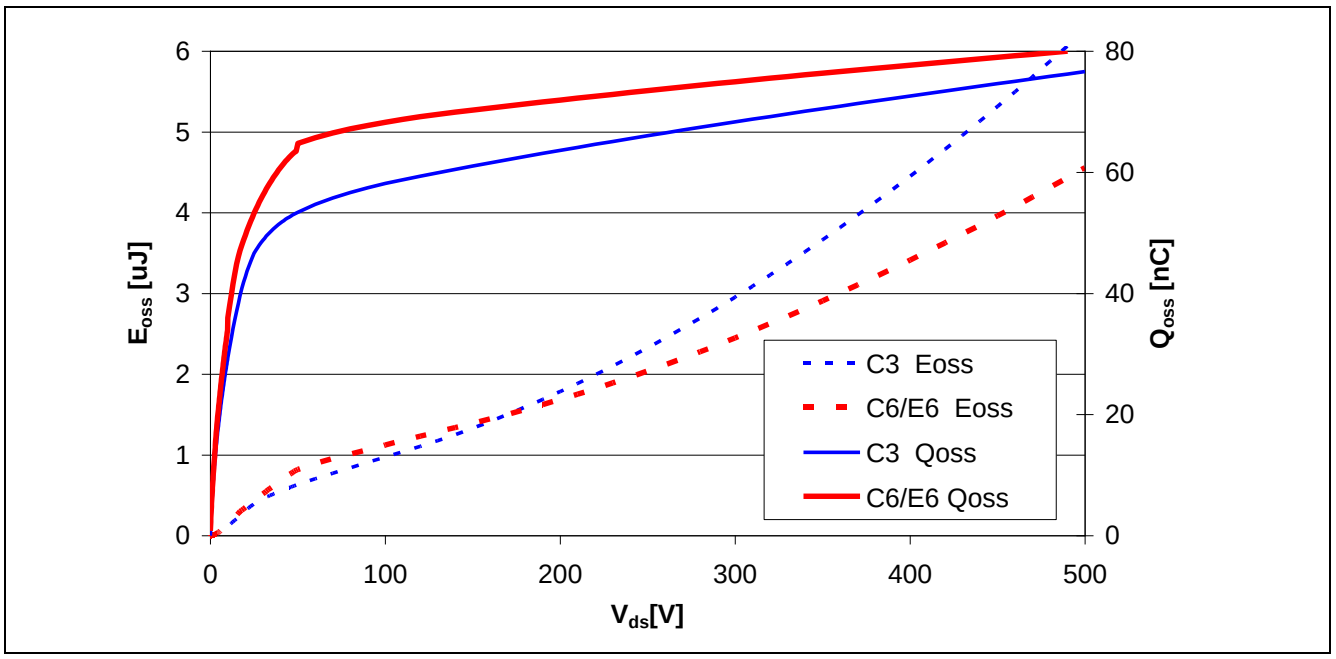

Figure 5 Figure 5: Comparison of the energy stored in the output capacitance E_{oss} and the capacitive displacement charge Q_{oss} for CoolMOS™ C3 versus C6 and E6, $R_{DS(on),max}$=280 mΩ

Figure 5 shows a comparison of the energy stored in the output capacitance E_{oss} and the capacitive displacement charge Q_{oss} as a function of the voltage the device is charged up to. As it can be clearly seen from the graph the new CoolMOS™ generations C6 and E6 shows the best E_{oss} values at 400 V, which helps to lower the capacitive losses in applications with hard turn on such as continues current mode PFC applications. As the capacitive losses are load independent these loss contribution typically dominates during light load conditions, when both conduction and Joule switching losses get lower due to their square or linear relationship with load current respectively. At 200 V the E_{oss} curve of C6 intersects with C3 yielding similar capacitive losses at this operation point, which is e.g. important for Two Transistor Forward (TTF) and Interleaved TTF topologies. Please note that CoolMOS™ C6 and E6 have identical device capacitances.

The Q_{oss} charge is a measure for the time it takes to charge up the device from 0V to the voltage shown on the X-axis. This time is important for the dead time considerations in resonant switching applications such as the LLC converter. The capacitive displacement charge Q_{oss} of CoolMOS™ C6 and E6 at 400 V is ~7% higher than for CoolMOS™ C3 and would therefore require an adaption of the dead time of about the same percentage.

2.5 Behavior during hard commutation of the body diode

An important point in resonant switching applications is the topology's inherent possibility of turning on into the conducting body diode of the same leg. This condition may appear in LLC converters during start up or heavy load jumps and is also not unknown in phase shift ZVS topologies. As such conditions do not happen during normal operating conditions the body diode behavior of the MOSFET is not influencing efficiency but is an important factor for high reliability of the design.

CoolMOS™ C6 and E6 allow for an inherent active re-turn on of the device after the body diode conduction in the current discontinuation phase. The voltage overshoot can be limited actively by choosing a higher gate turn off resistor value which is balancing of the self driven dv/dt triggered turn on and di/dt triggered turn off.

Technology Characteristics of CoolMOS™ C6 and E6 650V

Figure 6 shows the excellent waveforms of CoolMOS™ C6 and E6 during hard commutation of the body diode. The voltage overshoot is limited by the device itself.

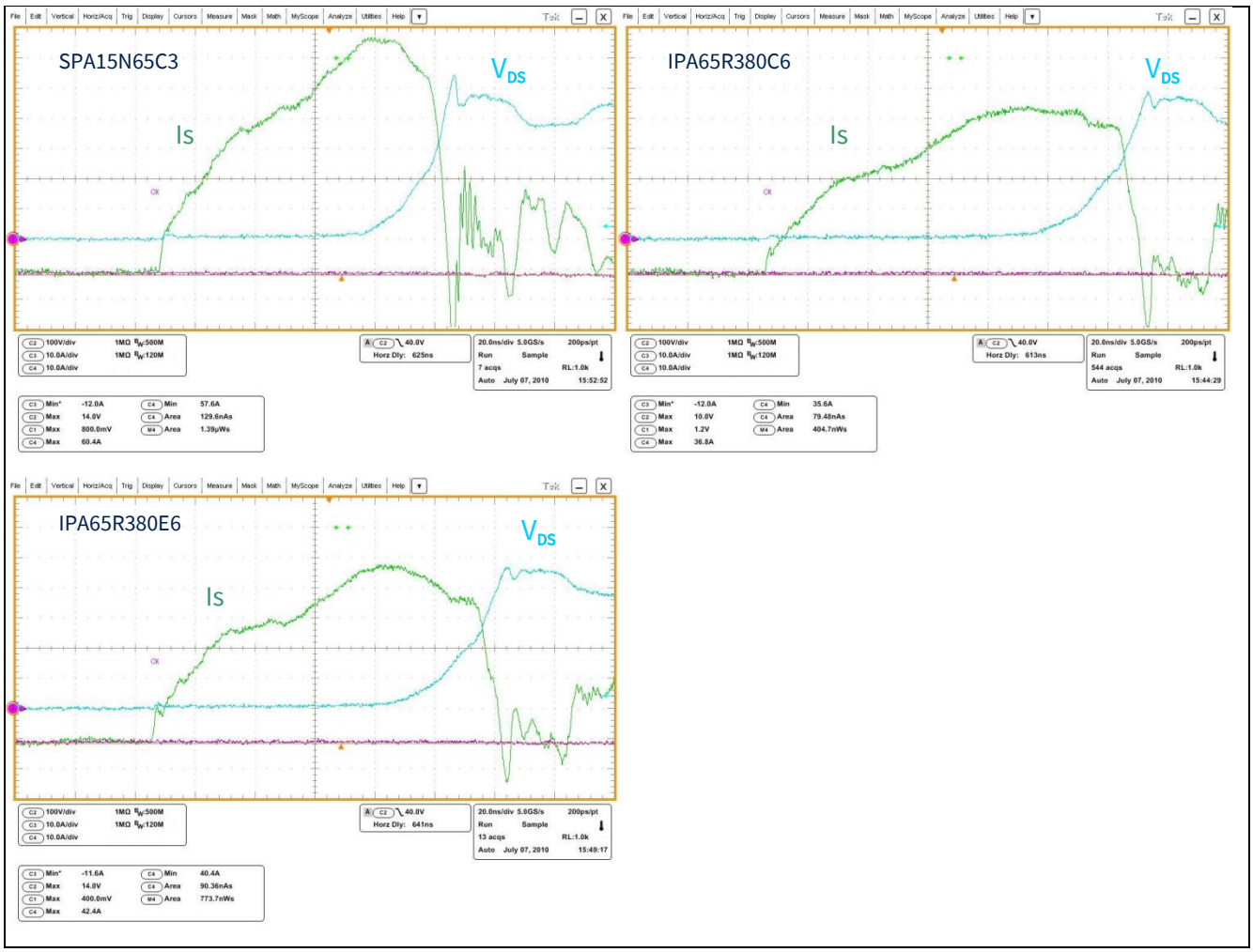

Figure 6 Hard commutation on the body diode for CoolMOS™ C3, C6 and E6. 280 mΩ types, $R_{G,ext}$=10 Ω, I_D=10 A, V_{DS}=400 V

3 Application Results

3.1 PFC stage of a 300W Power Supply

Driven by initiatives such as 80+ and the ubiquitous energy efficiency demands power supplies need to deliver a very high efficiency over a broad load and input voltage range. These requests translate into more demanding semiconductor requirements as well as more strict discipline in avoiding parasitic inductances and capacitances in the layout.

As seen in Figure 7, CoolMOS™ C6 and E6 generations allow for same efficiency characteristics as achieved with CoolMOS™ C3 if the same total gate resistance is used (external R_G + integrated R_G). For this measurement the used external gate resistors were very different, ranging from 10 Ω for C3 and 6.8 Ω for E6 to 0.3 Ω for C6 to give the same total gate resistance in the range of 12.6 Ω.

As shown in chapter 2.3.2, the switching waveforms of C6 are cleaner than for C3 using same external R_G, allowing for safe operation of CoolMOS™ C6 with much lower external R_G than typically used. C6 is therefore ideally suited to replace C3 if the external gate resistor is adjusted to lower values.

As a high integrated R_G represents a natural limit in efficiency for those applications that run with very low $R_{G,ext}$ already today, the E6 series is offered with lower integrated R_G to provide the optimum solution also for such applications.

Please note that the $R_{G,int}$ differences of the technologies need only be taken into account in the $R_{DS(on)}$ range 190 mΩ to 600 mΩ which is mainly used in consumer applications where easy implementation and lowest noise levels are key requirements.

For $R_{DS(on)}$ values below 100mΩ, additional self limitation of di/dt and dv/dt characteristics is not necessary. The internal gate resistance for C6 is chosen to be as low as for previous technology generations and is able to satisfy highest efficiency requirements.

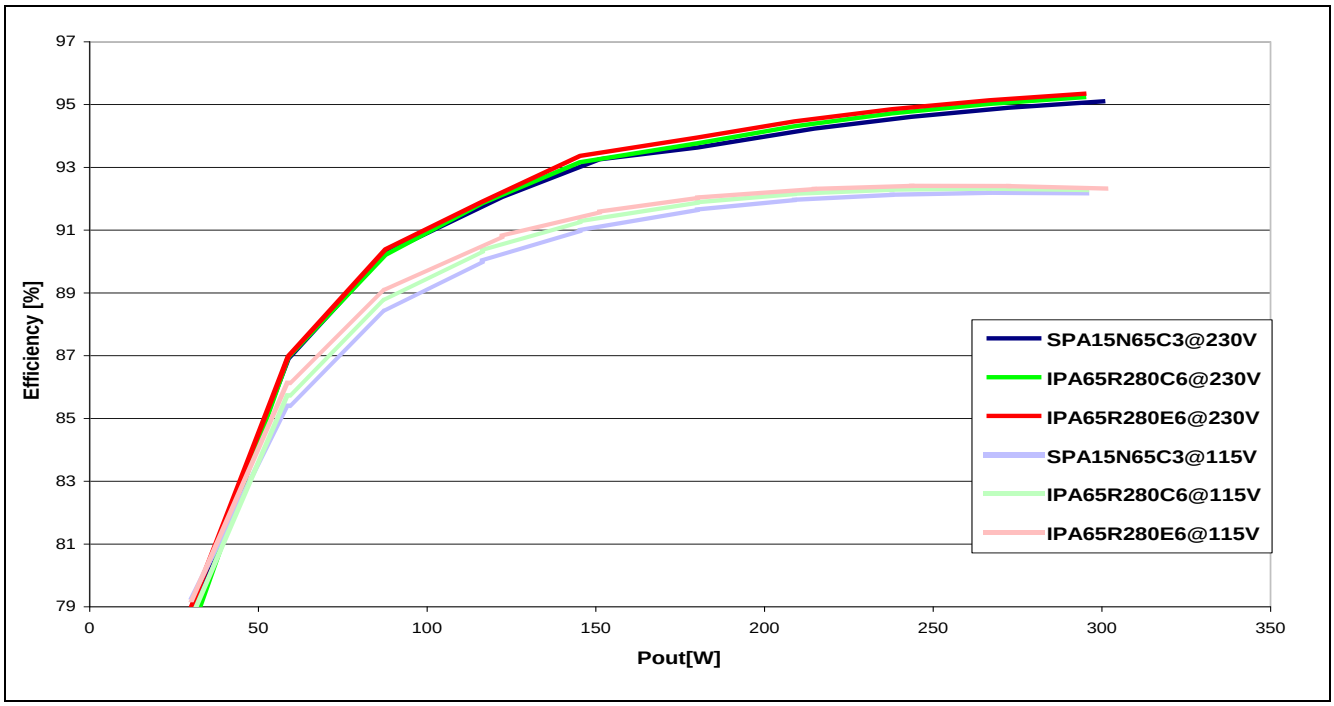

Figure 7 System efficiency versus load of a 300 W PFC in DCM, comparing 650 V CoolMOS™ C3, C6 and E6 in high line and low line operation. All devices were measured with R_{G_on}=10Ω and a comparable total R_{G_off} ($R_{G,int}$+$R_{G,ext}$) of 11.4 to 13.8 Ω.

4 Product Portfolio and Naming System

650V CoolMOS™ C6 and E6 series follow the same naming guidelines as already established with the CP series e.g. IPP65R099C6, where I stands for Infineon Technologies, P for power MOSFETs, P for the package TO-220, 65 for the voltage class (divided by 10), R099 for the on-state resistance in milliohms and C6 for the name of the series.

650V CoolMOS™ C6

I_D [A]	$R_{DS(on)}$ [mΩ]	TO-220	TO-262 (I^2PAK)	TO-263 (D^2PAK)	TO-220 FullPAK	TO-247	TO-252 (DPAK)	ThinPAK 5x6
83,2	37					IPW65R037C6		
53,5	70					IPW65R070C6		
57,7	74	IPP65R074C6						
38,0	99	IPP65R099C6	IPI65R099C6	IPB65R099C6	IPA65R099C6	IPW65R099C6		
20,2	190	IPP65R190C6	IPI65R190C6	IPB65R190C6	IPA65R190C6	IPW65R190C6		
16,1	250						IPD65R250C6	
13,8	280	IPP65R280C6	IPI65R280C6	IPB65R280C6	IPA65R280C6	IPW65R280C6		
10,6	380	IPP65R380C6	IPI65R380C6	IPB65R380C6	IPA65R380C6		IPD65R380C6	
7,3	600	IPP65R600C6	IPI65R600C6	IPB65R600C6	IPA65R600C6		IPD65R600C6	
	650							IPL65R650C6S
4,5	950						IPD65R950C6	
	1000						IPD65R1K0C6	IPL65R1K0C6S
3,2	1400						IPD65R1K4C6	IPL65R1K5C6S

Figure 8 Portfolio of 650 V CoolMOS™ C6

650V CoolMOS™ E6

I_D [A]	$R_{DS(on)}$ [mΩ]	TO-220	TO-251 (IPAK SL)	TO-262 (I^2PAK)	TO-263 (D^2PAK)	TO-220 FullPAK	TO-247	TO-252 (DPAK)	ThinPAK 8x8
20.2	190	IPP65R190E6				IPA65R190E6	IPW65R190E6		IPL65R190E6
16.1	250							IPD65R250E6	
13.8	280	IPP65R280E6		IPI65R280E6	IPB65R280E6	IPA65R280E6	IPW65R280E6		
13.1	310								IPL65R310E6
10.6	380	IPP65R380E6				IPA65R380E6		IPD65R380E6	
	420								IPL65R420E6
7.3	600	IPP65R600E6	IPS65R600E6			IPA65R600E6		IPD65R600E6	
6.7	660								IPL65R660E6

Figure 9 Portfolio of 650 V CoolMOS™ E6

Revision History

Major changes since the last revision

Revision	Description of change
1.0	First Release
1.1	Modify front page contents; update CoolMOS™ C6 and E6 portfolios in page #11

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Do you have a question about any aspect of this document?

Email: erratum@infineon.com

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