TVS Diodes in Chip Scale Package reduce size and save cost

ESD108-B1-CSP0201
ESD119-B1-W01005
ESD200-B1-CSP0201
ESD202-B1-CSP01005

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Page	Device naming: ESD119-B1-CSP01005 => ESD119-B1-W01005

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1 Introduction

Modern electronics market, and especially mobile devices market is driven by two main trends:

- Miniaturization and integration
- Increasing complexity and data rates

Miniaturization leads to reduced maximal allowed voltages and smaller margin between working- and maximal allowed voltage. For example, ICs manufactured in 130nm technology commonly have second breakdown trigger voltage Vt2 around 13V. For 28nm technology this value drops to only 4V. Sensitivity of the components to overvoltage, particularly from ESD, increases (see Figure 1).

Increasing complexity of devices, and component density on PCBs leads to increased probability of interaction between adjacent circuits, including propagation of ESD events.

Due to these reasons ESD protection becomes more and more important with technology advance. At the same time it gets more challenging. Due to reducing voltage margins new generation protection devices must provide lower clamping voltage and dynamic resistance, as well as lower overshoot. Moreover, growing data rates and increasing operating frequencies lead to the requirement of reduced parasitic parameters.

Another effect of current trends is growing demand for smaller packages. Currently common 0201-size package is gradually replaced by 01005-size. However, for plastic packages like TS(S)LP this size is unreachable.

Chip scale package (CSP) package provides good solution of mentioned problems.

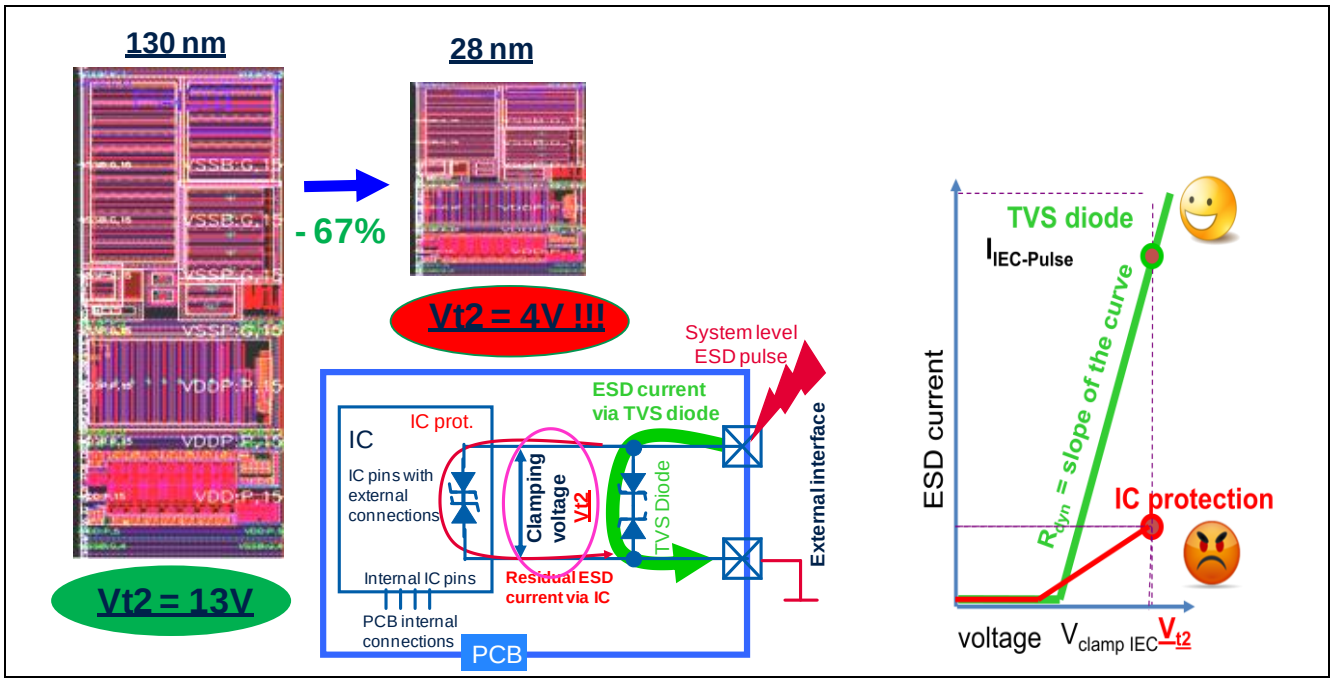


Figure 1 Miniaturization influence on ESD protection requirements

2 Overview

Infineon's Chip Scale Packages are called Silicon Green - Wafer Level Leadless (SG-WLL). SG-WLL are bare silicon packages for discrete components. They are especially appropriate for applications with limited space on the board. For package board interconnection, the packages have a NiP – Pd - Au (Nickel-Phosphorus Palladium Gold) surface on the package pads. The remaining surface is passivated by silicon nitride.

Figure 2 CSP/SG-WLL Package

2.1 CSP/SG-WLL Package Features

- Reduced cost compared to plastic package
- Smallest x-y-z-package dimensions
- No package internal interconnect (e.g. wire bond or flip chip connection) – lower inductance
- Chip size (silicon)-package without redistribution layer
- Lead free package
- Lowest moisture sensitivity (MSL1) due to bare silicon product

3 Low Clamping Voltage TVS Diodes in a thin 0201/01005 package

3.1 Family overview

Infineon low clamping voltage TVS diodes usually have part numbers starting with ESD2xx. Let us focus on devices with working voltage up to around ±5V in Chip Scale Package:

- ESD200-B1-CSP0201
- ESD202-B1-CSP01005

Both devices have almost identical features and differ mainly in package size, 0201 vs. 01005. For comparison, device with similar features in plastic package (TSSLP-2-3) is shown:

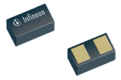
- ESD205-B1-02ELS

3.2 Key Applications

- Keypad, touchpad, buttons, convenience keys
- LCD displays, camera, audio lines in mobile communication, consumer products (E-Books, MP3-, DVD-Players, etc)
- Notebooks, tablets and desktop computers and their peripherals

3.3 Feature Comparison

Table 1 Features and electrical characteristics of ESD200-B1-CSP0201/ ESD202-B1-CSP01005/ ESD205-B1-02ELS

Feature	ESD205-B1-02ELS	ESD200-B1-CSP0201	ESD202-B1-CSP01005
Package	**TSSLP-2-3** (0201 plastic) 	**WLL-2-1** (0201 CSP) 	**WLL-2-2** (01005 CSP) 
Package dimensions	0.62 x 0.32 mm²	0.58 x 0.28 mm²	0.43 x 0.23 mm²
Package thickness	0.31 mm	0.15 mm	0.15 mm
Maximum working voltage	V_{RWM} = ±5.5 V	V_{RWM} = ±5.5 V	V_{RWM} = ±5.5 V
ESD protection of signal lines according to **IEC61000-4-2**	**±20 kV** (air/contact)	**±16 kV** (air/contact)	**±16 kV** (air/contact)
Surge protection of signal lines according to **IEC61000-4-5**	**±2.5 A (8/20 µs)**	**±3 A (8/20 µs)**	**±3 A (8/20 µs)**
Line capacitance	C_L = 5 pF (typical) [1)]	C_L = 6.5 pF (typical)[1)]	C_L = 6.5 pF (typical)[1)]
Series inductance	L_S = 200 pH (typical)[1)]	L_S < 50 pH	L_S < 50 pH
Reverse current	I_R < 1 nA (typical)	I_R = 0.1 nA (typical)	I_R = 0.1 nA (typical)
Dynamic resistance	$R_{DYN} \leq 0.2/0.3\ \Omega$ (typical, forward/reverse)	$R_{DYN} \leq 0.2\ \Omega$ (typical)	$R_{DYN} \leq 0.2\ \Omega$ (typical)
I/V characteristics symmetry	Good	Very high	Very high
Initial overshoot	Low	Very low	Extremely low
Pb-free package (RoHS compliant)	RoHS HAL	RoHS HAL	RoHS HAL

1) at f = 1 MHz

3.4 Description

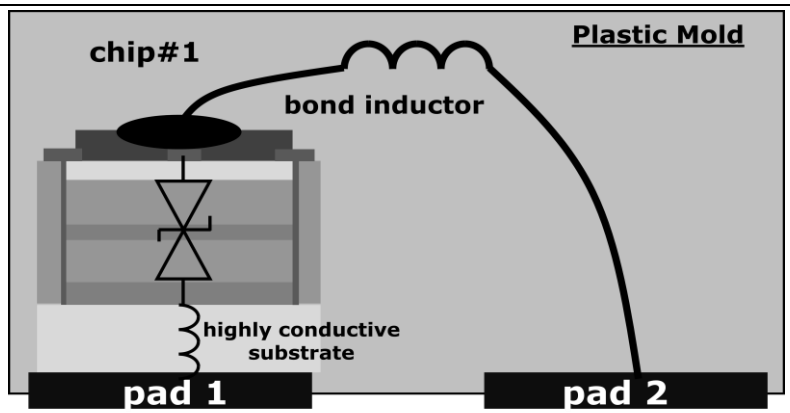


Figure 3 Internal structure of ESD205-B1-02Series in plastic package (vertical ESD diode design)

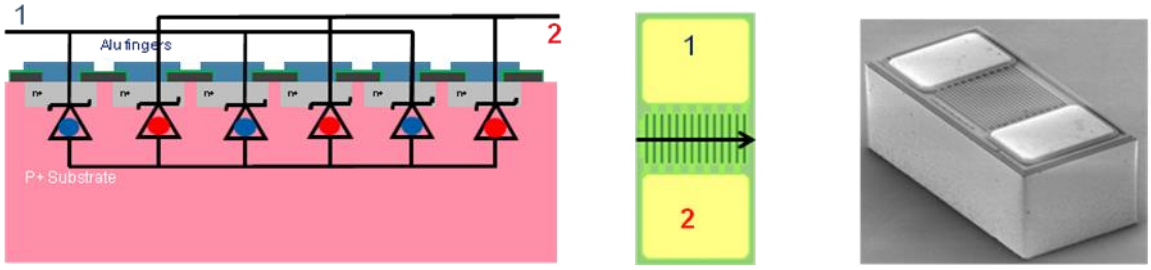


Figure 4 Internal structure of ESD200-B1-CSP0201 / ESD202-B1-CSP01005 (lateral ESD diode design)

ESD200-B1-CSP0201, ESD202-B1-CSP01005 and ESD205-B1-Series are devices designed for applications requiring low clamping voltage. They have comparable main features, like line capacitance and protection level. However, due to technological difference in chip and package design each of them provide different advantages.

ESD205-B1-02Series in plastic package has **highest ESD protection level**, making it perfect for applications where 16-20kV according to IEC61000-4-2 is required. Moreover, there is **bigger version** of the device (ESD205-B1-02LS) in 0402 package if PCB technology cannot handle smaller 0201 (ESD205-B1-02ELS) part. Internal structure of ESD205-B1-Series can be seen in Figure 3.

ESD200-B1-CSP0201 structure is shown in Figure 4. This device is realized in Chip Scale Package (CSP) technology. An advanced technology with performance-optimized chip structure and without bond wires guarantees **very low series inductivity** of the device. In turn, the **initial overshoot is drastically reduced** (compare Figure 5 and Figure 6).

ESD202-B1-CSP01005 is internally similar to ESD200-B1-CSP0201 and is the **next step of miniaturization**. It offers you reliable ESD protection in the smallest package possible – size **01005**. Furthermore the package shrink to 01005 reduces the electrical length between input and output node. This leads to further reduction in series inductivity and initial overshoot.

Another advantage of devices in chip-scale packages is **reduced cost** due to simplified packaging procedure.

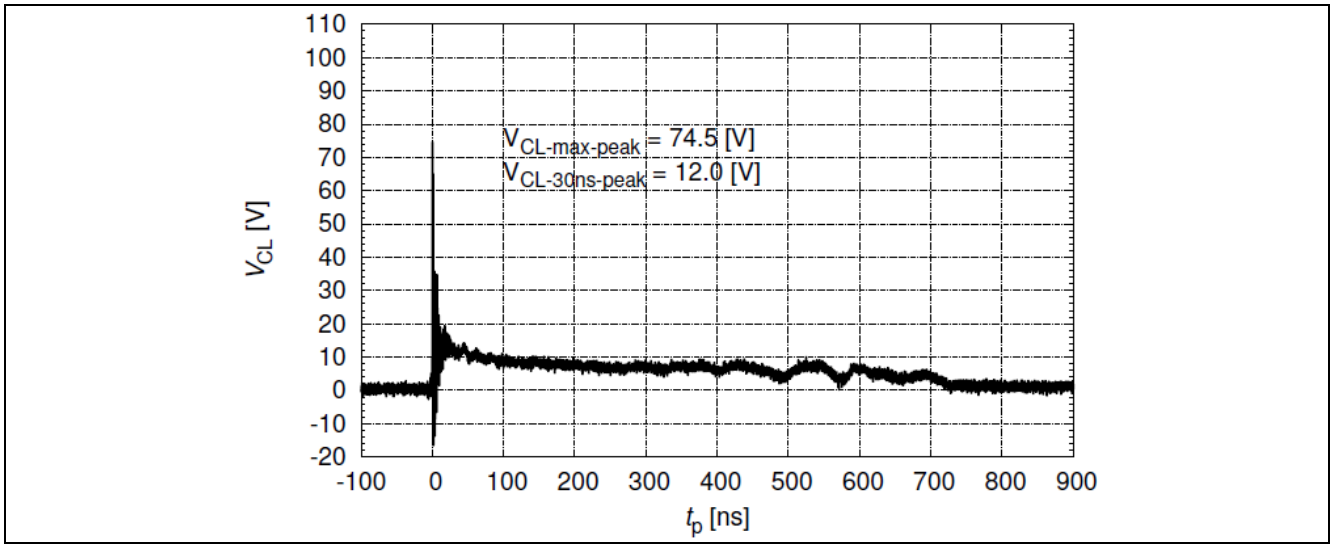


Figure 5 ESD205-B1-02ELS voltage response to 15 kV ESD strike according to IEC61000-4-2

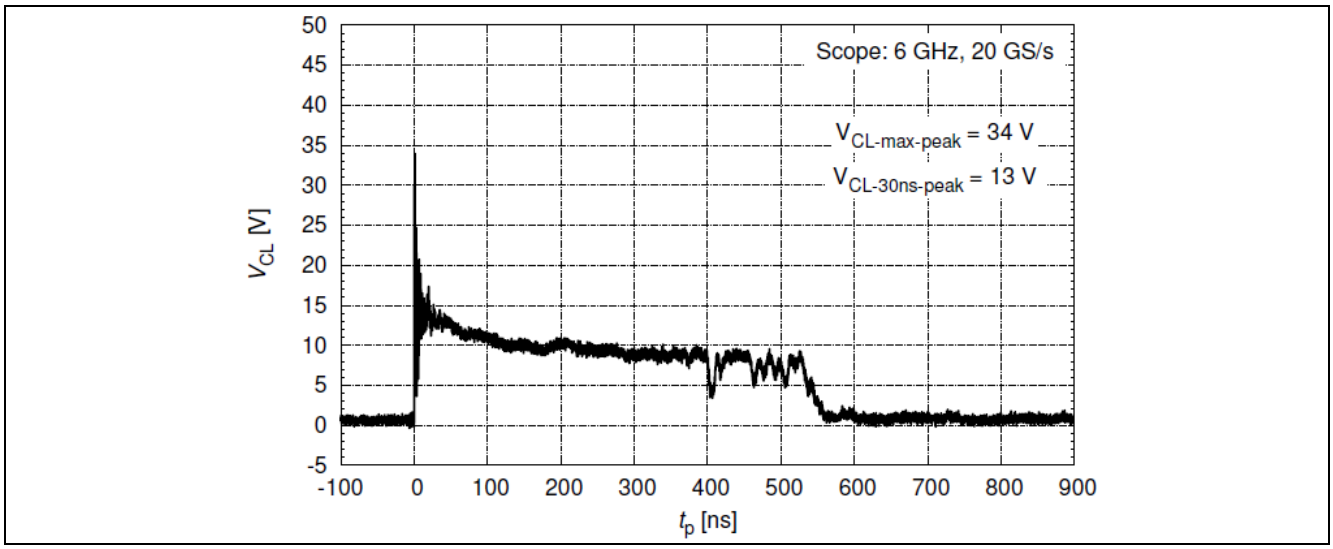


Figure 6 ESD200-B1-CSP0201 voltage response to 15 kV ESD strike according to IEC61000-4-2

4 Ultra Low Capacitance TVS Diodes for High-Speed Interfaces

4.1 Family overview

Infineon ultra-low capacitance TVS diodes usually have part numbers starting with ESD1xx. Let us focus on devices with working voltage up to around ±5V in Chip Scale Package:

- ESD108-B1-CSP0201
- ESD119-B1-W01005

Both devices have almost identical features and differ mainly in package size, 0201 vs 01005. For comparison, device with similar features in plastic package (TSSLP-2-3) is shown:

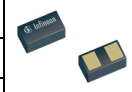
- ESD112-B1-02ELS

4.2 Key Applications

- High-speed digital interfaces: USB 3.0, Firewire, DVI, HDMI, S-ATA, DisplayPort, Thunderbolt
- Mobile Devices: Mobile HDMI Link, MDDI, MIPI, SWP / NFC
- RF antenna protection, frontend module, GPS, mobile TV, FM radio, UWB

4.3 Feature Comparison

Table 2 Features and electrical characteristics of ESD108-B1-CSP0201/ ESD112-B1-02ELS

Feature	ESD112-B1-02ELS		ESD108-B1-CSP0201		ESD119-B1-W01005	
Package	**TSSLP-2-3** (0201 plastic)		**WLL-2-1** (0201 CSP)		**WLL-2-2** (01005 CSP)	
Package dimensions	0.62 x 0.32 mm²		0.58 x 0.28 mm²		0.43 x 0.23 mm²	
Package thickness	0.31 mm		0.15 mm		0.15 mm	
Maximum working voltage	V_{RWM} **= ±5.3 V**		V_{RWM} **= ±5.5 V**		V_{RWM} **= ±5.5 V**	
ESD protection of signal lines according to **IEC61000-4-2**	**±20 kV** (air/contact)		**±25 kV** (air/contact)		**±25 kV** (air/contact)	
Surge protection of signal lines according to **IEC61000-4-5**	**±3 A (8/20 µs)**		**±2.5 A (8/20 µs)**		**±2.5 A (8/20 µs)**	
Line capacitance	C_L **= 0.23 pF** (typical)[1)]		C_L **= 0.28 pF** (typical)[1)]		C_L **= 0.28 pF** (typical)[1)]	
Series inductance	L_S **< 200 pH**		L_S **< 150 pH**		L_S **< 100 pH**	
Reverse current	I_R **< 1nA** (typical)		I_R **= 0.1 nA** (typical)		I_R **= 0.1 nA** (typical)	
Dynamic resistance	R_{DYN} **= 1 Ω** (typical)		R_{DYN} **= 0.78 Ω** (typical)		R_{DYN} **= 0.78 Ω** (typical)	
Initial overshoot	Low		Very low		Extremely low	
Pb-free package (RoHS compliant)	RoHS HAL		RoHS HAL		RoHS HAL	

1) at f = 1 MHz

4.4 Description

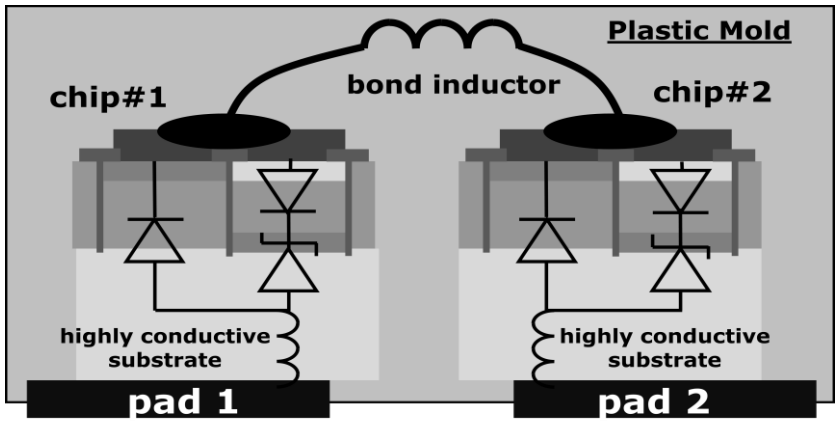


Figure 7 Internal structure of ESD112-B1-02Series

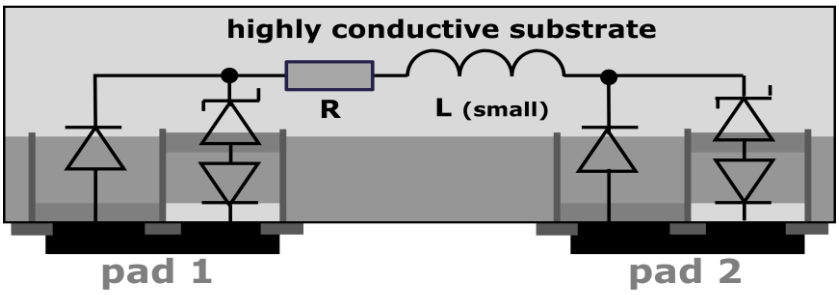


Figure 8 Internal structure of ESD108-B1-CSP0201 / ESD119-B1-W01005

ESD108-B1-CSP0201, ESD112-B1-02Series and ESD119-B1-W01005 are all designed for applications sensitive to parasitic parameters, such as high-speed interfaces. They have comparable key parameters, like line capacitance and protection level. However, due to technological difference in chip and package design each of them provide different advantages.

ESD112-B1-02Series in plastic package has slightly lower capacitance then other devices. Also, there is a **bigger version** of the device (ESD112-B1-02EL) in 0402 package if PCB technology cannot handle smaller 0201 (ESD205-B1-02ELS) part. Internal structure of ESD112-B1-02Series can be seen in Figure 7.

ESD108-B1-CSP0201 structure is shown in Figure 8. This device in Chip Scale Package provides big advantage of **cost saving**. Also, advanced technology with performance-optimized chip structure and without bond wires guarantees **minimal series inductivity** of the device.

ESD119-B1-W01005 is internally similar to ESD108-B1-CSP0201 and is **next step of miniaturization**. It offers you reliable ESD protection in the smallest package possible – size **01005**. Additionally, package shrinking leads to further reduction in series inductivity.

5 Handling Information

Infineon's Silicon Green - Wafer Level Leadless (SG-WLL) packages designed to be direct drop-in replacement for plastic TSSLP package. Special care was taken to make the devices compatible with commonly used assembly processes. The PCB footprint recommendations are included in product data sheets. We highly recommend following these PCB footprint recommendations to get best assembling reliability.

This section is only meant to highlight key aspects of CSP handling. For detailed information on Board Assembly of Infineon SG-WLL Packages please refer to [1].

5.1 PCB Pad Design

Generally we recommend Non-Solder Mask Defined (NSMD) pad design for SG-WLL packages.

- Chip-Scale packages and its pads are very small and require precise PCB pad manufacturing. NSMD pad design eliminates the influence of solder mask manufacturing tolerances on resulting PCB pad size
- On the other hand, NSMD design opens parts of the lines connecting the pads to the remaining circuit. The reason is the solder-mask opening being bigger than the pad itself. To minimize the influence of the solder paste wetting these open parts of the lines during reflow soldering, the width of the connecting lines on the PCB should be as small as possible (100 µm or less). Connection lines have to be placed correctly to avoid any de-adjustment between PCB footprint and device during soldering process.

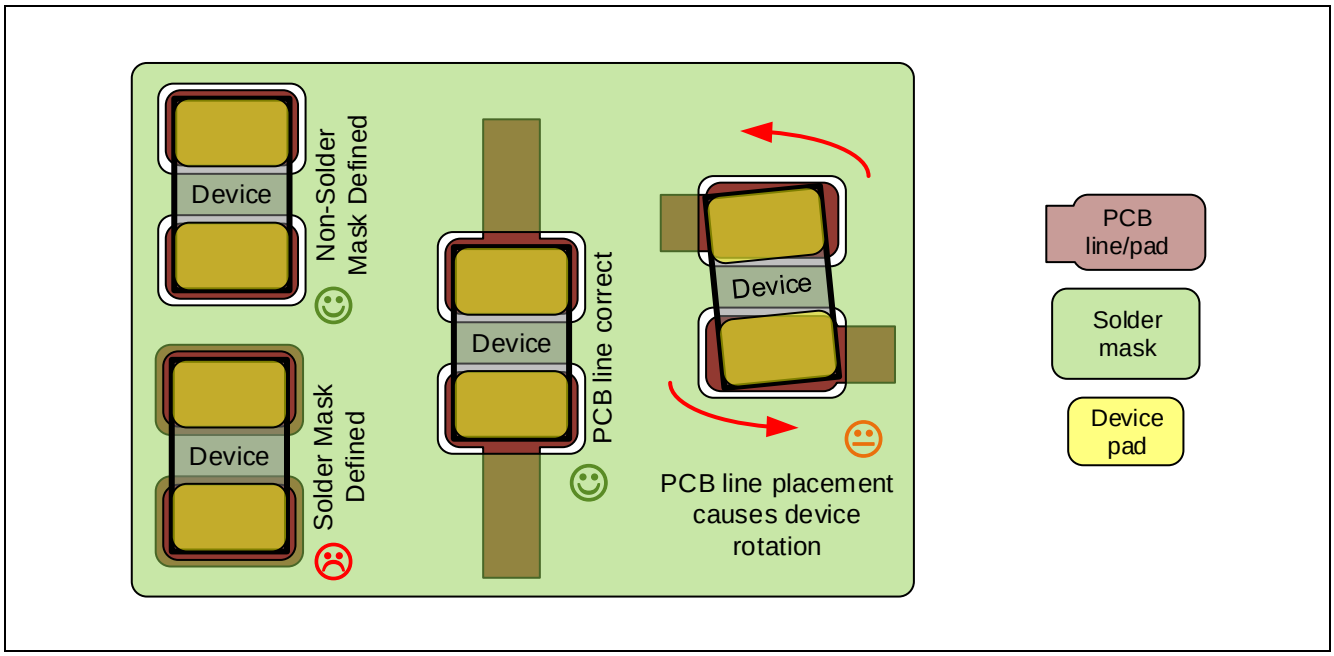


Figure 9 NSMD layout with and without correct PCB line placement

- Depending on the capabilities of the PCB manufacturer, it might not be possible to separate two PCB pads of one SG-WLL package by a solder mask dam. Providing that the stencil openings for the solder paste printing process are suitably designed and the printing process itself is well-controlled, the missing solder mask dam between the pads may not be critical. Experiments have shown that it is helpful to increase the PCB pad size slightly compared to the package pads.

In general the PCB pad oversize respective to the device pad must be minimized for leadless TSSLP and CSP devices. The solder area is restricted to the pads below the device. Too big pads might lead to undesirable wetting of device side walls, leading to performance deterioration. We strongly discourage from using the same pad size for leadless TSSLP/CSP packages and for devices with side wall terminal metallization (e.g. capacitors, varistors, resistors).

5.2 Solder Paste

A “no-clean” solder paste is preferred for SG-WLL packages since the solder joints will be formed below the components, where cleaning will be difficult or impossible.

The paste must be suitable for printing the solder stencil aperture dimensions; the usage of paste type 4 or a higher type (with lower grain size of the solder alloy powder) is recommended. The paste with ROL0 flux is preferred.

5.3 Solder Stencil

To ensure a uniform and sufficiently high solder-paste transfer to the PCB, laser-cut stencils (mostly made from stainless steel) with coating for improved solder paste release (nano-coating) are preferred. A maximum recommended stencil thickness is 100 µm for devices in 0201-size, and 80 µm for 01005-size.

5.4 Rework

If a rework (component replacement) is planned, you need to take into account that the devices are very small and that package material is silicon itself. The equipment used should be suitable for the smallest package sizes and for handling bare silicon devices (e.g. no metal tweezers used, etc).

6 References

[1] Infineon AG - Recommendations for Printed Circuit Board Assembly of Infineon WLL Packages

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