Application Note No. 178

ESD Protection for RF Antennas using Infineon ESD112-B1-02ELS and ESD112-B1-02EL

RF and Protection Devices

Edition 2014-05-27

Published by
Infineon Technologies AG
81726 München, Germany

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Application Note No. 178

Revision History: 2014-05-27, Rev. 1.1

Previous Version: 2008-12-05, Rev. 1.0

Page	Subjects (major changes since last revision)
All	Update to new sales codes

1 Introduction

This application note deals with the applicability of Infineon's low capacitance (≤ 0.4 pF) ESD protection diodes for RF antenna protection. The first one, ESD0P4RFL—an anti-parallel ESD protection diode—exhibits a noise figure as low as 0.1 dB at 3 GHz and is suitable for use as ESD protection before the LNA (low noise amplifier). The second one, ESD112-B1—a bidirectional ESD protection diode—exhibits a capacitance as low as 0.2 pF and can handle voltages of up to ±5.3 V, which makes it suitable to protect RF interfaces for active antennas as well. ESD0P4RFL comes in the TSLP-4-7 (thin small leadless package) with dimensions of 1.2 mm x 0.8 mm x 0.39 mm (EIA case size 0503) and ESD112-B1 is available in TSSLP-2-4 (thin super small leadless package) with dimensions of 0.62 mm x 0.32 mm x 0.31 mm (EIA case size 0201) as well as in TSLP-2-20 with dimensions of 1.0 mm x 0.6 mm x 0.39 mm (EIA case size 0402).

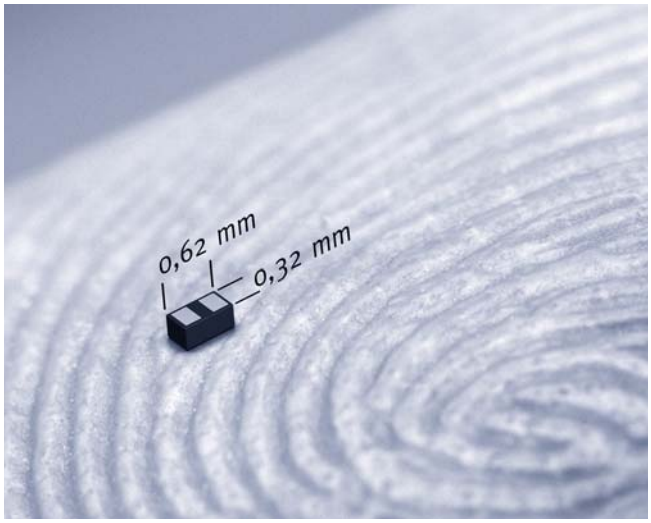

Figure 1 Infineon's Thin Super Small Leadless Package TSSLP-2-4

ESD0P4RFL

The anti-parallel ESD protection diode ESD0P4RFL was designed to protect RF receiver interfaces from ESD events. With a typical capacitance of 0.4 pF at a frequency of 1 GHz it features both lowest noise figure and lowest clamping voltage.

ESD112-B1-02ELS / -02EL

The bidirectional ESD protection diode ESD112-B1 is very much suitable for ultra wide band applications or active RF antennas operating at voltages of up to ±5.3 V at leakage currents of less than 10 nA. With a typical capacitance of 0.2 pF at 1 GHz it features lowest insertion loss and low clamping voltage.

2 Overview

S-parameters of packaged diodes were measured with wafer probes in order to avoid the error-prone procedure of de-embedding S-parameters from a printed circuit board (PCB). However, for evaluation purposes a FR-4 eval board is provided by Infineon (see **Figure 2**). Please note that the S-parameters provided by Infineon do not include any PCB and SMA connector losses.

First of all some ESD protection concepts for RF antennas and their differences are discussed. Next, the capacitance of Infineon's ESD protection diodes versus frequency and voltage is shown. This is followed by a discussion of basic RF parameters: insertion loss, return loss, noise figure and bandwidth. Since silicon diodes are nonlinear devices, harmonic generation is considered as well. The reason why the analog bandwidth of the scope is crucial for clamping voltage measurements is pointed out and clamping voltage, peak voltage and response time of Infineon's ESD protection diodes are presented. But most important, an application example, layout guidelines and guidelines on how ESD hardness can be further enhanced are shown as well. Finally, other solutions available on the market are discussed briefly.

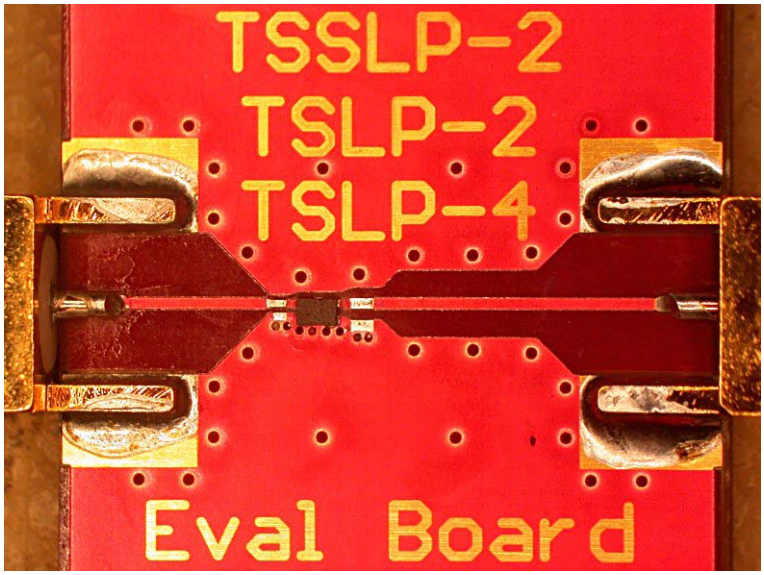

Figure 2 Photo of Infineon eval board for T(S)SLP (here with an ESD0P4RFL in TSLP-4-7)

3 ESD Protection Concepts

In order to use silicon diodes for RF interfaces in the gigahertz range, one important key feature has to be the low parasitic capacitance of the diode. PIN diodes with its lightly doped intrinsic semiconductor region between the p-type and n-type region make capacitances of only a few tenths of a picofarad possible. However, the charge carrier life time of general purpose PIN diodes is in the microsecond range and therefore these diodes are far too slow for ESD events, for which carrier life times in the region of 1 nanosecond are a must-have. To overcome this behavior of general purpose PIN diodes, Infineon developed fast switching, low-capacitive diodes suitable for ESD protection. Unlike Zener diodes, these low-cap diodes must not be operated beyond their breakdown voltage and even an ESD event in reverse biased condition permanently damages the diode. Thus, for ESD protection always a pair of low-cap diodes is required, each one for either polarity of an ESD event, so that the current arising from the ESD event is always conducted in forward direction by either diode. **Figure 3** shows three different configurations, each with a pair (or two pairs) of fast switching, low-capacitive diodes. In the anti-parallel configuration either diode operates in forward biased condition, and thus the voltage on the signal line must be approximately between -0.3V and +0.3V. This is equivalent to 0dBm at an impedance of 50Ω. Infineon's ESD0P4RFL with a line capacitance of 0.4pF (this is the total parasitic capacitance) integrates two low-cap diodes in anti-parallel configuration into one package. For all measurements presented herein ESD0P4RFL was configured in the anti-parallel way.

There are two possibilities to overcome this limitation on the voltage. The first one is to use an additional Zener-like diode as shown in **Figure 3 (b)**. Since the Zener-like diode is in series with the low-cap diodes, the much higher capacitance of the Zener-like diode does not count to the line capacitance. By using two pairs of low-cap diodes in series, the line capacitance of the ESD protection diode is only half the capacitance of an anti-parallel configuration. Such a bidirectional ESD protection diode can handle voltages between $-V_{RWM}$ and $+V_{RWM}$ (V_{RWM} is the maximum reverse working voltage) on the signal line. Infineon's ESD protection diode ESD112-B1 with a line capacitance of 0.2pF and a reverse working voltage of 5.3V max integrates this configuration into an incredible small package (EIA 0201 case size).

The third option shown in **Figure 3 (c)** is the rail-to-rail configuration where the low-cap diodes are not connected to ground like for the anti-parallel configuration but to V_{EE} and V_{CC} instead (but often V_{EE} is equivalent to ground). Such a configuration can handle any voltage between V_{EE} - 0.3V and V_{CC} + 0.3V on the signal line. However, the

current arising from ESD events must be conducted to chassis ground and thus either big-sized capacitors or unidirectional ESD protection diodes are needed for the V_{EE} and V_{CC} rail, which are not shown here. (Of course, in case the V_{EE} rail is equivalent to ground, this is only needed for the V_{CC} rail.) Infineon's ESD0P4RFL can also be used in rail-to-rail configuration as shown in **Figure 3**.

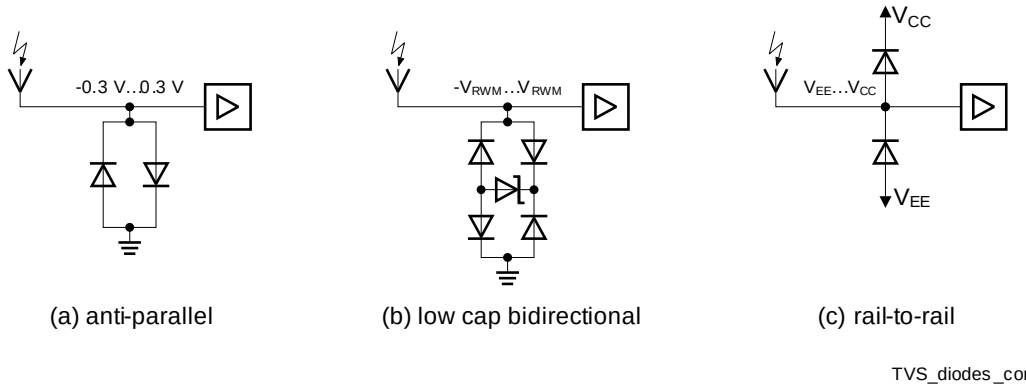

Figure 3 Three different concepts for ESD protection diodes: (a) two low-cap diodes in anti-parallel configuration, (b) combination of four low-cap diodes and one Zener-like diode to a bidirectional configuration and (c) two low-cap diodes in rail-to-rail configuration

4 Capacitance

The capacitance of silicon diodes is generally voltage- and frequency-dependent. **Figure 5** shows the apparent capacitance of ESD0P4RFL in anti-parallel configuration and of ESD112-B1 for a working voltage V_R = 0V. The apparent capacitance shown in **Figure 5** and **Figure 6** is the capacitance of an equivalent, frequency dependent parallel RC circuit as shown in **Figure 4**. Usually, capacitance reduces with frequency and working voltage, but at higher frequencies the inductance of the bond wire—0.2nH for ESD0P4RFL and ESD112-B1-02ELS and 0.4nH for ESD112-B1-02EL—apparently increases the capacitance of the diode. **Figure 6** shows the apparent capacitance of ESD112-B1-02ELS versus working voltage between 0V and 5V. Since the junction capacitance is only about half the total line capacitance, the apparent capacitance shows only little dependence on the working voltage, typically only about 3% change in capacitance up to 5V. This is also true for ESD0P4RFL in rail-to-rail configuration, but unlike ESD112-B1, it offers a maximum reverse working voltage as high as 50V. See **Figure 7** for a plot of the apparent capacitance of ESD0P4RFL in rail-to-rail configuration with the reverse working voltage applied to either diode.

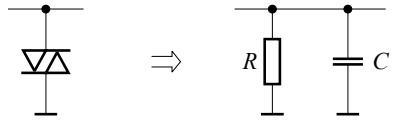

Figure 4 Equivalent parallel RC circuit

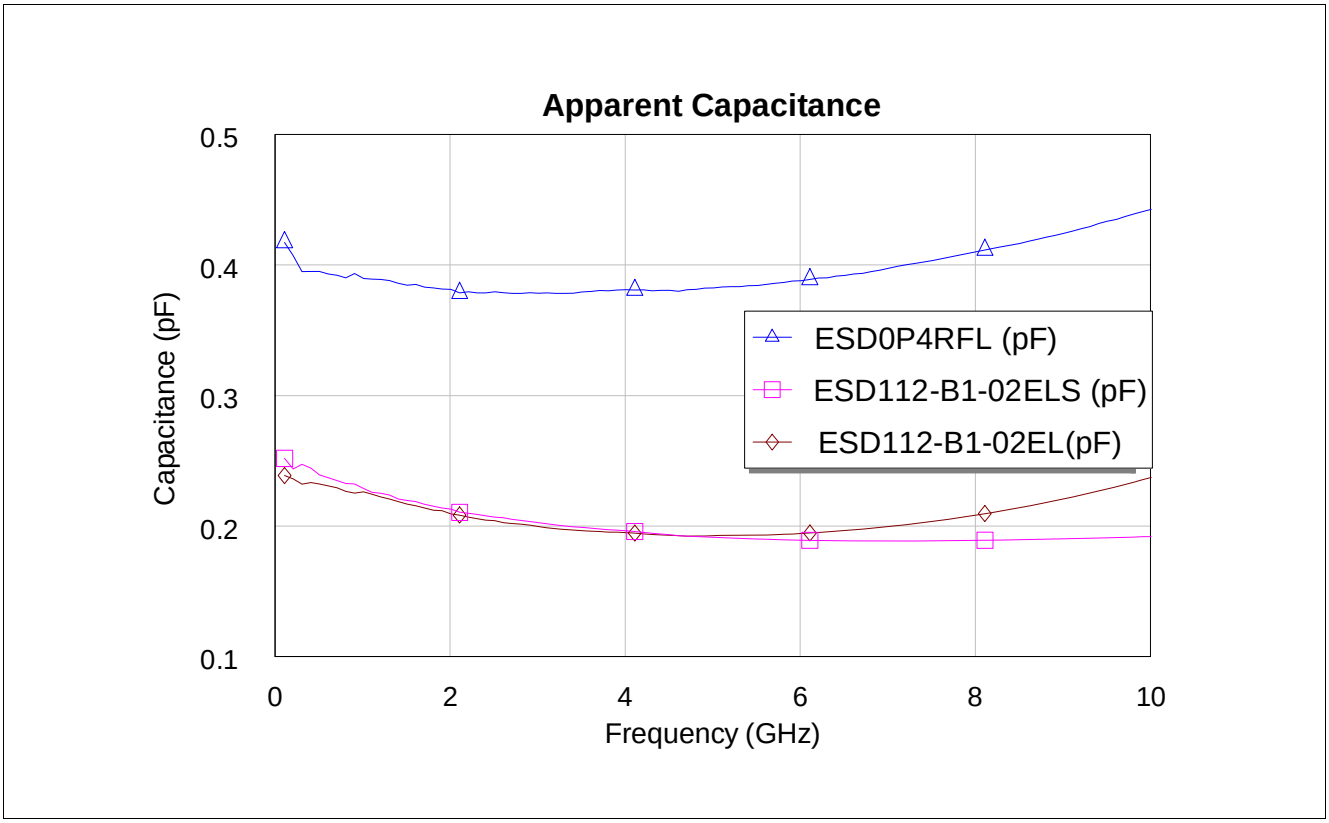

Figure 5 Apparent parallel capacitance of ESD0P4RFL and ESD112-B1

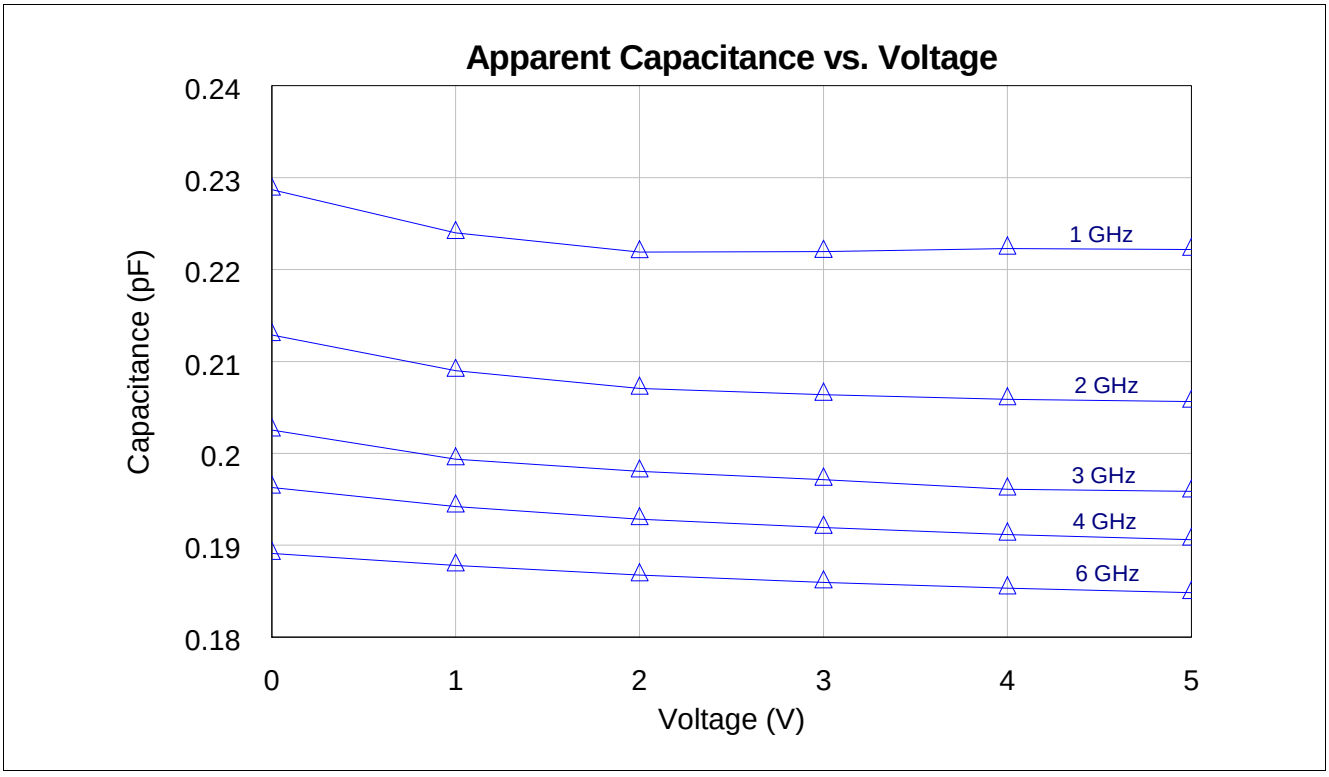

Figure 6 Apparent parallel capacitance of ESD112-B1-02ELS vs. working voltage

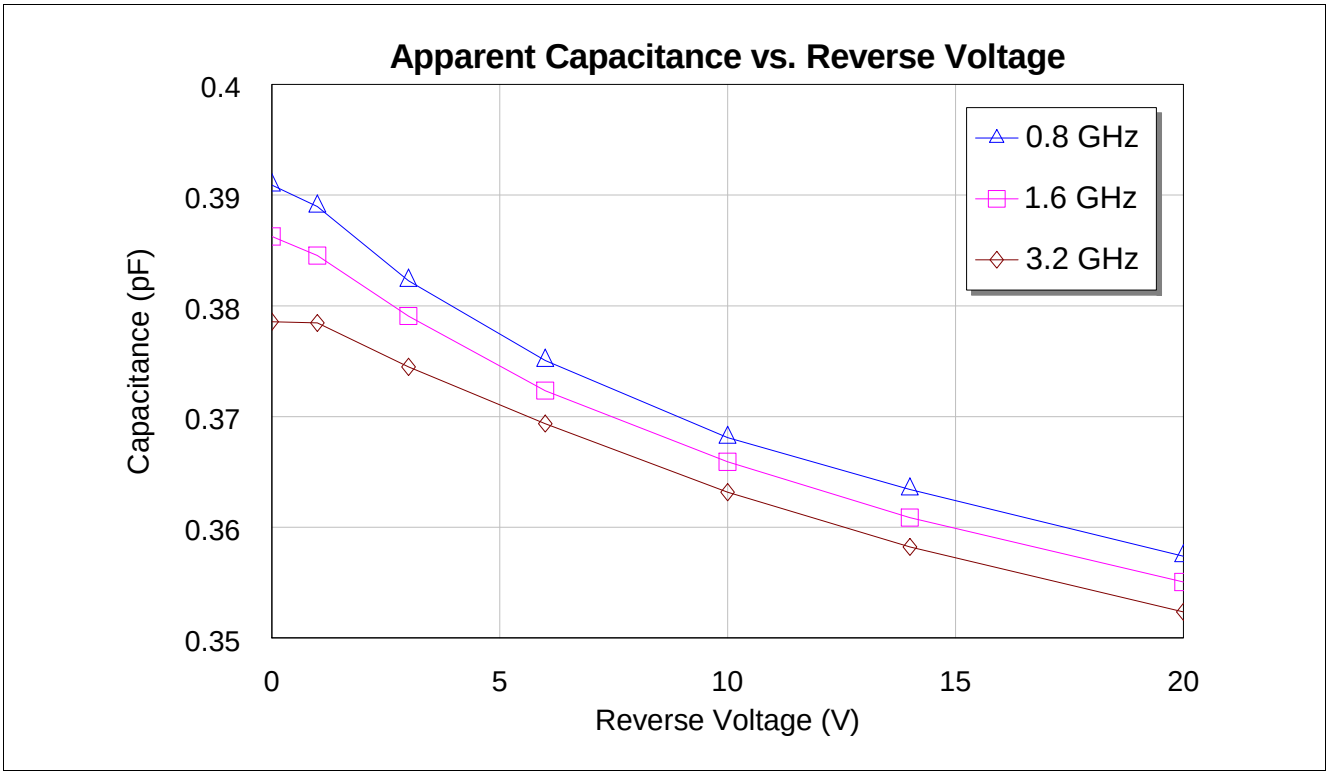

Figure 7 Apparent parallel capacitance of ESD0P4RFL in rail-to-rail configuration vs. reverse working voltage

5 Insertion Loss and Return Loss

Insertion loss, IL, and return loss, RL, are two key characteristics for RF applications that are mainly determined by the capacitance of the ESD protection diode and are calculated from the S-parameters as follows:

$$IL = -20\log|S_{21}| \quad (1)$$

and

$$RL = -20\log|S_{11}|, \quad (2)$$

whereas IL and RL are expressed in decibel (dB). **Figure 8** and **Figure 9** show insertion loss and return loss respectively of ESD0P4RFL in anti-parallel configuration and of ESD0P2RF for a reverse working voltage of V_R = 0V. Up to 3GHz insertion loss does not show a significant difference between these ESD protection diodes. Due to the higher bond wire inductance of the bigger package, insertion loss of ESD112-B1-02EL is greater than that of ESD112-B1-02ELS.

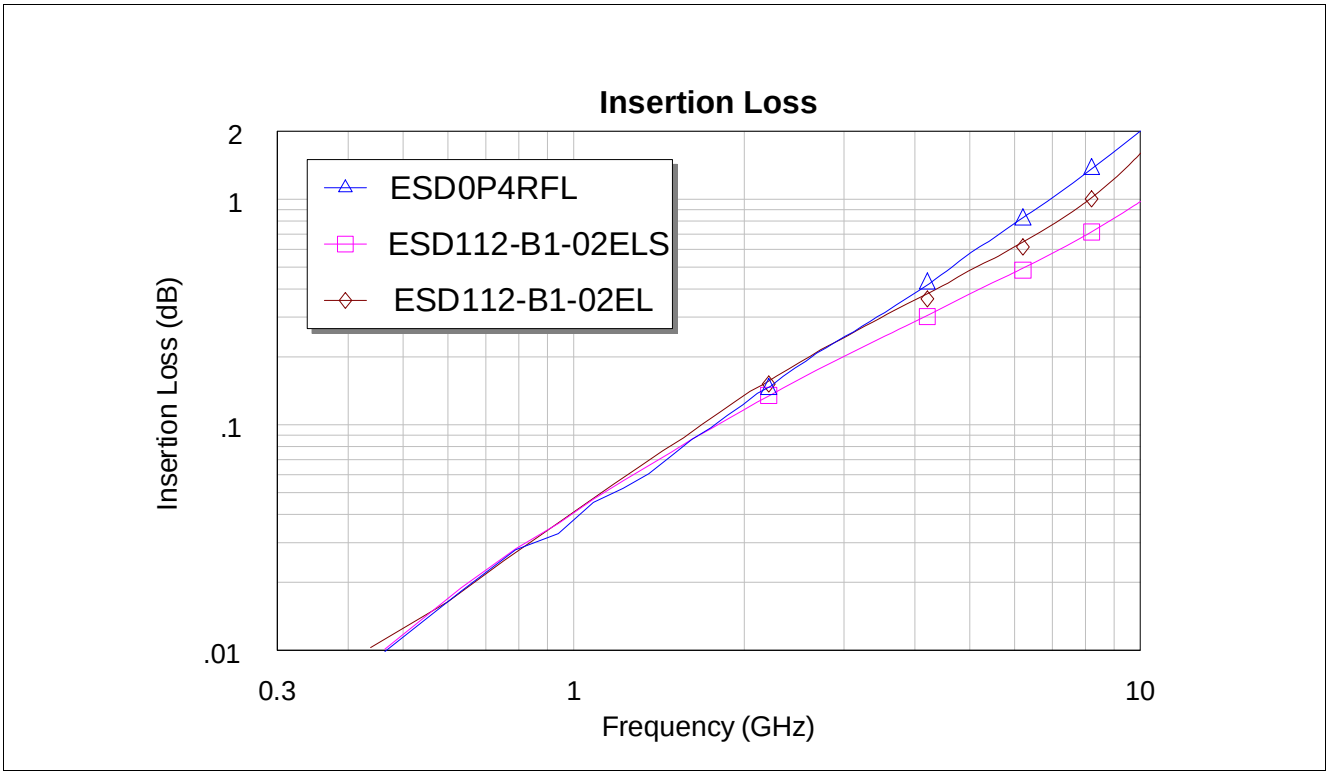

Figure 8 Insertion loss of ESD0P4RFL and ESD112-B1

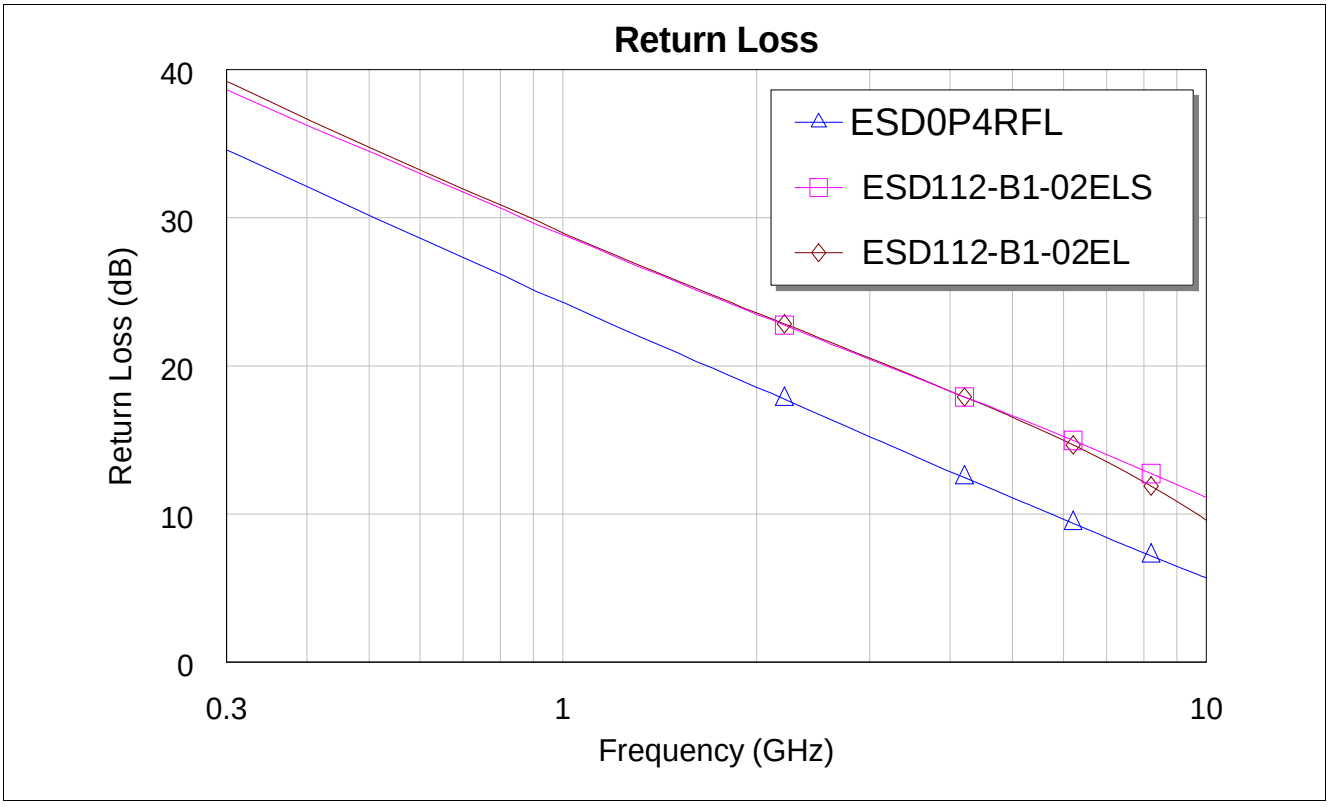

Figure 9 Return loss of ESD0P4RFL and ESD112-B1

6 Noise Figure

Noise figure, NF, expressed in dB, of a passive, lossy two-port circuit at room temperature ($T \cong 290\,\mathrm{K}$) is given as

$$NF|_{\mathrm{dB}} \cong -G_{\mathrm{A}}|_{\mathrm{dB}} = IL|_{\mathrm{dB}} - ML|_{\mathrm{dB}}\,, \tag{3}$$

where G_{A} is the available gain of the passive two-port circuit, IL is the insertion loss and ML is the mismatch loss, all expressed in dB. Since the uncertainty of the Y-factor method which is used by noise figure analyzers to measure noise figures increases to infinity at zero noise figure and zero gain, a noise figure analyzer can not be used to measure noise figures of low-loss passive circuits. However, according to **Equation (3)** the noise figure of a passive circuit can be calculated from the S-parameters measured at room temperature. For more details on this please see **“Appendix” on Page 25**.

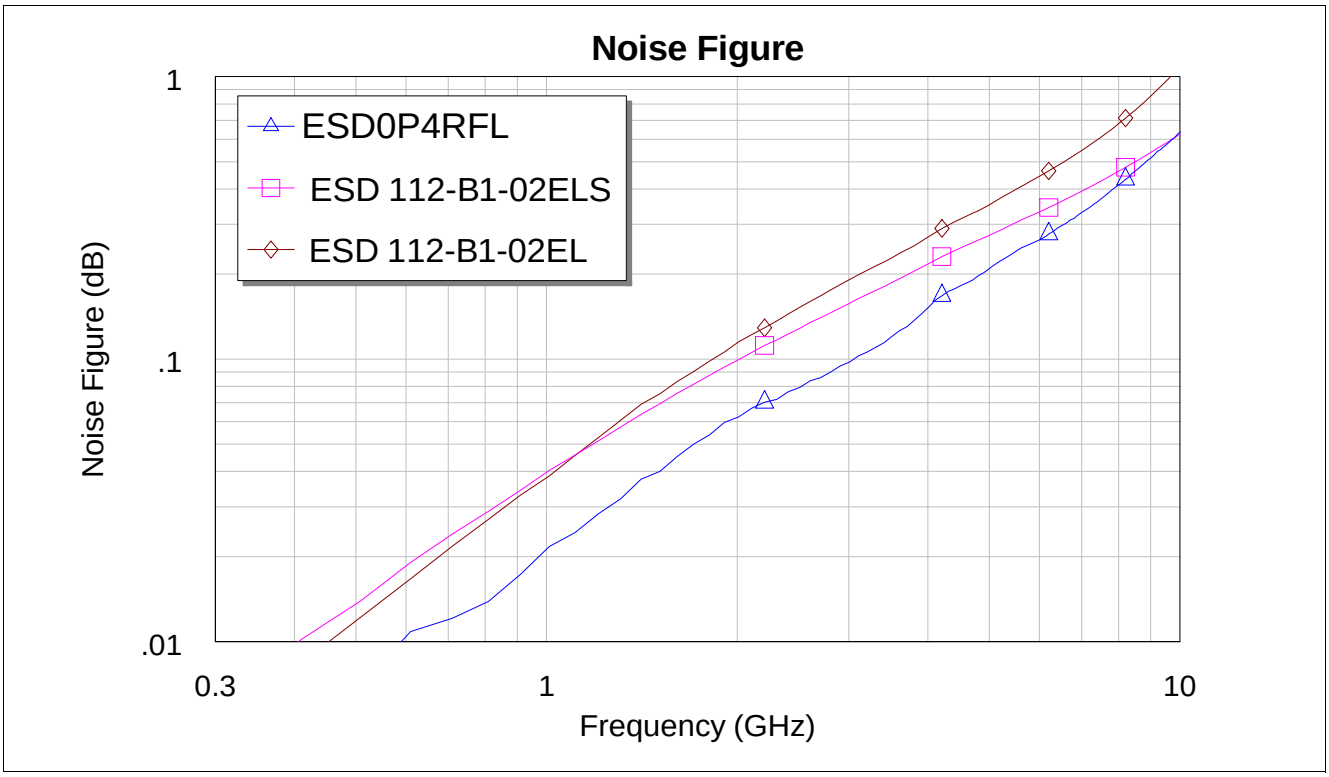

Figure 10 Noise figure of ESD0P4RFL and ESD112-B1

7 Bandwidth

Figure 11 shows a wide-span plot of the transmission coefficient S_{21}, from which the 3dB bandwidth can be read off. With a 3dB bandwidth of approximately 18GHz, ESD112-B1-02ELS is very much suitable, for example, for ESD protection of ultra-wide band applications. ESD112-B1-02EL has twice the bond wire inductance (due to the bigger package) and ESD0P4RFL has twice the capacitance of ESD112-B1-02ELS, and thus the 3dB bandwidth of both ESD0P4RFL and ESD112-B1-02EL is approximately 12GHz.

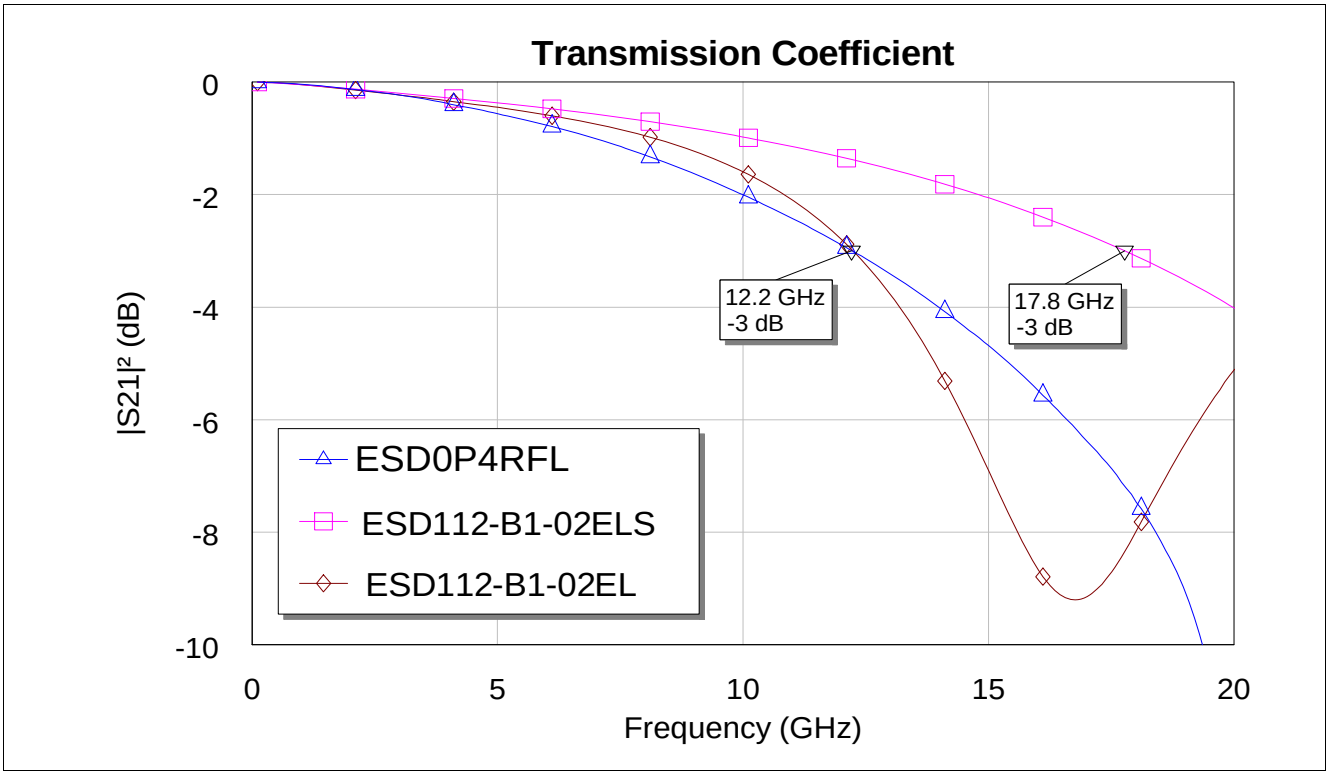

Figure 11 3dB bandwidth of ESD0P4RFL and ESD112-B1

8 Harmonic Generation

The frequency of the fundamental tone for the measurement of the 2nd and 3rd harmonic was 900MHz and the power level was swept from -10dBm to 19dBm (see **Figure 12** for test setup). Thus, the 2nd harmonic was measured at 1.8GHz and the 3rd harmonic was measured at 2.7GHz. In the small signal region, that is for power levels less than 0dBm, the intercept point characterizes the nonlinear behavior of the diode. The 2nd order intercept point, IP_2, and the 3rd order intercept point, IP_3, are given by

$$IP_2 = P_{H1} + (P_{H1} - P_{H2}) \text{ and} \tag{4}$$

$$IP_3 = P_{H1} + \frac{P_{H1} - P_{H3}}{2}, \tag{5}$$

where P_{H1} is the power level of the fundamental tone, and P_{H2} and P_{H3} are the power levels of the 2nd and 3rd harmonics respectively. All power levels are in dBm. See **Table 1** for the small signal IP_2 and IP_3 values.

Please note that these values are only valid in a wide-band 50Ω environment, which is usually not the case for real-world applications. In order to minimize intermodulation products from strong interfering out-of-band signals, the out-of-band impedance seen by the interfering signal at the ESD protection diode should be low. By this means, the voltage drop across the diode is also low and thus the junction capacitance of the diode is less modulated by the interfering signal. In the case of strong interfering signals there is often a filter following the ESD protection diode. The intermodulation products generated by the ESD protection diode are then affected by tuning the out-of-band impedance of this filter. If the out-of-band impedance of the filter itself cannot be adjusted, the same effect is achieved, at least for interfering signals at high frequencies, by tuning the length of the transmission line between antenna, ESD protection diode and filter. In principle, also the out-of-band impedance of the antenna rather than the filter can be tuned. For example, a loop antenna can be designed such that it provides a short at the E-field maxima of the interfering signal.

Table 1 Harmonic generation in the small signal region
T_A = 25 °C, f_{H1} = 900 MHz, P_{H1} = -10 dBm, Z_S = Z_L = 50 Ω

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ESD0P4RFL						
2nd order intercept point	IP_2		100		dBm	f_{H2} = 1.8 GHz
3rd order intercept point	IP_3		34		dBm	f_{H3} = 2.7 GHz
ESD112-B1						
2nd order intercept point	IP_2		100		dBm	f_{H2} = 1.8 GHz
3rd order intercept point	IP_3		40		dBm	f_{H3} = 2.7 GHz

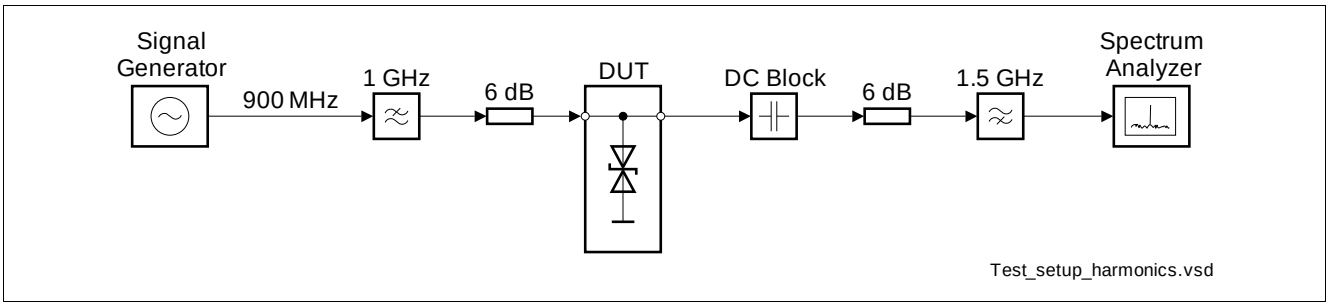

Figure 12 Test setup for harmonics measurements

Harmonics are generated due to nonlinearities. In the case of a silicon diode, there is a nonlinear dependence of junction capacitance (leakage current) on voltage. In general, harmonics of even order (2nd, 4th, …) can be suppressed by a balanced configuration of two diodes [1]. As shown in Figure 13, the DC voltage drop over either diode must be exactly the same in a balanced configuration. When there is no DC voltage on the signal line, both ESD0P4RFL and ESD112-B1 are balanced configurations and thus the 2nd harmonic is greatly reduced compared to any unbalanced configuration such as an unidirectional ESD protection diode. For this reason, unidirectional ESD protection diodes are not recommended for RF applications where the 2nd harmonic is critical.

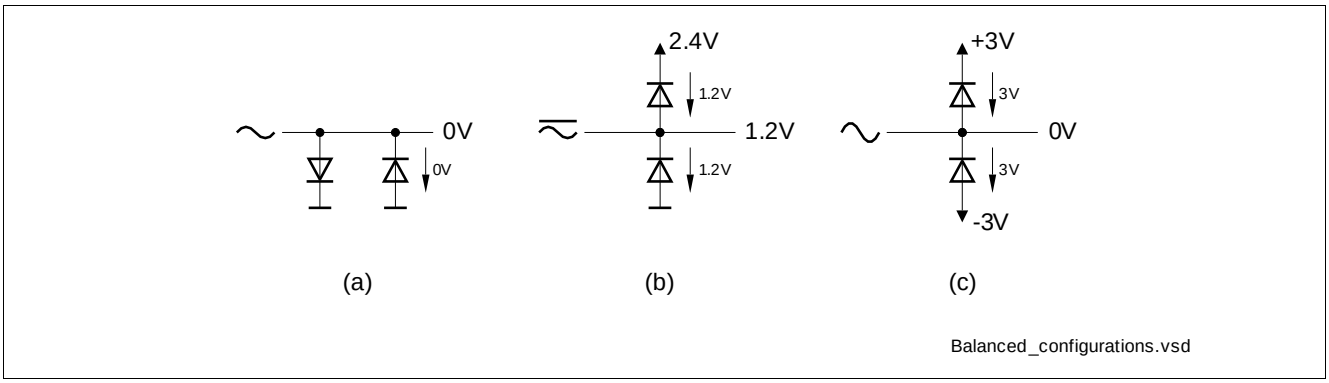

Figure 13 Examples of balanced configurations of two diodes: (a) anti-parallel configuration, (b) rail-to-rail configuration with superimposed DC voltage on signal line and (c) rail-to-rail configuration with negative bias voltage

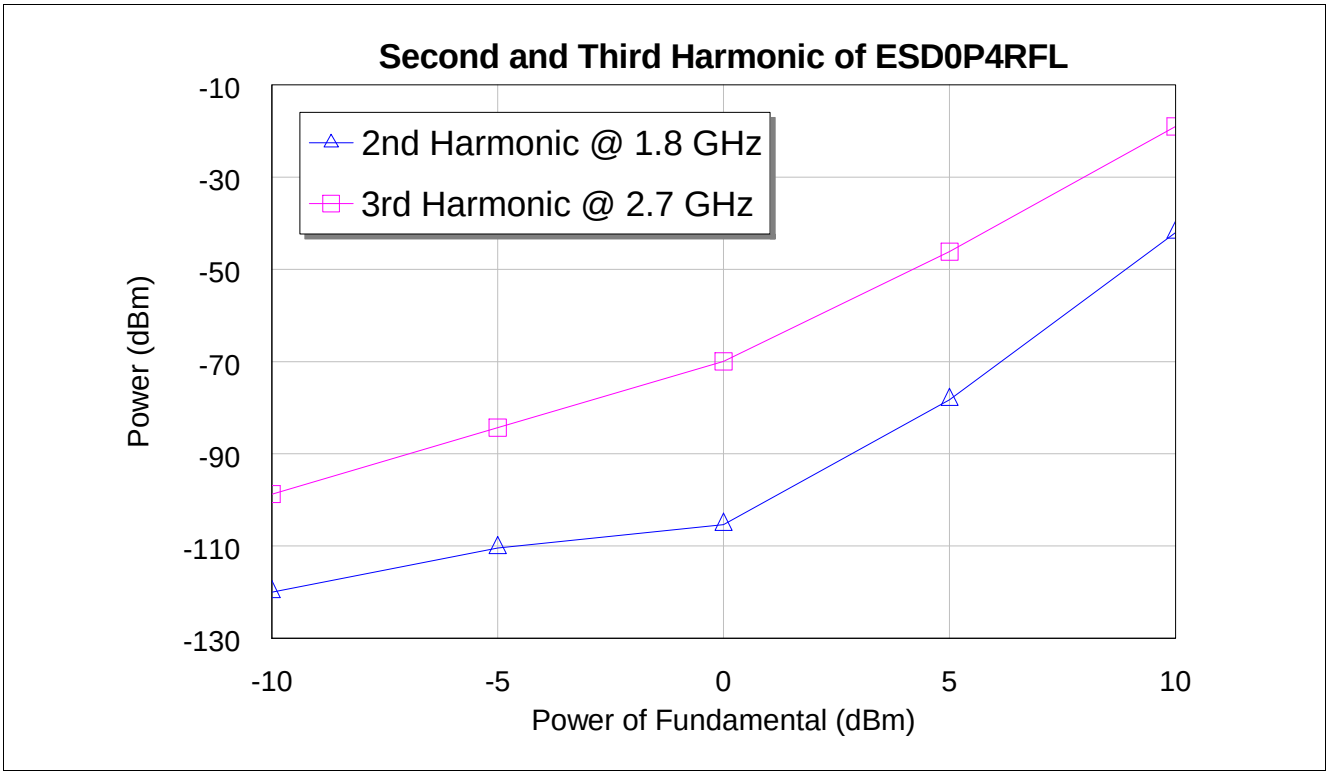

Figure 14 Harmonics generated by ESD0P4RFL from a fundamental tone at 900 MHz in a 50 Ω environment

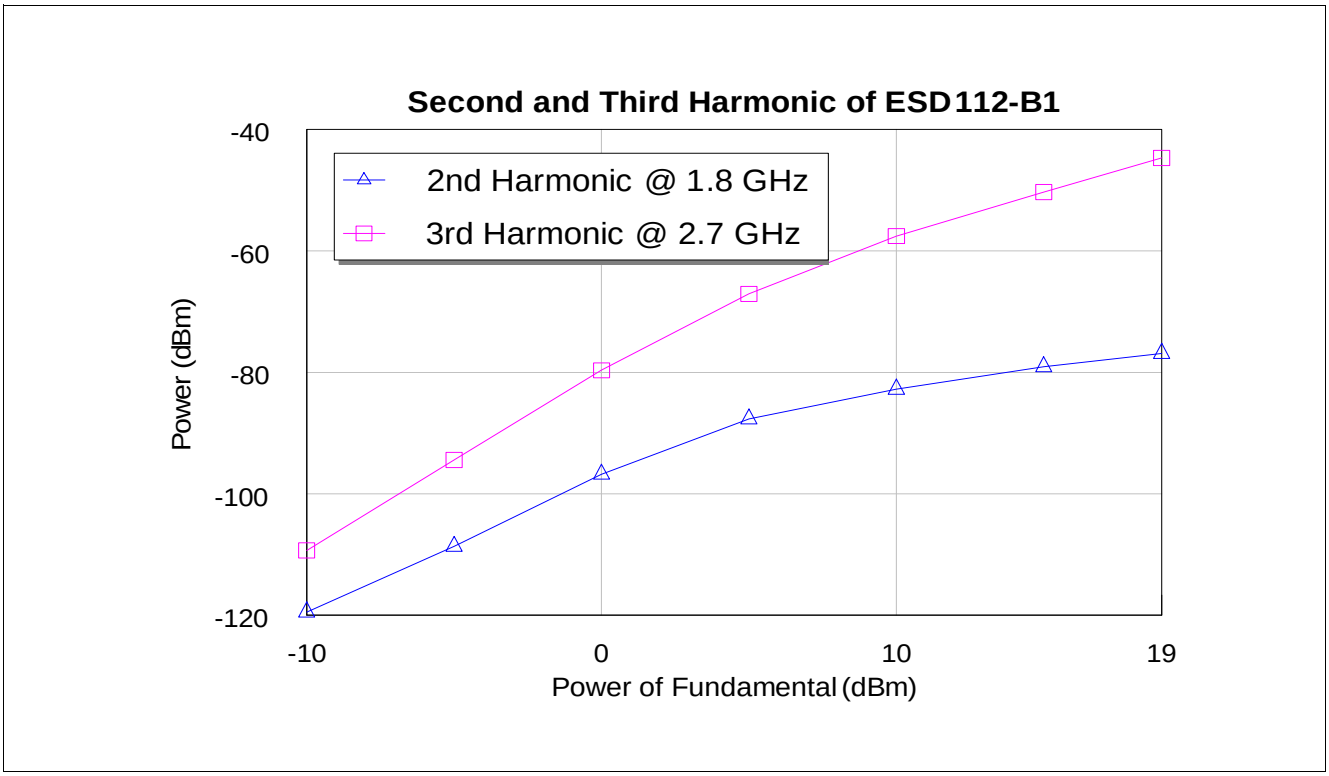

Figure 15 Harmonics generated by ESD112-B1 in steady-state from a fundamental tone at 900 MHz in a 50 Ω environment

Clipping and Self-Biasing

At high RF power levels of more than 0dBm there is a fundamental difference between the anti-parallel ESD0P4RFL and the bidirectional ESD112-B1 (see **Figure 14** and **Figure 15**). While ESD0P4RFL in anti-parallel configuration starts to clip the RF signal and thus becomes even more nonlinear, ESD112-B1 starts to self-bias and becomes less nonlinear. This is because a reverse biased diode, that is when a positive reverse working voltage is applied, is more linear than an unbiased diode (V_R = 0V). The examples shown in **Figure 13** are ordered by their nonlinear behavior with **Figure 13 (a)** showing an unbiased diode (V_R = 0V) with lowest linearity and **Figure 13 (c)** showing a reverse biased diode with higher linearity (V_R = 3V). The self-biasing of ESD112-B1 is therefore an advantage when strong RF interferers are expected. **Figure 16** shows how self-biasing works. The nodes in the middle are gradually charged by the strong interfering signal, which improves the linearity of the bidirectional ESD protection diode significantly. The charging process takes several milliseconds, which makes it appropriate for permanent interfering signals such as TV signals or FM radio signals that are not expected to change their signal strength rapidly within microseconds.

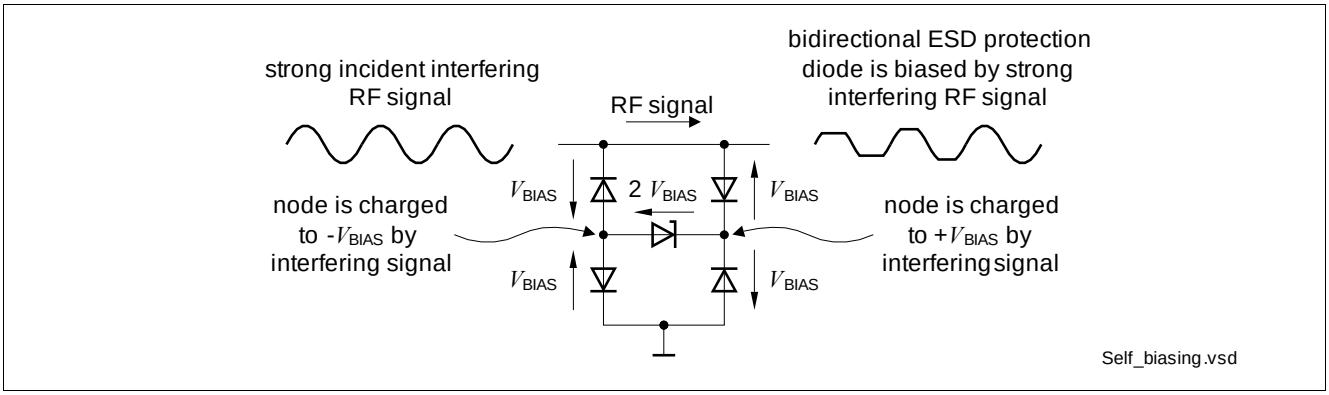

Figure 16 Self-biasing of bidirectional ESD protection diode

9 Clamping Voltage

The clamping voltage were measured with a scope of at least 3GHz analog bandwidth at a sample rate of 20GS/s and a load impedance of 50Ω (see **Figure 17**). Since the maximum peak voltage at the 50Ω input of the scope must not exceed ±4V, an attenuator is needed to damp the voltage to a safe level for the scope. The overall attenuation of 40dB, which forms a 1:100 voltage divider, has been calibrated out prior to measurements. In the post-processing step, offset error and trigger offset were corrected and for noise reduction, a median discharge waveform was calculated by taking the median over 20 consecutive discharges (statistical ensemble).

Of course, in the actual application there will never be a wide-band 50Ω load, and therefore the following figures of merit provide only some kind of benchmark to compare different types of ESD protection diodes. However, the lower the clamping voltage the better the ESD protection capability, but there is no linear relationship between clamping voltage and ESD hardness in the final application. The series resistance is around 1Ω for the bidirectional ESD protection diode ESD112-B1 and even less then 0.5Ω for the anti-parallel ESD protection diode ESD0P4RFL. Therefore, the systematic error due to the load impedance of 50Ω is only 1% and 2%, respectively, which is far less than the variance of the discharge current delivered by the ESD generator.

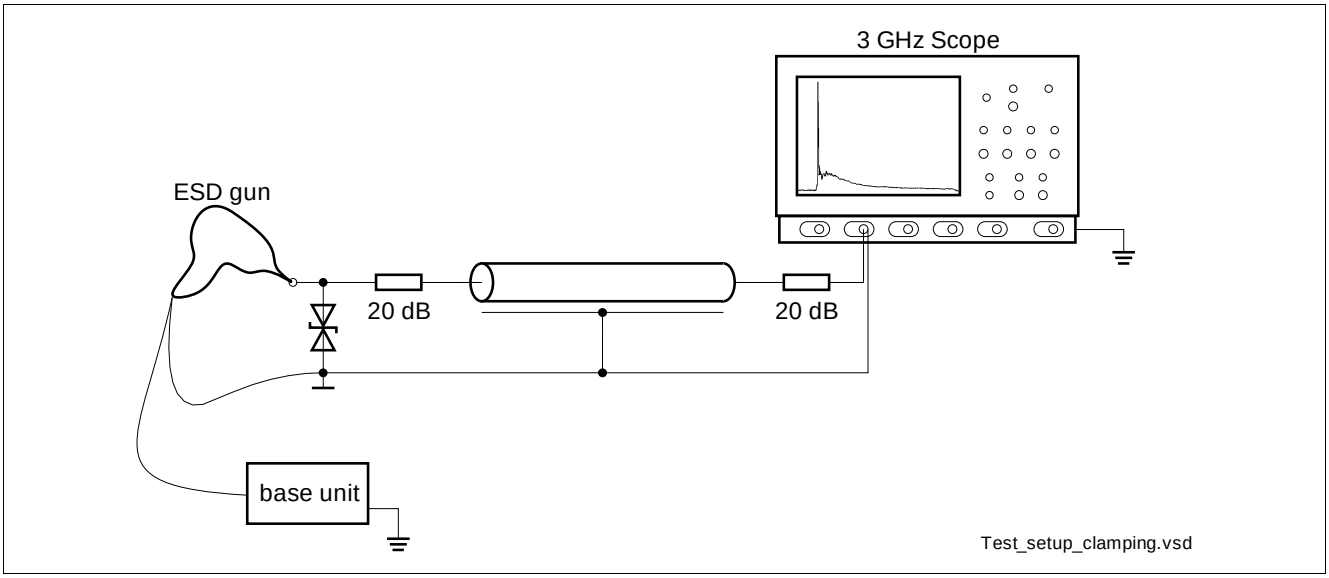

Figure 17 Test setup for clamping voltage measurements

Figure 18 shows the contact discharge short-circuit current waveform of the ESD generator used for clamping voltage measurements. Please note that an ESD source is a current source rather than a voltage source and thus the short-circuit current waveform is defined by the IEC 61000-4-2 standard **[5]**. For more details on this please also refer to Infineon's application note AN103 **[6]**.

The LNA can sustain damage either due to thermal overload because of too much of electrical energy that is dissipated in the LNA or due to too high of a peak voltage (peak current) that results in some kind of breakdown such as dielectric breakdown or second breakdown. It strongly depends on the technology the LNA is based on if either dissipated energy or peak voltage (peak current) will irreversible destroy the LNA. In the following, we will discuss both effects separately from each other.

Energy

Too much of electrical energy can damage the LNA. Therefore, the ESD protection diode has to absorb as much energy as possible. This is equivalent to the claim that the ESD protection diode should have as low a clamping voltage as possible. Due to the inherent nature of bidirectional diodes, their clamping voltage is always higher than the clamping voltage of anti-parallel diodes, which achieve very low clamping voltages. As we will see in the next chapter, low-frequency energy is further suppressed by a simple DC blocking capacitor, which may be already integrated on-chip. ESD0P4RFL suppresses the energy that is dissipated in a wide-band 50Ω load by 38dB, that is the energy of 682,000nWs of the unclamped 8kV ESD event is reduced down to only 106nWs. This is due to the very low clamping voltage, which is, for example, only 7.6V after 30ns. The clamping voltage of ESD112-B1-02ELS is 25V after 30ns and the energy of an 8kV ESD event is suppressed by 27dB down to 1,360nWs. See **Figure 19** for a plot of the clamping voltage and **Figure 20** for a plot of the single side band energy spectral density that is dissipated in a broadband 50Ω load. On the energy spectral density curve it can be seen that ESD protection diodes are quite broadband suppressors with a fairly constant suppression up to 500MHz. The high broadband suppression of ESD0P4RFL is especially advantageous for ESD protection of broadband amplifiers, where decoupling between ESD protection diode and ESD sensitive LNA is hardly possible (see also next chapter).

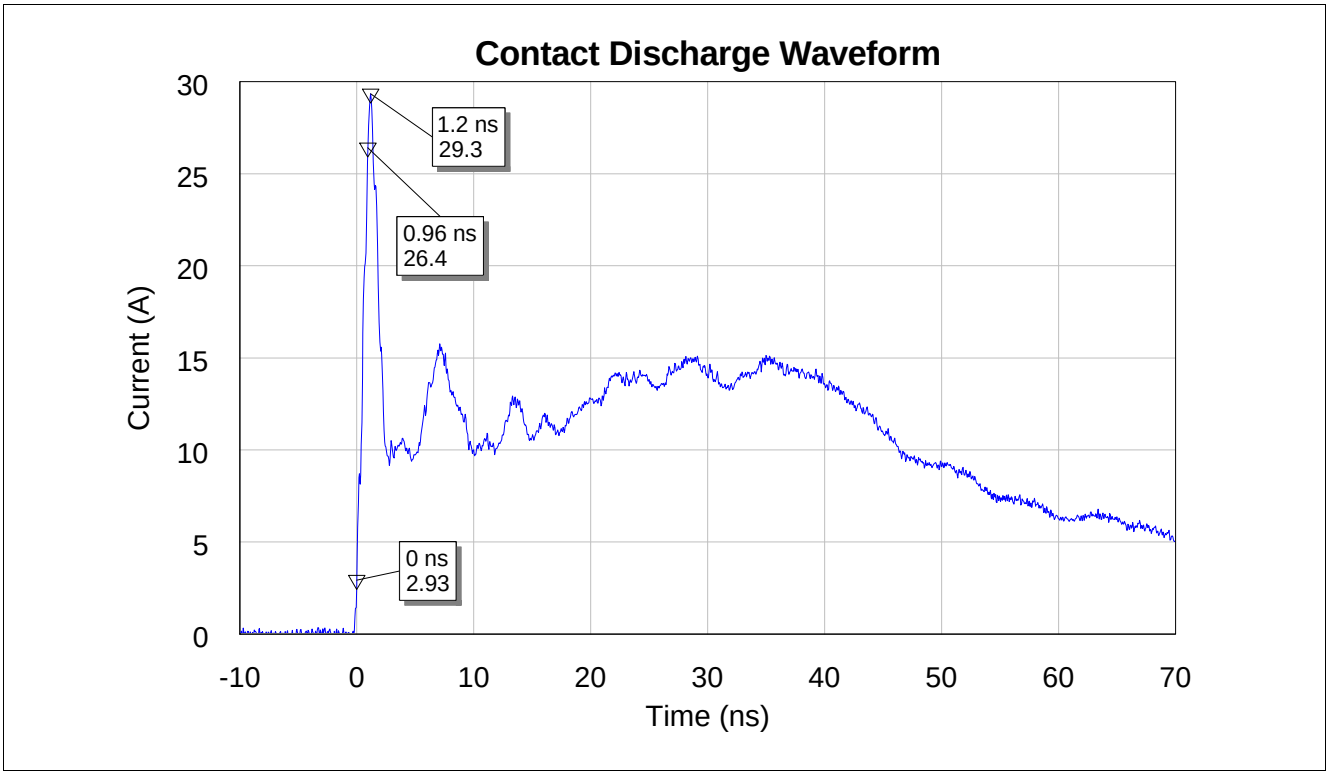

Figure 18 Contact discharge waveform of ESD generator, charge voltage = 8kV (level 4)

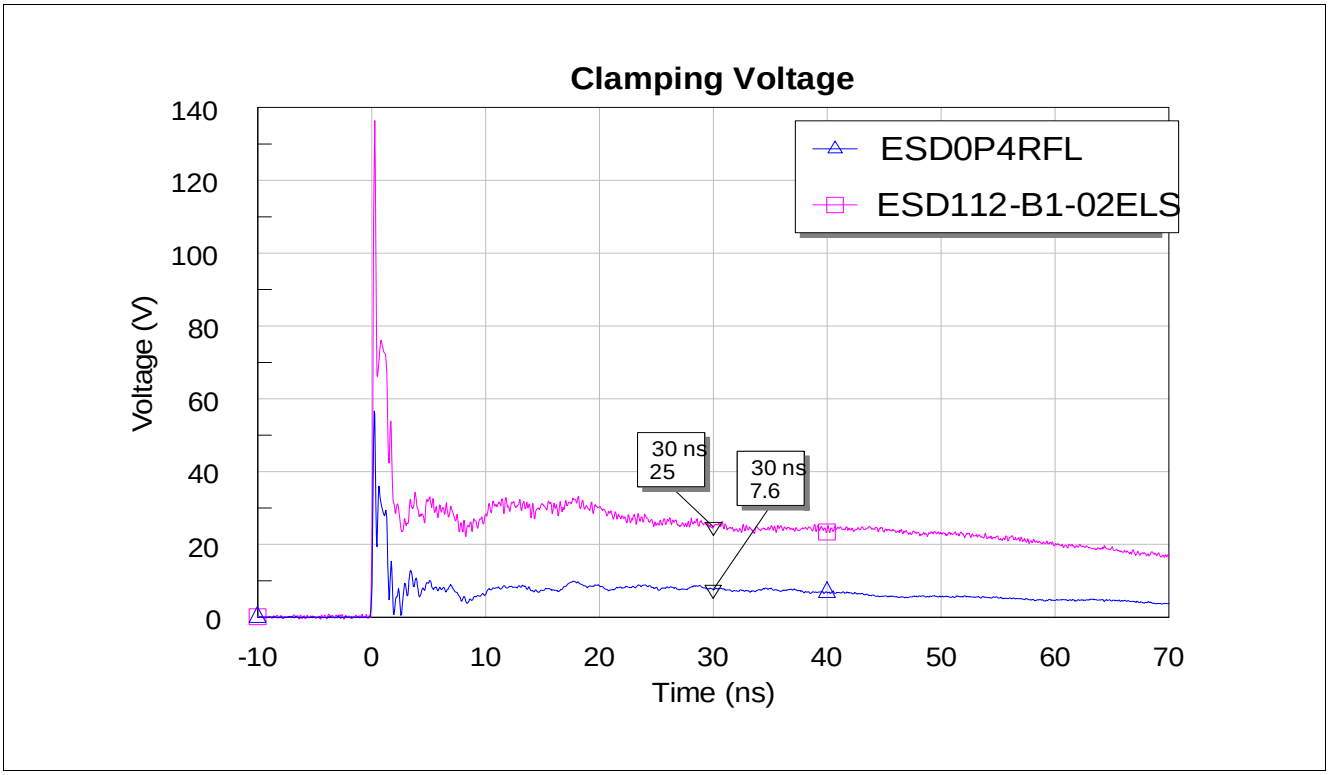

Figure 19 Clamping voltage of ESD112-B1-02ELS and ESD0P4RFL, charge voltage = 8kV

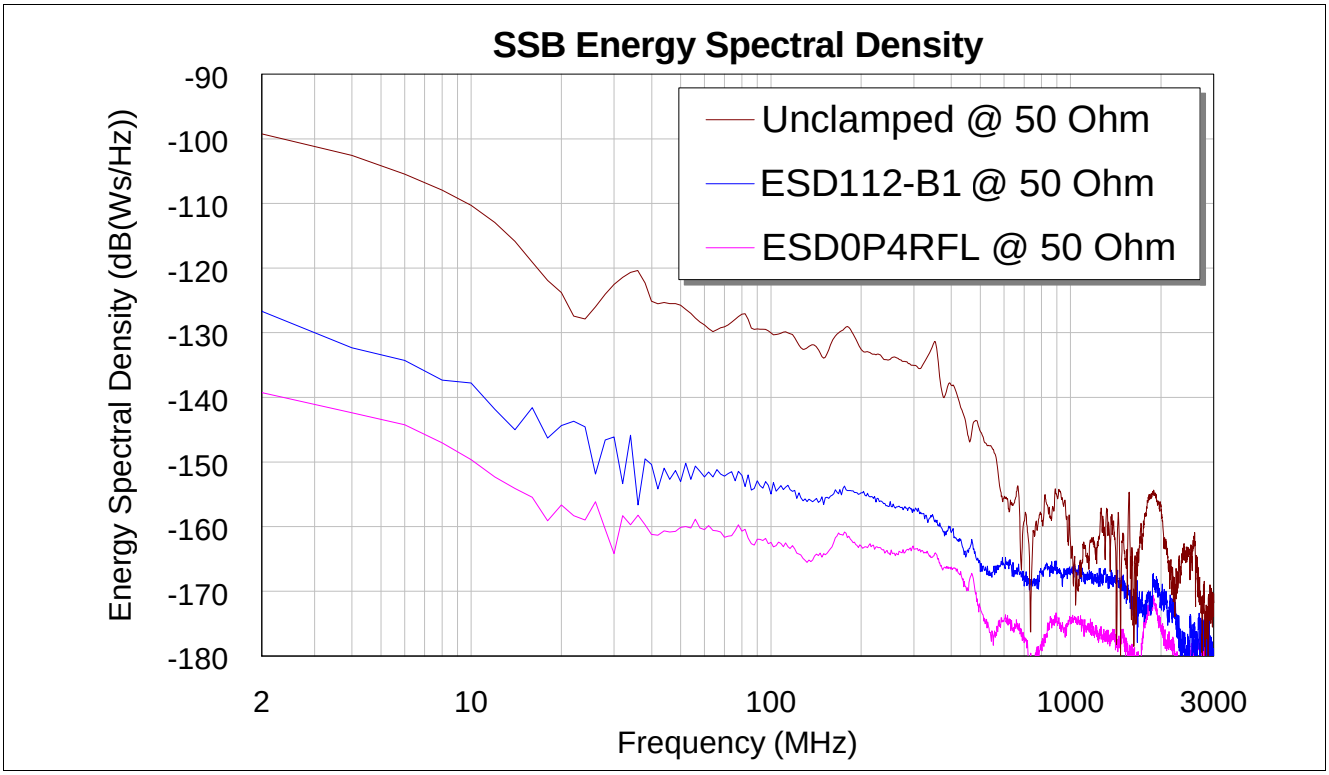

Figure 20 Single side band energy spectral density dissipated in a 50Ω load, charge voltage = 8kV

Peak Voltage

Too high of a peak voltage can damage the LNA. Therefore, the ESD protection diode should respond significantly faster than 1ns, because the typical rise time of a 5kV ESD event is between 0.7ns and 1ns. Please note that the contact discharge waveform of the ESD generator defined by the IEC61000-4-2 standard is based on a typical 5kV ESD event. This means that the rise time is independent of charge voltage while the discharge current scales linearly with charge voltage. **Figure 18** shows the 8kV contact discharge waveform of the ESD generator, which equates to level 4 of the IEC 61000-4-2 standard. As one can see, the rise time of the contact discharge waveform of the ESD generator is 0.96ns. Scopes are usually provided with an analog filter with maximally flat response. For such filters, the relationship between 10% to 90% rise time, t_r, and 3dB bandwidth, f_{3dB}, is as follows:

$$f_{3dB} \approx \frac{0.45}{t_r} \tag{6}$$

According to **Equation (6)** a scope with an analog bandwidth of 1GHz is sufficient to measure the peak voltage of the contact discharge waveform of the ESD generator correctly. However, since the ESD protection diode must be much faster than 1ns, a scope with an analog bandwidth of at least 2.5GHz is needed to measure the peak voltage correctly. Furthermore, also a high sample rate is needed in order to make sure that the peak will be sampled at all. All curves shown herein were measured on scopes with an analog bandwidth of at least 3GHz and at a sample rate of 20GS/s. As shown in **Figure 21** the 10% to 90% rise time of both ESD0P4RFL and ESD112-B1 is about 0.2ns and thus both are significantly faster than a typical ESD event.

The very low peak voltage of only 57V together with the very low clamping voltage make ESD0P4RFL the first choice for ESD protection of extremely ESD sensitive RF LNAs. Due to the inherent nature of ESD112-B1-02ELS, the peak voltage of 136V is roughly twice as high as that of ESD0P4RFL. However, by appropriate decoupling ESD112-B1-02ELS can protect ESD sensitive LNAs almost as good as ESD0P4RFL (see also next chapter). The low peak voltage is not only due to the fast response time, but also due to the very low parasitic inductance of the

leadless package. Even an additional inductance of only 0.2nH results in an increase in peak voltage of approximately 12V. Therefore, diodes in leaded packages are not recommended to protect ESD sensitive RF LNAs.

Attention: In order to measure peak voltage correctly, the analog bandwidth of the scope must be at least 2.5GHz and the sample rate must be at least 10GS/s. Do not trust clamping curves measured with sample rate of only 5GS/s or less!

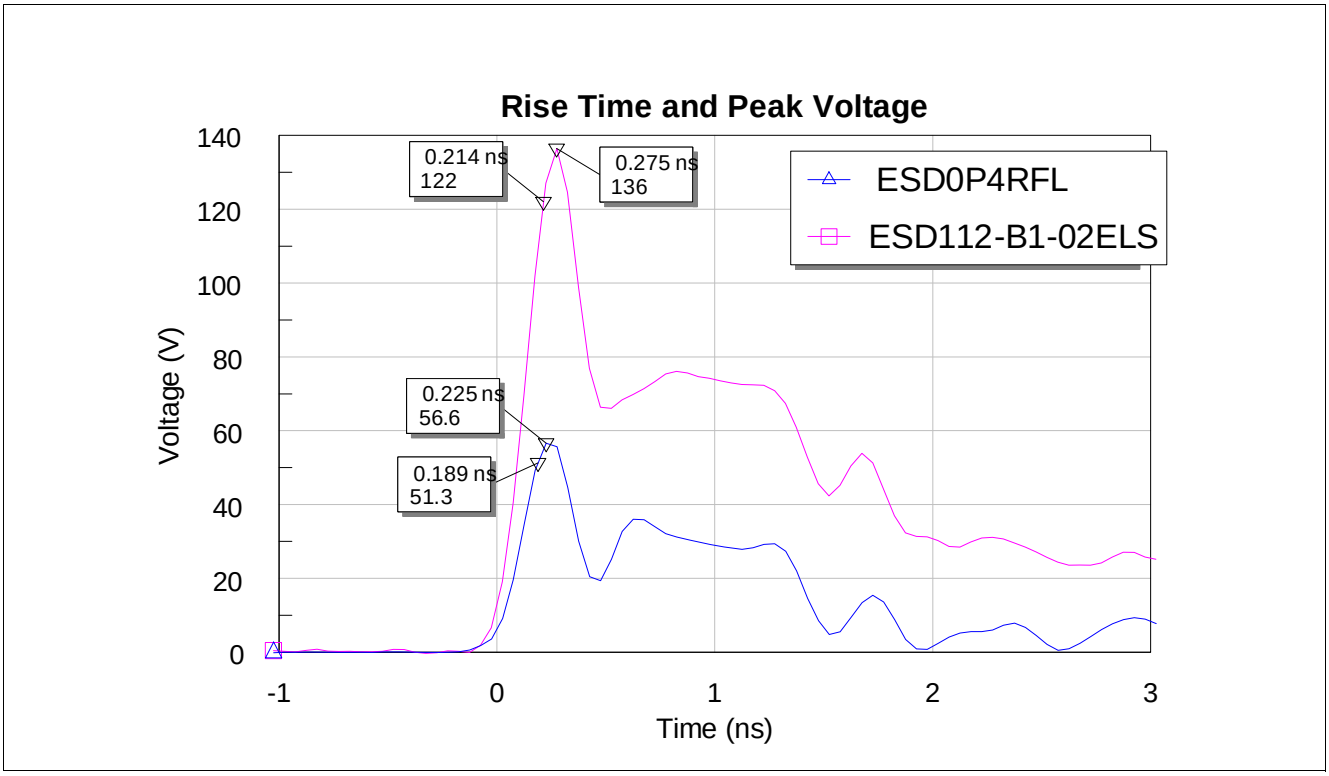

Figure 21 Peak voltage and rise time of ESD112-B1-02ELS and ESD0P4RFL, charge voltage = 8kV

10 Application Example

Please also refer to Infineon's application note AN167 **[8]** for an example of ESD protection with ESD0P4RFL and ESD112-B1-02ELS.

10.1 Low-inductive ground path

Any inductance in series to the ESD protection diode must be avoided. This not only reduces the RF bandwidth, but—even more critical—also results in excessive ringing of the clamping voltage and thus in an increased peak voltage. Do not use a thin trace as ground for ESD protection diodes. Use a big copper pad and place vias to ground as close as possible to the ground pad of the ESD protection diode. See **Figure 22** for an example.

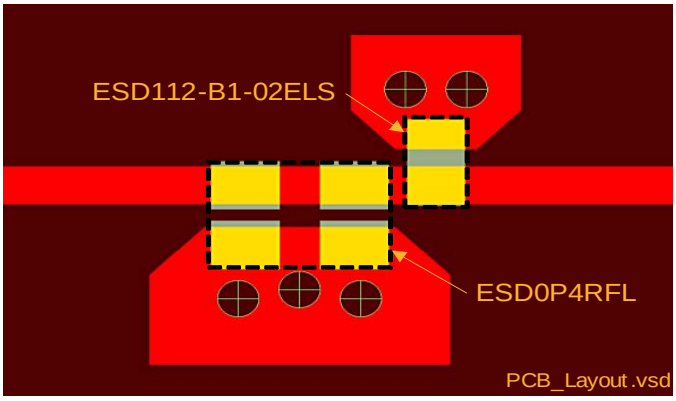

Figure 22 PCB layout example for ESD112-B1-02ELS and ESD0P4RFL

10.2 Decoupling of ESD protection diode and LNA

Since most of the energy of an ESD event is located in the low-frequency region, ESD hardness can be enhanced by a high-pass filter between ESD protection diode and LNA. Therefore, the greater the cut-off frequency of the high-pass filter the greater the ESD hardness. Basically, decoupling means that due to Kirchhoff's laws most of the current arising from the ESD event is forced through the ESD protection diode rather than be divided more or less equally between ESD protection diode and LNA. For example, in the case of a bipolar RF transistor as LNA there would be two diodes in parallel without decoupling: The base-emitter diode of the transistor and the ESD protection diode.

DC Blocking Capacitor

The easiest high-pass filter is a simple DC blocking capacitor as shown in **Figure 23 (a)**. For a high cut-off frequency one should use low-cap DC blocking capacitors on the antenna RF line (between ESD protection diode and LNA). For example, a 15 pF capacitor of 0402 case size has a typical self-resonant frequency of 1.8 GHz. So, for an application operating above 1 GHz there is no benefit from using a 1 nF capacitor instead. Quite the contrary, the higher impedance of the 15 pF capacitor at low frequencies significantly enhances ESD hardness. The minimum DC blocking capacitance, C, for a given insertion loss, IL (expressed in dB), at the lower pass-band frequency is as follows:

$$C = \frac{1}{2\omega_1 Z_0 \sqrt{a-1}}, \tag{7}$$

where Z_0 is the source and load impedance seen by the capacitor (usually $Z_0 = 50\,\Omega$), $\omega_1 = 2\pi f_1$ and

$$a = |S_{21}|^{-2} = 10^{IL/10} \tag{8}$$

is the attenuation of the DC blocking capacitance at frequency f_1 (see also **Figure 24**). Of course, if the DC blocking capacitor is already integrated on-chip on the LNA, no additional external DC blocking capacitor is needed anymore. Furthermore, even on-chip capacitors that are realized as MIM-caps are limited to some picofarad only and therefore provide a high cut-off frequency.

Band-pass filter

For pass-band frequencies below 100 MHz a simple DC blocking capacitor may not be sufficient to block the first pulse arising from the ESD event. In this case, decoupling can be enhanced by an additional inductor forming a band-pass filter as shown in **Figure 23 (b)**. Due to the low quality factor of inductors at low frequencies we have

to consider the loss of the inductor as well. Thus, the inductance, L, for a given insertion loss, IL, at the lower pass-band frequency can be calculated as follows:

$$L = \frac{2Z_0 Q_{ind}}{\omega_1} \cdot \frac{\sqrt{1+q(a-1)}-1}{q}, \text{ with } q = 1 + Q_{ind}^2\left(1-\left(\frac{\omega_0}{\omega_1}\right)^2\right)^2, \quad (9)$$

where Z_0 is the source and load impedance seen by the filter,

$$\omega_0 = \sqrt{\omega_1 \omega_2} \quad (10)$$

is the resonant frequency of the band-pass filter, $\omega_1 = 2\pi f_1$ is the lower pass-band frequency, $\omega_2 = 2\pi f_2$ is the upper pass-band frequency, Q_{ind} is the quality factor of the inductor at the lower pass-band frequency, f_1, and a is the attenuation of the band-pass filter at the lower pass-band frequency, f_1, as given by **Equation (8)**. See **Figure 24** for an equivalent circuit of the band-pass filter. The capacitance, C, is then given by:

$$C = \frac{1}{\omega_0^2 L} \quad (11)$$

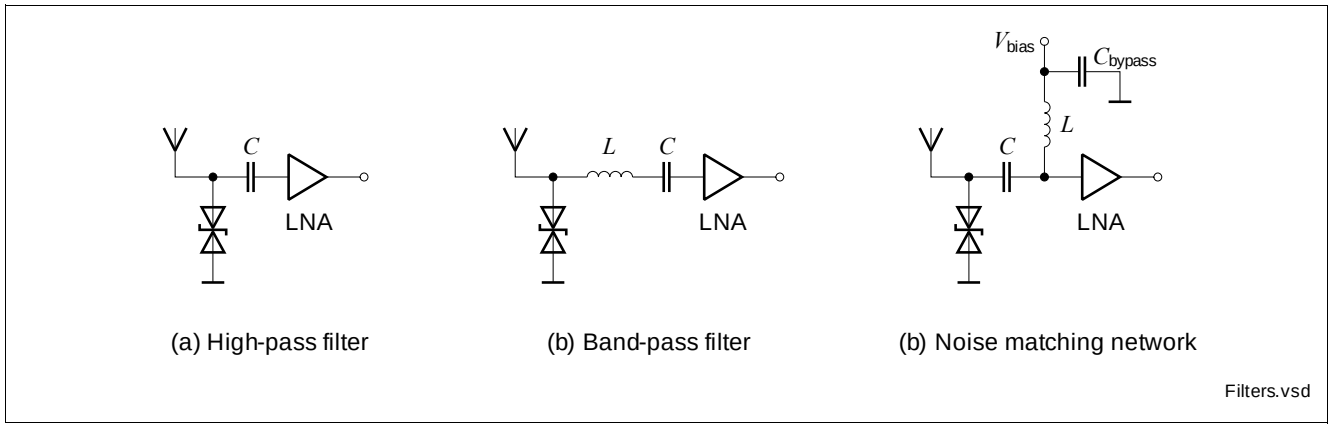

Figure 23 Three different techniques for decoupling of ESD protection diode and LNA: (a) simple DC blocking capacitor as 1st order high-pass filter, (b) band-pass filter for applications operating around 100 MHz or lower and (c) noise matching network as 2nd order high-pass filter

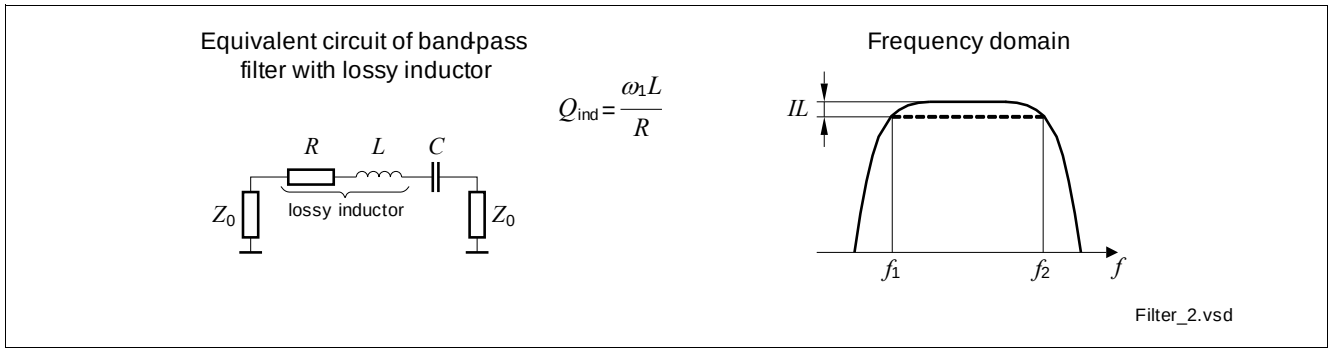

Figure 24 Equivalent circuit of band-pass filter. Insertion loss, IL, is defined at the lower frequency f_1

Noise matching network

If an impedance matching network for optimum noise match for an ESD sensitive LNA is needed, the noise matching network should be designed as 2nd order high-pass filter as shown in **Figure 23 (c)**. The 3dB cut-off frequency of the noise matching filter is usually somewhat lower than the application frequency, but it should be greater than one third of the application frequency. In this way one gets noise matching and decoupling for LNAs operating in the gigahertz range in one go. An example of a GPS LNA operating at 1.575GHz is shown in **Figure 25**. The Infineon RF transistor BFP740F, which can withstand only 400V as per HBM (Human Body Model **[4]**), is effectively protected up to ±10kV as defined by the IEC 61000-4-2 standard by simple using ESD0P4RFL together with a noise matching network that has a cut-off frequency of 1.1GHz. ESD0P4RFL increases noise figure of the LNA only by 0.06dB.

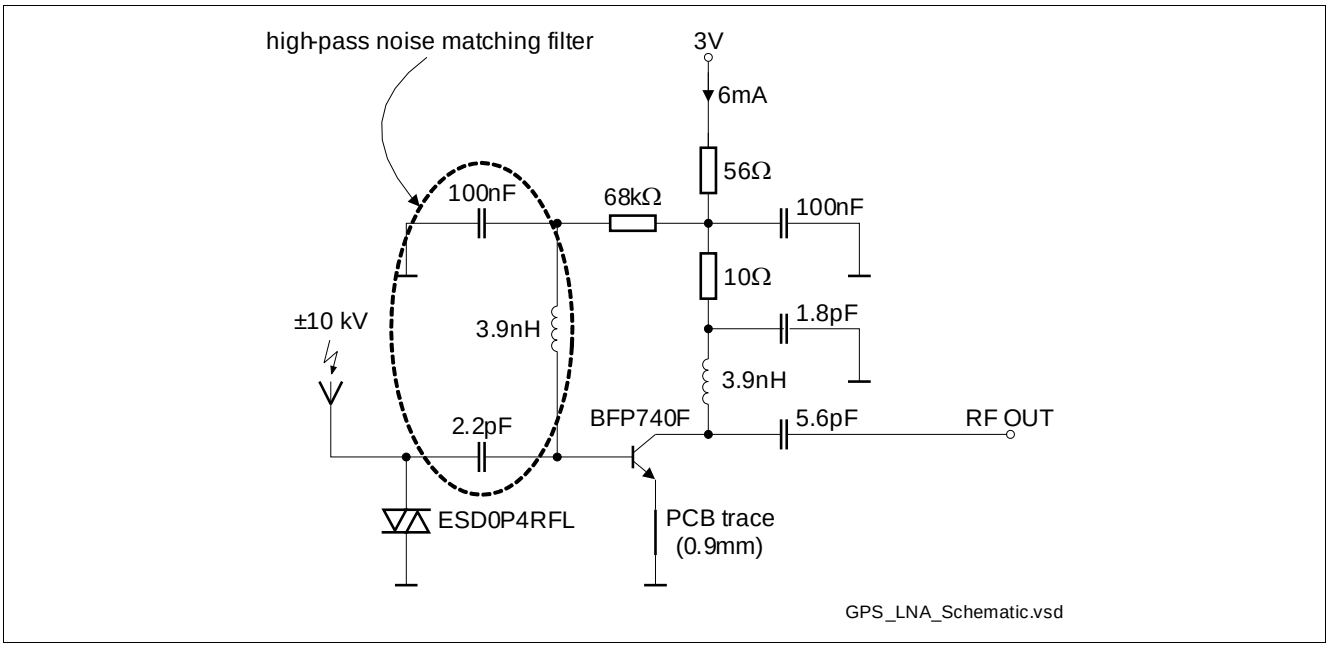

Figure 25 Example of a high-pass noise matching network to decouple ESD protection diode and ESD sensitive RF transistor

Table 2 Electrical characteristics of GPS LNA shown in Figure 25

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{CC}		3		V	
Supply current	I_{CC}		6		mA	
Gain	$\|S_{21}\|^2$		20		dB	
Noise figure[1)]	NF		0.85		dB	incl. SMA connector and PCB losses
Input return loss	RL_{IN}		11		dB	
Output return loss	RL_{OUT}		12		dB	
Reverse isolation	I_{REV}		27		dB	
Stability factor	k		> 1			from 0 to 8.5GHz
ESD hardness	V_{ESD}		> 10		kV	IEC 61000-4-2 contact discharge

1) Noise figure without ESD0P4RFL is 0.8dB (including SMA connector and PCB losses)

10.3 Ultra wide band applications

For ultra wide band applications the low capacitance of ESD112-B1-02ELS can be easily compensated to extend the frequency range of the 20dB return loss point from 3.2GHz to 10GHz, which is more than adequate for recent UWB applications. Here, compensation is achieved by a 1.9mm long, 84Ω microstrip line surrounding the ESD protection diode as shown in **Figure 27**. Even with compensation the 20 dB return loss point cannot be extended to any frequency range, because the length of the compensation structure must be significantly shorter than the wave length. Thus, for UWB applications an inherent low capacitance of the ESD protection diode is mandatory. For example, to compensate the capacitance of ESD0P4RFL a 84Ω microstrip line with a length of 3.7mm is needed. This is twice the length that is needed for ESD112-B1-02ELS, and therefore the frequency range of the 20dB return loss point can be extended to “only” 6GHz. **Figure 26** shows a plot of the return loss of ESD112-B1-02ELS with compensation of capacitance, which is based on the simulation of the layout shown in **Figure 27**. For more details on this please refer to Infineon’s application note AN140 **[7]**.

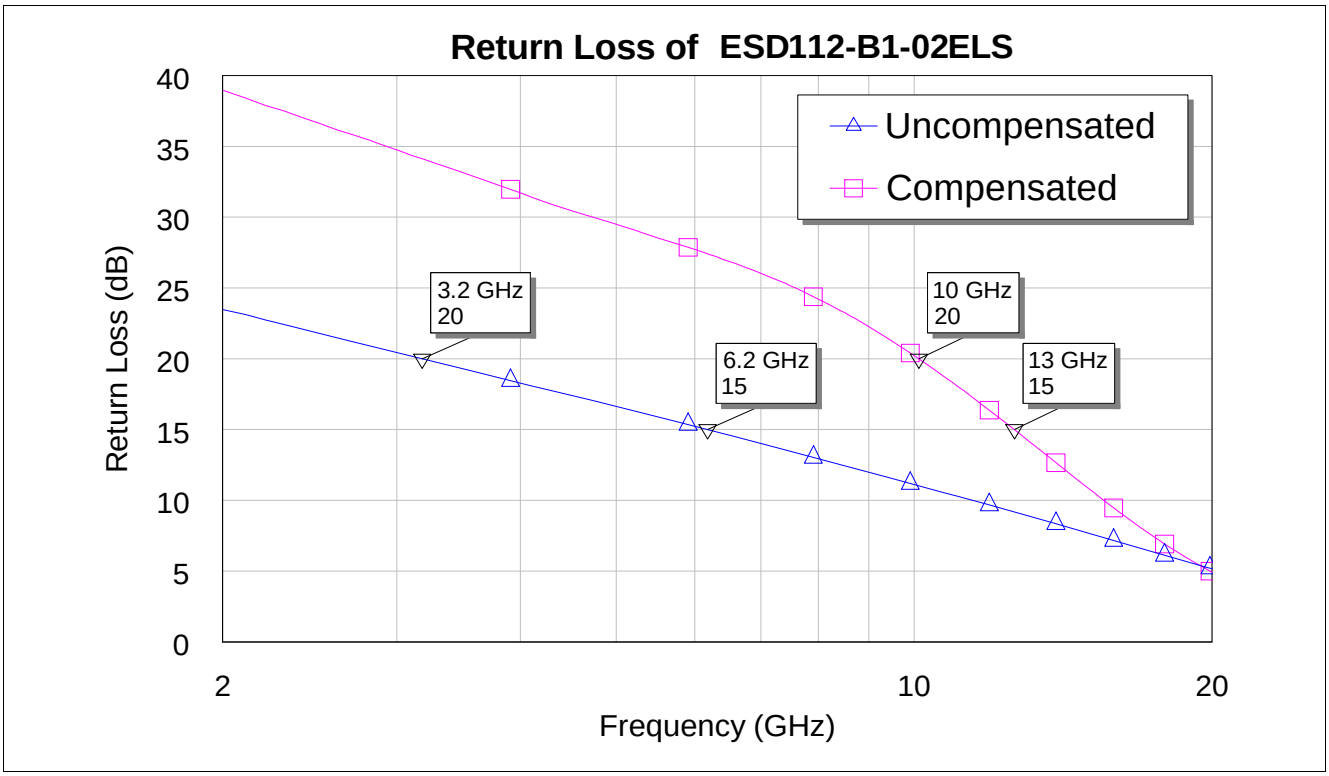

Figure 26 Return loss of ESD112-B1-02ELS without and with compensation of capacitance

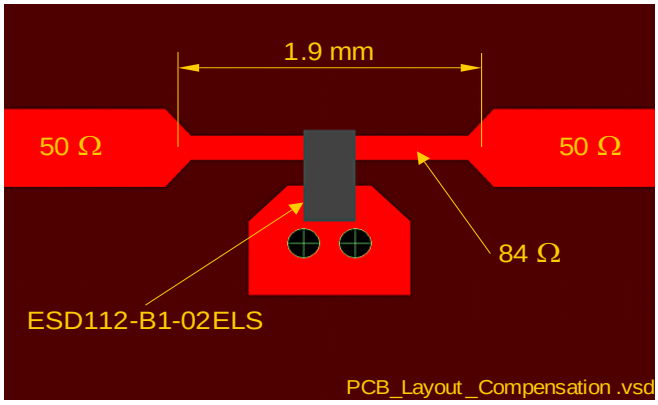

Figure 27 Layout example on how the small capacitance of ESD112-B1-02ELS can be compensated

11 About Other Solutions

On the market one can find other sub-picofarad solutions than low-cap ESD protection diodes such as polymer-based suppressors or multilayer varistors. For a comparison of clamping voltages please refer also to Infineon's application note AN103 **[6]**. So, the question that arises is whether they can protect ESD sensitive RF transistors as well. To answer this question, the GPS LNA shown in **Figure 25** was also tested with a multilayer varistor (MLV), which has a typical capacitance of 0.5pF, and a polymer-based suppressor, which has a typical capacitance of less than 0.15pF up to 1.8GHz. The ESD test voltage was increased step-by-step until the supply current significantly decreased, which indicates a failure or significant degradation of the RF transistor. At each step 10 contact discharges with either polarity were applied to the RF input pin. **Figure 28** shows the results as plot of supply current versus ESD test voltage. After the DC failure level was known a before and after comparison was done, for which the ESD test voltage was chosen to be approximately 30% below the DC failure level. See **Table 3** for a summary of the before and after comparison. Infineon's ESD0P4RFL effectively protects the RF transistor from ±10kV contact discharges and there is no significant change in electrical characteristics even after 500 contact discharges. This well exceeds protection level 4 as defined by the IEC 61000-4-2 standard, which is the highest protection level that is defined for contact discharge (8kV charge voltage).

Polymer-based suppressor

As expected, the polymer-based suppressor cannot protect the ESD sensitive RF transistor, because its trigger voltage of 300V is far too high. The RF transistor dies long before the polymer-based suppressor gets triggered. This makes polymer-based suppressors completely useless and a before and after comparison pointless.

Multilayer varistor

Multilayer varistors (MLVs) have a similar structure like multilayer ceramic capacitors (MLCCs), except that MLVs make use of zinc oxide (ZnO) grains as dielectric between two electrodes. In order to get sub-picofarad MLVs, the electrode spacing has to be increased, which lengthens the path through which the current must travel, increasing varistor voltage (= breakdown voltage) and series resistance. Therefore, sub-picofarad MLVs suffer from very high clamping voltages and their ESD protection capability is much worse compared to sub-picofarad ESD protection diodes. Furthermore, the before and after comparison has revealed that MLVs suffer from a large number of ESD events. After 500 contact discharges with only 4.5kV, which is quite below the maximum rating of the MLV, its noise figure increases by more than 0.4dB. Hence, MLVs are absolutely inadequate for ESD protection of ESD sensitive RF LNAs with noise figures around 1dB or less.

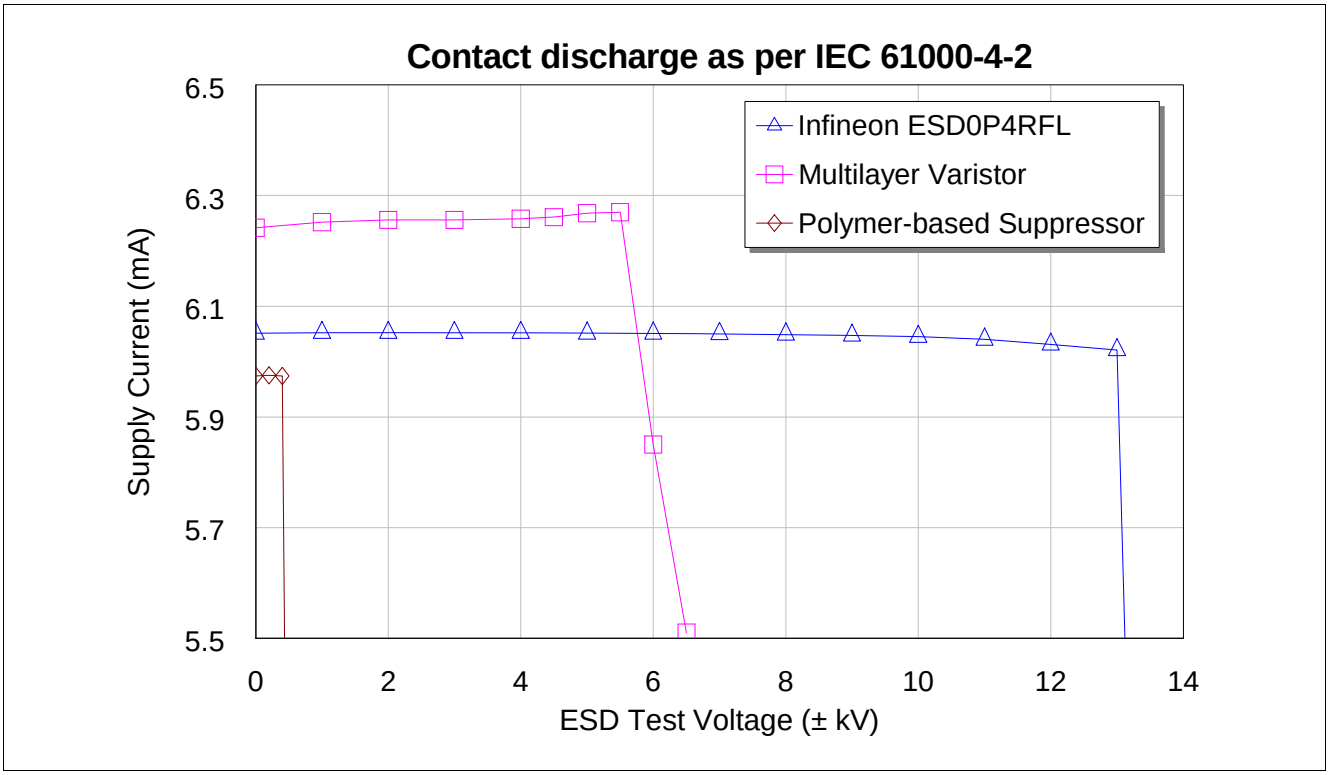

Figure 28 DC failure levels for different ESD protection devices

Table 3 Results of before and after comparison

Parameter	Symbol	ESD Protection Device				Unit
		w/o	ESD0P4RFL	MLV	Polymer-based	
Capacitance	C	-	0.4	0.5	< 0.15	pF
Noise figure	NF	-	0.06	0.10	< 0.02	dB
DC failure level	$V_{ESD\text{-}Failure}$	< 1	14	6	< 1	kV
Before ESD testing						
Supply current	I_{CC}	-	6.14	6.00	-	mA
Noise figure	NF	-	0.87	0.93	-	dB
After applying 500 contact discharges as per IEC 61000-4-2 (250 discharges per polarity)						
ESD test voltage	V_{ESD}	-	10	4.5	-	kV
Supply current	I_{CC}	-	6.08	5.96	-	mA
Noise figure	NF	-	0.88	**1.37**[1)]	-	dB

1) After the stressed MLV was replaced by a new one, noise figure was again 0.93 dB. So, it was the MLV that degraded and not the Infineon RF transistor BFP740F.

12 Conclusion

It has been shown that Infineon's ESD protection diodes ESD0P4RFL and ESD112-B1 are very much suited for ESD protection of RF interfaces up to frequencies as high as 10 GHz. Even though low capacitance is necessary for RF applications operating in the gigahertz range, it is not all to be considered. Low noise figure, low parasitic

inductance to gain high bandwidth, low harmonic generation, robustness against interferer, fast response time and, most important, low clamping voltage to protect even the most ESD sensitive RF transistor are also crucial factors for RF applications. And of course, the ESD protection device must not suffer from a large number of ESD events! Nothing is more annoying than an ESD protection device that ruins noise figure after several ESD events. Then all the effort and money spent on the LNA's low noise figure was to no avail. To cap it all off, Infineon shrunk the ESD protection diode and put it into an incredible small package of only 0201 case size. So, now there is no excuse anymore for not having enough space for ESD protection!

13 Appendix

For more details on the following please refer to **[2]** and **[3]**. A noisy microwave component can be characterized either by noise temperature or by noise figure. Noise temperature is the equivalent temperature of a resistor at the input of the component, which is then considered as noiseless, while noise figure is a measure of the degradation in the signal-to-noise power ratio between the input and output of the component. It is important to understand, that noise figure is defined for a matched noise source that consists of a resistor at temperature T_0 = 290K.

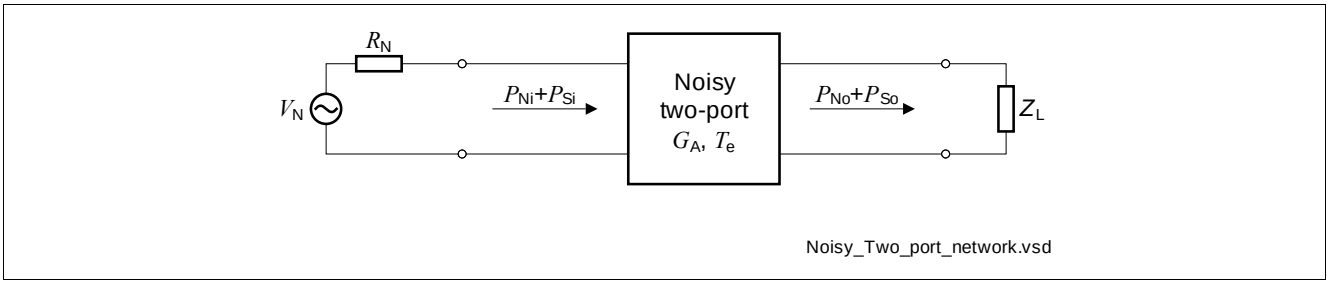

Figure 29 Equivalent circuit of a noisy resistor delivering noise power to a noisy two-port network

A noisy source resistor R_N can be modeled by a noiseless source resistor R_N and a noise voltage source V_N as shown in **Figure 29**. The maximum available noise power from the source resistor R_N is given by

$$P_N = \frac{V_N^2}{4R_N} = kTB\,, \tag{12}$$

where k = 1.38 10^{-23}J/K is the Boltzmann constant, T is the temperature in kelvin (K), B is the bandwidth of the system in Hz and V_N is the rms-value of the noise voltage in volt.

Noise factor F is defined as the ratio of the available signal-to-noise power ratio at the input to the available signal-to-noise power ratio at the output:

$$F = \frac{P_{Si}/P_{Ni}}{P_{So}/P_{No}}\,. \tag{13}$$

Since the available noise power at the input, P_{Ni}, and output, P_{No}, of the microwave component is considered, also the available signal power at the input, P_{Si}, and output, P_{So}, and thus the available power gain G_A of the microwave component must be considered, rather than simply the transducer power gain. Using the available power gain, G_A, of the microwave component, we can rewrite **Equation (13)** to

$$F = \frac{P_{No}}{P_{Ni}G_A}\,, \tag{14}$$

where

$$G_A = \frac{P_{So}}{P_{Si}}. \tag{15}$$

By definition, the available noise power at the input, P_{Ni}, is due to a resistor at temperature T_0 and thus from **Equation (12)** it follows that

$$P_{Ni} = kT_0B. \tag{16}$$

The noise power internally generated by the microwave component can also be thought of as noise power due to a resistor at equivalent temperature T_e at the input of an otherwise noiseless microwave component. The available noise power at the output of the microwave component can then be expressed as

$$P_{No} = k(T_0 + T_e)BG_A, \tag{17}$$

where T_e is the equivalent noise temperature of the microwave component. Using these results in **Equation (14)** gives noise factor as

$$F = 1 + \frac{T_e}{T_0}. \tag{18}$$

Now we will consider the special case for a passive, lossy two-port network **[2]**. When the entire system is in thermal equilibrium at temperature T, the maximum available noise power at the output must be $P_{No} = kTB$. But we can also think of this power coming from the source resistor and from the lossy two-port network itself:

$$P_{No} = kTB = k(T + T_e)BG_A. \tag{19}$$

Solving **Equation (19)** for the equivalent noise power T_e gives

$$T_e = (L-1)T, \tag{20}$$

where L is the loss factor, defined as $L = 1/G_A > 1$. Then from **Equation (18)** noise factor is

$$F = 1 + (L-1)\frac{T}{T_0}. \tag{21}$$

Therefore, noise factor of a passive, lossy two-port network at room temperature, that is $T \cong T_0$, is given by

$$F\big|_{T \cong T_0} \cong L = \frac{1}{G_A}. \tag{22}$$

Noise figure NF, which is noise factor F expressed in decibel (dB), of a passive, lossy two-port network at room temperature is therefore given as

$$NF\big|_{dB} \cong L\big|_{dB} = -G_A\big|_{dB}. \tag{23}$$

Insertion loss, IL, and return loss, RL, are defined as follows:

$$IL\big|_{dB} = -20\log|S_{21}|, \tag{24}$$

$$RL\big|_{dB} = -20\log|S_{22}|, \tag{25}$$

where $S_{21} = S_{12}$ is the transmission coefficient and $S_{22} = S_{11}$ is the reflection coefficient of the diode in a 50Ω environment as per **Figure 30**. The available gain, G_A, of the diode when the source impedance is matched to 50Ω, that is $\Gamma_S = 0$, calculates from the S-parameters as follows:

$$G_A = \left.\frac{|S_{21}|^2}{1-|S_{22}|^2}\right|_{\Gamma_S = 0} . \quad (26)$$

Thus, noise figure can also be interpreted as insertion loss minus mismatch loss:

$$NF|_{dB} = IL|_{dB} - ML|_{dB} , \quad (27)$$

where mismatch loss ML is according to **Equation (26)** as follows:

$$ML = \frac{1}{1-|S_{22}|^2} , \quad (28)$$

or expressed in dB

$$ML|_{dB} = -10 \log(1 - 10^{-RL/10}) . \quad (29)$$

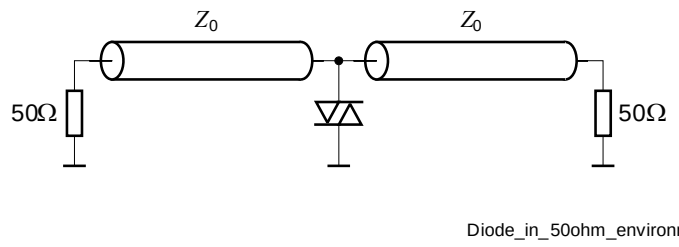

Figure 30 Diode, for example ESD0P4RFL, as two-port network in a 50 Ohm environment

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[3] Guillermo Gonzales, “Microwave Transistor Amplifiers: Analysis and Design,” Prentice-Hall, N.J., 1984.

[4] JESD22-A114D, “Electrostatic Discharge (ESD) sensitivity testing Human Body Model (HBM),” JEDEC Solid State Technology Association, March 2006.

[5] IEC 61000-4-2, Electromagnetic Compatibility (EMC) Part 4: Testing and measurement techniques – Section 2: “Electrostatic discharge immunity test,” International Electrotechnical Commission, 1995.

[6] Infineon Technologies: “Application Note No. 103: ESD and Antenna Protection using Infineon ESD0P8RFL”

[7] Infineon Technologies: “Application Note No. 140: ESD Protection for Digital High-Speed Interfaces (HDMI, FireWire,...) using ESD5V3U1U”

[8] Infineon Technologies: “Application Note No. 167: ESD Protection for Broadband Low Noise Amplifier BGA728L7 for Portable and Mobile TV Applications”