

EiceDRIVER™

High voltage gate drive IC



6ED family - 2nd generation

Technical description

Application Note

AN-EICEDRIVER-6EDL04-1

Rev. 1.3, 2014-03-23

Edition 2014-03-23

**Published by
Infineon Technologies AG
81726 Munich, Germany**

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Revision History	
Rev. 1.3, 2014-03-23	
Page or Item	Subjects (major changes since previous revision)
p. 1	Added classification icon "EiceDRIVER™ Compact"
p. 18	Updated section 3.8

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1 Scope and product family

The 6ED family – 2nd generation is a high voltage gate drive IC for three-phase converters up to a maximum blocking voltage of 600V. The converters can be used for example in drives applications which are basing on induction machines (IM) or brushless DC motors. The 6ED family – 2nd generation is designed in silicon-on-insulator-technology (SOI). This technology provides a high ruggedness against negative voltage spikes and noise.

This application note gives an overview of the technological characteristics. It also describes the most important sections in terms of the application and gives design recommendations for a proper operation of the device in the application. This document covers the following products:

Table 1 Members of 6ED family – 2nd generation

Sales code	control input HIN1,2,3 and LIN1,2,3	UVLO threshold	Bootstrap diode	Package	Optimal for
6EDL04I06NT	negative logic	12.1V/10.2V	Yes	DSO28	IGBT
6EDL04I06PT	positive logic	12.1V/10.2V	Yes	DSO28	IGBT
6EDL04N06PT / 6EDL04N02PR	positive logic	8.9V/8.0V	Yes	DSO28 / TSSOP28	MOSFET
6ED003L06-F2 / 6ED003L02-F2	negative logic	12.1V/10.2V	No	DSO28 / TSSOP28	IGBT, replacement of 1 st generation

It is obvious that the 6ED family covers positive and negative control logic as well as various under voltage lockout levels. The control signals, thresholds and parameters described in this application note must be understood according to the individual part.

Target applications are all cost sensitive applications in the consumer and low end industrial area. All devices are therefore compatible even to microcontrollers with a supply voltage of 3.3 V. 6ED family – 2nd generation is similar to use as IR2136 and its derivatives. It is compatible to the same footprint, but not compatible in terms of the internal thresholds, which may concern the external circuitry. Please refer here to the product specifications of 6ED family – 2nd generation.

2 Technology Characteristics

SOI is the abbreviation of **Silicon-On-Insulator** and is an advanced technique for MOS/CMOS fabrications. It differs from the conventional bulk process by placing the active transistor layer on the top of an insulator, as shown in **Figure 1**.

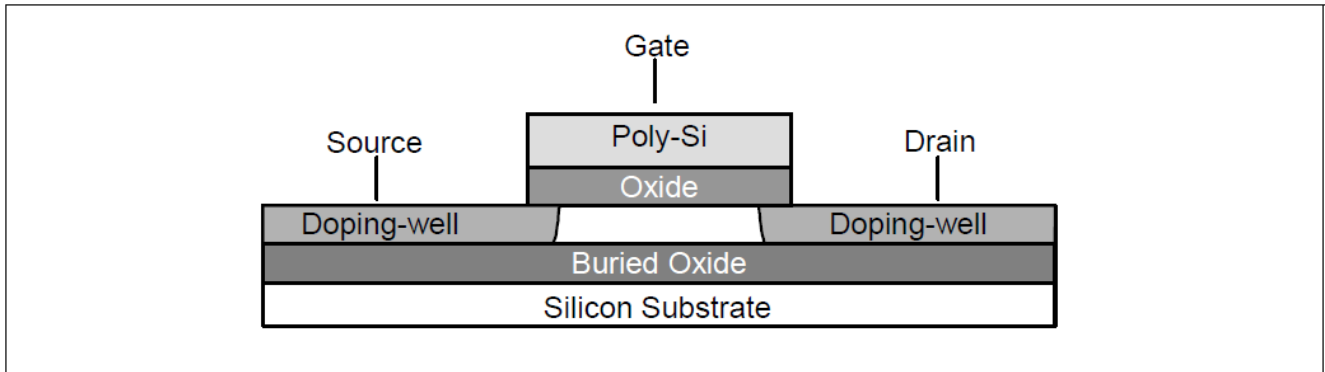


Figure 1 Cross section of a FET in SOI-technology

The silicon is separated by a buried silicon oxide layer to one layer on the top and the other on the bottom. The one on the top, which is the silicon film, is used to produce the transistor and the one on the bottom is used as the silicon substrate. The buried silicon oxide provides an insulation barrier between the active layer and silicon substrate and hence reduces the parasitic capacitance tremendously. Moreover, this insulation barrier disables leakage or latch-up currents between adjacent devices.

A major technological advantage of the Thin-Film-SOI technology is the easy way of lateral insulation of elements inside the silicon film. The thin film technology allows each device to be separated from all other devices by a simple local oxidation (LOCOS) process. Thus, there is no need for CMOS-wells for preventing the "latch-up" effect and reducing the chip size.

The small size of PN-junctions inside the thin silicon film leads to higher switching speed, lower leakage currents and consequently higher temperature stability. In order to obtain a proper body contact for the thin SOI-MOS transistor the channel doping is extended and connected to a common source contact (split source contact). Hence the thin-film SOI-MOS transistor exhibits an anti-paralleled diode that safeguards the device in case of polarity reversal.

In spite of the thin drift regions inside the silicon films, reasonable low on-resistance per area is achieved. This allows a cost effective layout of the output driver transistors.

The SOI technology is also implemented for the 600 V level-shift transistors and high-voltage diodes. The 600V-NMOSFET is based on the low-voltage SOI-NMOSFET structure in conjunction with a very long Drain-extension. The buried oxide insulation barrier cuts off parasitic current paths between substrate and silicon film. This prevents the latch-up effect even in case of high dv/dt switching under elevated temperature and hence provides improved robustness.

Besides these improvements, the thin-film SOI-technology provides additional benefits like lower power consumption and higher immunity to radioactive radiation or cosmic rays.

3 Technical description of the 6ED family – 2nd generation

3.1 General data sheet review

The datasheet of the 6ED family – 2nd generation shows an essential difference to many competitor parts such as [1] or [2] and others. The 6ED datasheets give the absolute maximum ratings referenced to VSS. This is an important aspect, when estimating the robustness of the IC. VSS is the ground reference for the IC as well as for the application and all other parameters vary against this point. All parameters can be measured at any pin with reference to ground, which is VSS and which is the common way of measuring electrical values. Figure 2 shows the fundamental difference between VSS-rated devices and COM-rated devices, which are also available in the market. There are also devices available, which do not give any information about the reference potential at all. A close look to the reference level is therefore highly recommended.

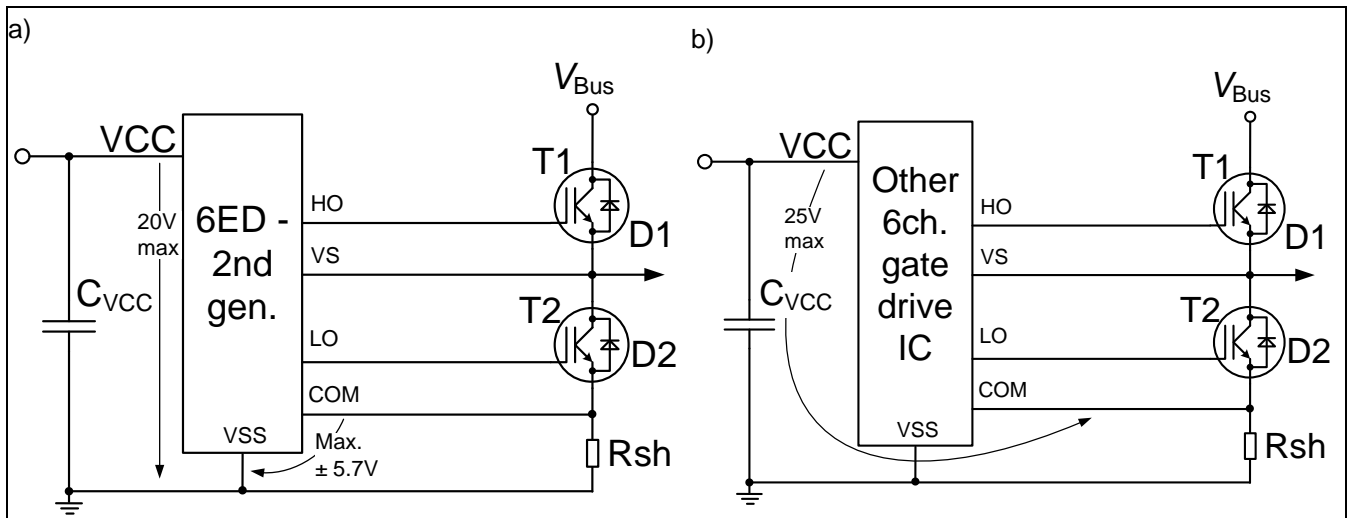


Figure 2 Different reference systems for
a) 6ED family – 2nd generation
b) many other 6channel gate drive IC

There is usually an additional levelshifter designed with a capability of a few volts in order to provide stability for the COM pin. This can be used e.g. for decoupling a shunt from the ground network. However, it is this levelshift structure, which gives another option for the pin COM to float in respect to VSS (=ground of application). The result is that the 6ED family – 2nd generation has another margin of 5.7 V with respect to COM. The relevant maximum rating of 6ED family – 2nd generation in the datasheet on p. 14 are:

- The 6ED family – 2nd generation gives a maximum rating for VCC in respect to VSS (20 V)
- The 6ED family – 2nd generation gives a maximum rating for COM in respect to VSS (± 5.7 V)
- The 6ED family – 2nd generation give a maximum rating for VBSx in respect to VSx (20 V)

One can now calculate a scenario of absolute maximum ratings for a potential COM-rated 6ED device:

$$V_{CC,max}^* = V_{COM} = 25 \text{ V with reference to COM}$$

$$V_{BS,max}^* = V_{BS,max} + V_{COM} = 20\text{V} + 5.7 \text{ V} = 25.7 \text{ V with reference to COM and VS} = \text{VSS}$$

$$V_{S,min}^* = V_{CC,max} - V_{BS,max} - 6\text{V} - V_{COM} = 20\text{V} - 20\text{V} - 6\text{V} - 5.7\text{V} = -11.7\text{V with reference to COM}$$

It is easy to see, that the 6ED family – 2nd generation has same or even higher rated values, when ratings are referenced to pin COM instead of pin VSS. Please note here, that rated values, which are referenced to COM are – if at all – only of little relevance for the application.

3.2 Control input section

All control input pins (HIN, LIN, ITRIP, EN) contain clamping zener diodes. The purpose of these diodes is ESD protection. Therefore they are designed to manage low energy single pulse stresses only. A continuous operation above the absolute maximum ratings is forbidden, such as hard pull-up to voltages above 10 V with a pull-up resistance of 0Ω . However, a soft pull-up up to VCC is allowed, if the input current is less than 1 mA. Please note, that this causes additional losses and must be considered in the losses calculation.

3.2.1 Highside input pins (HIN), Lowside input pins (LIN)

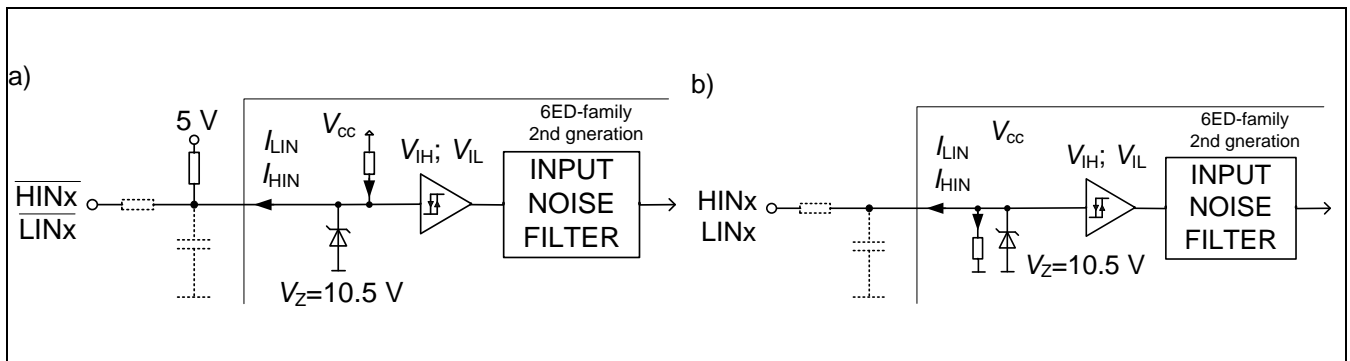


Figure 3 Control input pin structure
a) negative logic
b) positive logic

All gate control input pins are equipped with an integrated zener clamp which is activated, when the input signal is higher than 5.25 V according to Figure 2. It must be guaranteed by application design, that these zener diodes are not overstressed by excessive voltages larger than $V_{IN} = 5.8$ V. The HIGH levels of the input Schmitt-trigger is typically $V_{IH} = 2.1$ V and the LOW level is $V_{IL} = 0.9$ V. This setting of levels provides a full compliance to LSTTL- and CMOS-levels, so that the 6ED family - 2nd generation is compatible to common microcontroller output pins. Some competitor's components do not provide the full compliance to these voltage levels, so that the connectivity to the microcontroller is a major concern. Electromagnetic interference may cause distortions of the control signals, so that a RC-filtering of the input pins can improve the signal integrity of the system. The RC filter must not distort the control signal, so that the edges are still steep. A good design is therefore to use a resistor of 100 Ω and a capacitor of 1 nF. Please note here, that the impedance of the RC filter must follow the I/O-pin specifications of the microcontroller, so that the controller can drive the RC-filter sufficiently.

A) of Figure 3 shows the input structure of the negative logic. The integrated pull-up resistor pulls the inputs to HIGH, if the pin is floating or driven from a high impedance source. The maximum current out of each /HIN- or /LIN-pin is $I_{LIN-} = I_{HIN-} = 200$ μ A, if applying a LOW signal. An external additional pull up resistor can help to obtain a reliable and precise control signal. B) of Figure 3 presents the structure of positive logic. The pull down resistor has a value of typical 5 k Ω . The input bias currents with $I_{LIN+} = I_{HIN+} = 660$ μ A are therefore higher compared to the negative logic

The input noise filter suppresses short pulses and prevents the driven power transistor from excessive switching losses due to linear operation of the switching transistors. The input noise filter time at any control input LIN or HIN is typically $t_{FILIN} = 270$ ns. This means, that an input signal must stay on its level for this period of time in order that the state change is processed correctly according to Figure 4. However, it is recommended to stay above a minimal pulse duration of 1 μ s.

3.2.2 Enable pin (EN)

The signal applied to pin EN controls directly the output sections. All outputs are set to LOW, if this signal is lower than $V_{EN-} = 1.3$ V typically and operation is enabled with signal levels higher than typical $V_{EN+} = 2.1$ V. The internal structure of this pin is similar as b) in Figure 3 except for the switching levels of the Schmitt-Trigger and the pull-down resistor has a value of typ. 75 k Ω . The typical propagation delay time from EN to the output sections is $t_{EN} = 780$ ns.

The IC is steadily enabled, when the EN pin is pulled up to VDD (i.e. +5V / +3.3V). It is not recommended to pull this pin up to VCC (i.e. +15V), because this may lead to an excessive power dissipation in the input structure of this pin and could destroy the IC. This pin can be used as a redundant way to shut down the application in case that a (double) failure occurs or a first shut down mechanism fails by incident.

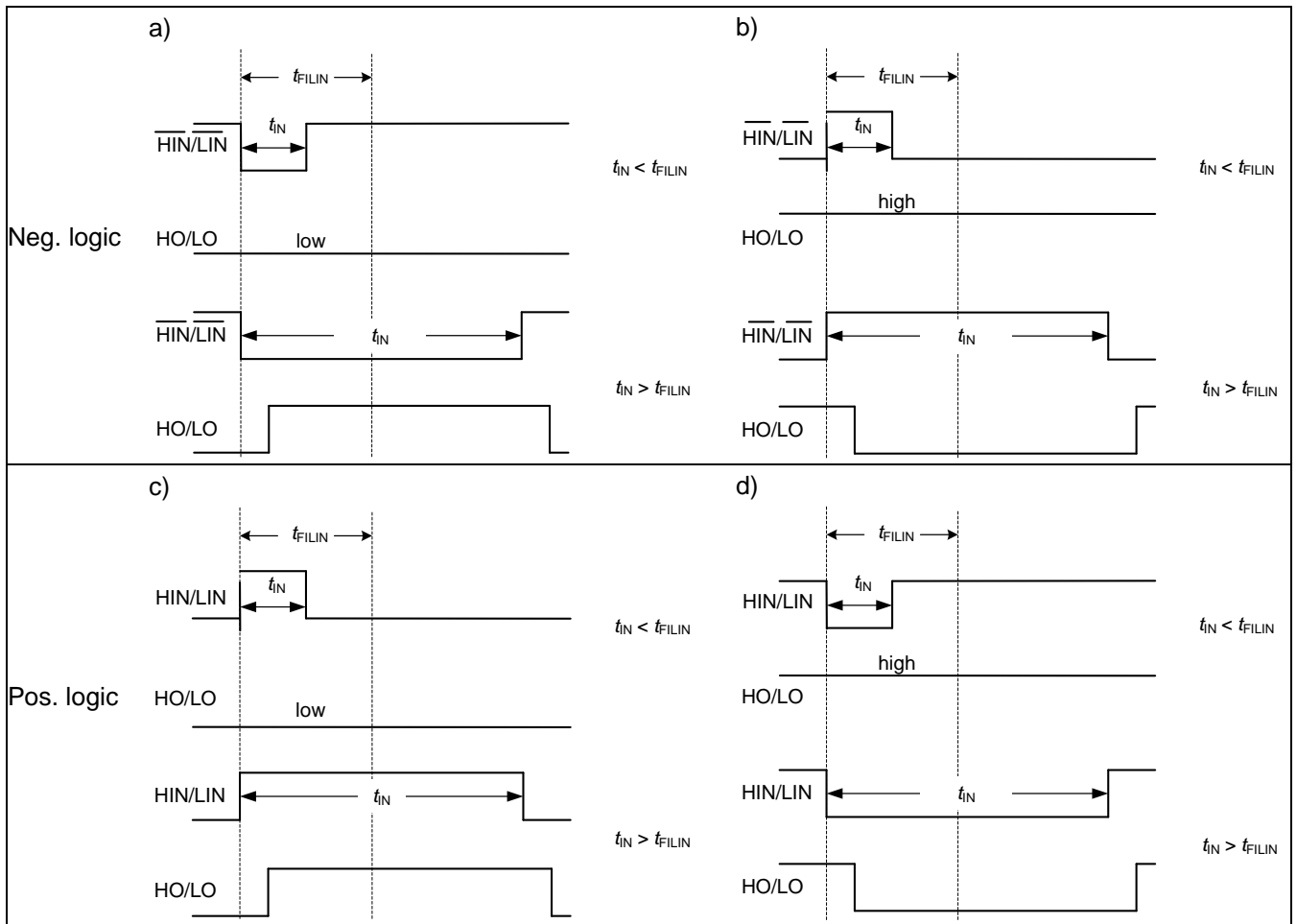


Figure 4 Short pulse suppression (left: short ON pulse; right: short OFF pulse)
 a) and b): negative logic
 c) and d): positive logic

3.3 Control output section (/FAULT)

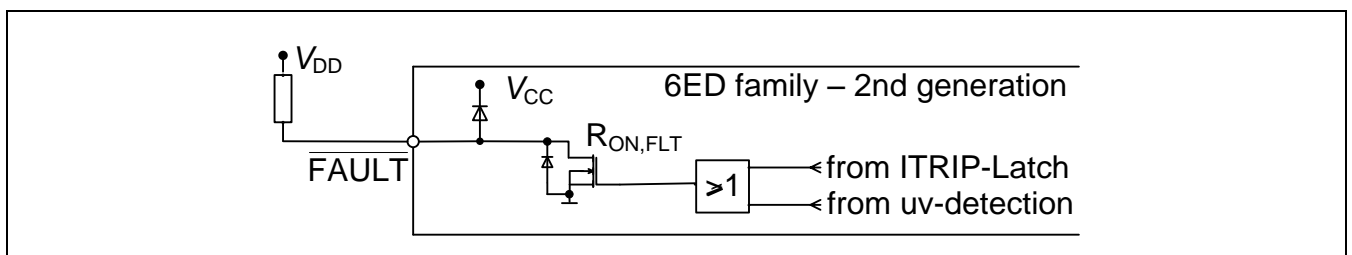


Figure 5 Schematic of the structure of the /FAULT-pin

This pin indicates the failure status of the IC. The level of this pin is LOW in case of undervoltage lockout or triggering of the overcurrent protection. An external pull-up resistor to VDD in the range of a few kΩ (e.g. 4.7 kΩ) is necessary for this open drain pin. The voltage at this pin is internally clamped to VCC, as one can see in the internal structure according to Figure 5. The internal pull-down FET has a typical resistance of $R_{ON,FLT} = 61 \Omega$. The delay time from the triggering event to the change of status at the /FAULT-pin is $t_{FLT} = 450 \text{ ns}$ typically according to the timing diagram shown in Figure 6.

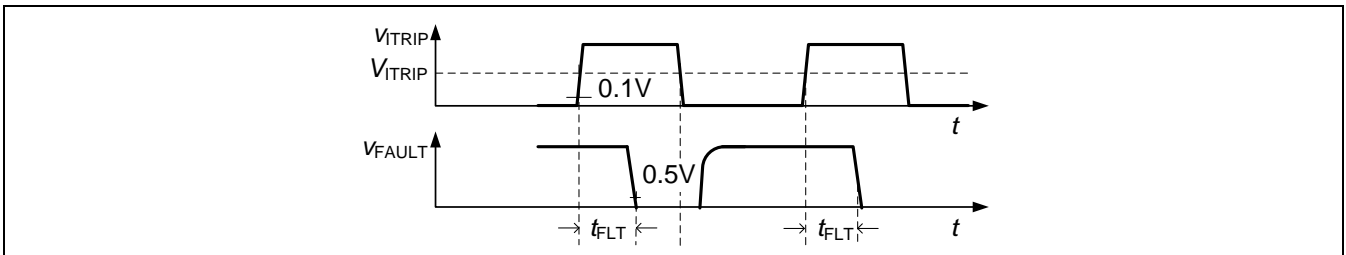


Figure 6 Timing diagramm for ITRIP to FAULT propagation delay

3.4 IC supply section

The 6ED family – 2nd generation supports the operation of IGBT as well as power MOSFET. There is a considerable difference between both types of power transistors in respect of driving their gates. IGBT usually have a gate threshold voltage $V_{GE(th)} = 4.5 \text{ V} \dots 7 \text{ V}$, where power MOSFET have a gate threshold of $V_{GS(th)} = 3 \text{ V} \dots 4 \text{ V}$. As a consequence, MOSFET are usually driven sufficiently with a gate source voltage of $V_{GS} = 10 \text{ V}$ without losing conduction performance, where IGBT need a recommended gate emitter voltage of $V_{GE} = 15 \text{ V}$. This difference is considered in the two different undervoltage lockout (UVLO) levels of the 6ED family – 2nd generation. The absolute maximum rating is in all cases $V_{CC,max} = 20 \text{ V}$ regardless of the undervoltage lockout levels.

The supply voltage of the IC must reach initially at least a typical voltage of V_{CCUV+} and V_{BSUV+} , respectively for the lowside and highside supply, before the IC gets into an operational state. The levels of these parameters are either 11.7 V or 9 V depending on the individual type of the 6ED family. It is recommended to have a margin of at least 1 V in respect to V_{CCUV+} and V_{BSUV+} in order to avoid unintended shut-down caused by noise. The IC shuts down the individual gate sections, when the related supply voltage is below V_{CCUV-} or V_{BSUV-} . The levels here are either 9.8 V or 8.1 V. This prevents the driven transistors from critically low gate voltage levels during on-state and therefore from excessive power dissipation. Please refer to section 3.7.4 for further information.

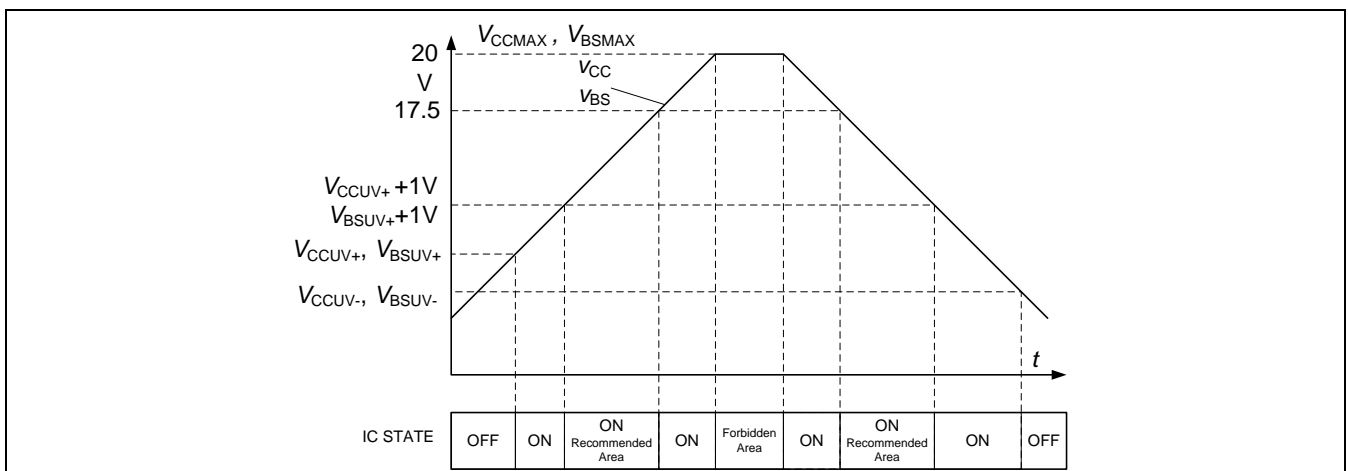


Figure 7 Areas of operation

Figure 8 shows the IC states and the correlated areas of operation concerning the supply voltages for both the lowside supply voltage v_{CC} and the highside supply voltages v_{BS} . There is a forbidden area for supply voltages above 20 V, because here the internal clamping structures begin to break through and the IC is endangered to be damaged by locally excessive power dissipation.

3.5 Gate drive section

3.5.1 Low side gate drive

The lowside gate drive sections contain FET in push-pull configuration. The typical on-state resistance of them is approximately $R_{DS(on),p} = 35 \Omega$ for the turn-on FET (p-channel) and $R_{DS(on),n} = 11 \Omega$ for the turn-off FET (n-channel) according to Figure 8. This results in a typical turn-on current of $I_{O+} = 165 \text{ mA}$ and a typical turn-off current of $I_{O-} = 375 \text{ mA}$. The $R_{DS(on)}$ -values can easily be calculated by means of the parameter V_{OL} , V_{OH} and their test conditions.

There is a levelshift structure included in the 6ED family - 2nd generation in order to allow the potential at pin COM to be negative referenced to pin VSS without forcing substrate current in the IC. This is important, because instantaneous diode forward voltage drop of the low side freewheeling diode can be larger than -0.7 V . Please note here, that this levelshift is not correlated with negative voltage transients of pin VSx referenced to COM.

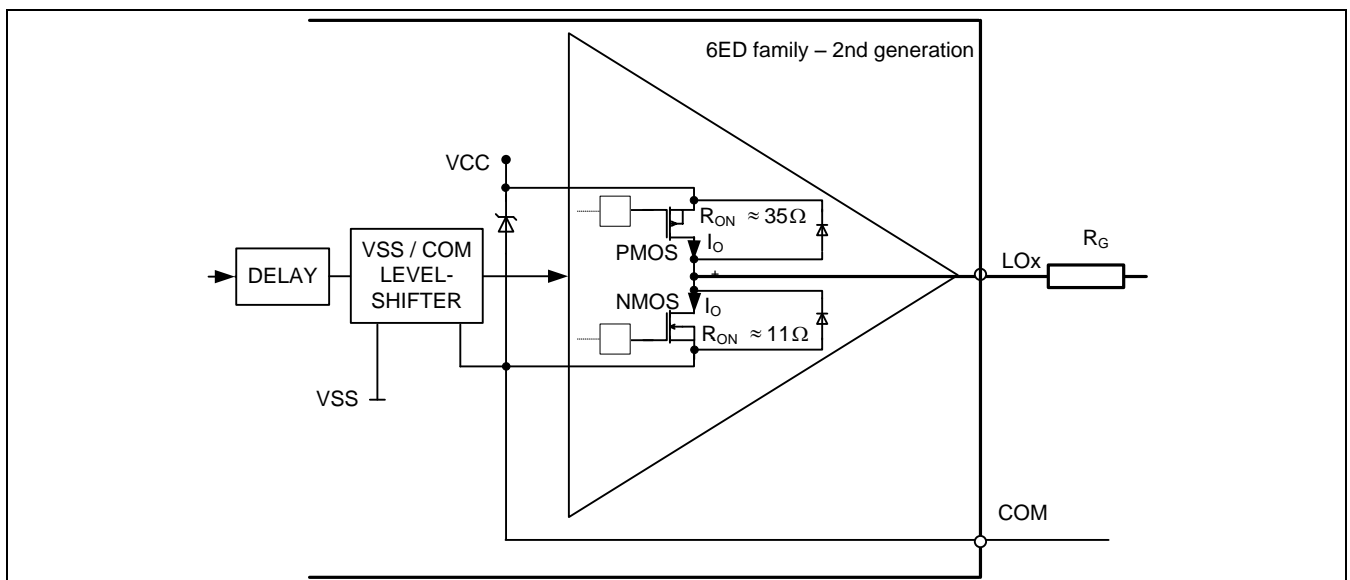


Figure 8 Structure of the lowside gate drive section

The output pins LOx are clamped to the supply voltage VCC of the IC via the reverse diodes of the FET. This prevents the output pins from excessive pulse voltages, which may be coupled into the gate track. There is also an internal zener clamp of the push-pull circuit between COM and VCC.

3.5.2 High side section

The high side gate drive section is shown in Figure 9. The control signal passes the high voltage level shift section and is stored in the gate drive flipflop-latch. The incoming signal as well as the output gate drive signal are clamped internally by integrated diodes to the reference voltage (pin VSx) and the bias voltage (pin VBx), which is identical to the low side sections.

Please note, that there is a parasitic connection from each high side to the low side control area in case of the types 6ED003L06-F2 and 6ED003L02-F2. It must be guaranteed by the design of the individual application, that there are no negative voltages lower than -50 V referred to VSS at pin VS1, VS2 or VS3, which last longer than 500ns according to the maximum rating of the datasheet of 6ED family - 2nd generation.

All other members of the 6ED family – 2nd generation contain an integrated bootstrap diode. Please refer to section 3.6 for further information about the integrated bootstrap diode.

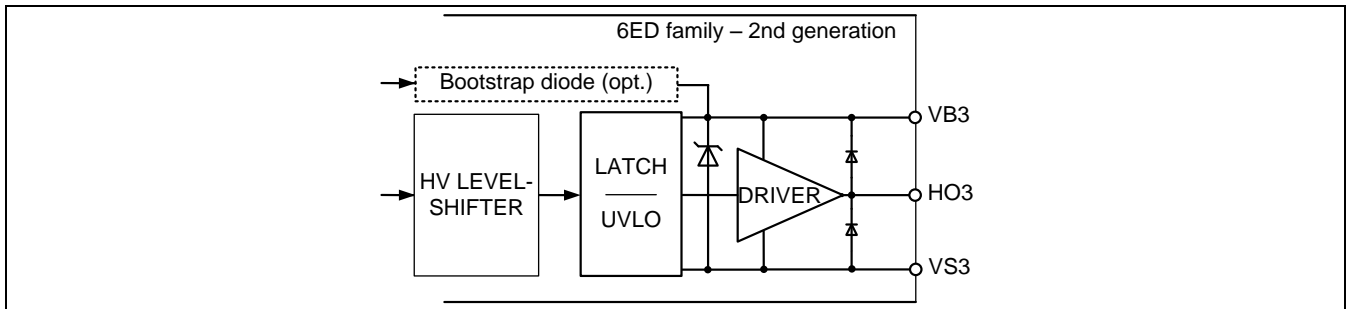


Figure 9 Structure of the lowside gate drive section

3.5.3 Negative Transients at High Side Reference (pin VSx)

The 6ED family - 2nd generation is very robust against negative transient voltages thanks to the inherent oxide insulation of the SOI-technology. Therefore, the minimum voltage at the pins VSx is specified to -50 V for a period of time of 500 ns. This duration is long enough to cover the usual requirement for this stress in drives applications. However, it must be the target of any design to avoid such negative voltages at all.

Parasitic inductances can induce voltages, so that the potential at pins VS1, VS2 or VS3 becomes negative in respect to pin VSS. It is a well known failure mechanism of other driver IC technologies, that these negative voltages force current through the substrate material. The substrate currents can lead to a latch of the high side gate driver, which is then insensitive to any control signal. The result is, that the IGBT are operated in short circuit, which leads to excessive power dissipation and also to system breakdown.

The negative voltage can also increase the pulse current through the external or internal bootstrap diode and may lead to damage. The design target is therefore to avoid such negative transient voltage at all or to keep at least the absolute maximum ratings.

3.6 Bootstrapping

Bootstrapping is a common method of pumping charges from a low potential to a higher one. With this technique a supply voltage for the floating highside sections of the gate drive can be easily established according to Figure 10. This circuit is shown for one of the three half bridges. The current limiting resistor R_{Lim} may be connected to each of the three bootstrap diodes of the three halfbridges.

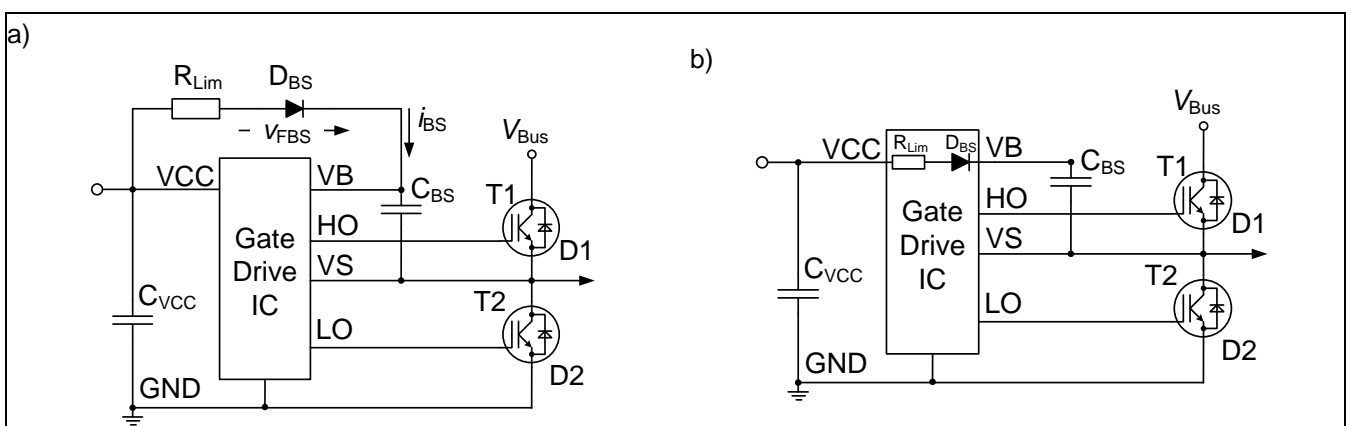


Figure 10 Bootstrap circuit for one halfbridge
a) 6ED003L06-F2 and 6ED003L02-F2
b) others

The first pulse of transistor T2 will force the potential of pin VS to GND. The existing difference between the voltage of the bootstrap capacitor V_{CBS} and V_{CC} results in the charging current i_{BS} into the capacitor C_{BS} . The current i_{BS} is a pulse current and therefore the ESR of the capacitor CBS must be very small in order to avoid losses in the capacitor, that results in lower lifetime of the capacitor.

This pin is on high potential again after transistor T2 is turned off and either T1 or D1 is conducting current. But now the bootstrap diode D_{BS} blocks a reverse current, so that the charges on the capacitor cannot flow back to the capacitor C_{VCC} . The bootstrap diode D_{BS} also takes over the blocking voltage between pin VB and VCC. It is good engineering to choose the same blocking voltage of power transistor T1 and external bootstrap diode. The voltage of the bootstrap capacitor can now supply the highside gate drive sections.

It is a general design rule for the location of bootstrap capacitors C_{BS} , that they must be placed as close as possible to the IC. Otherwise, parasitic resistors and inductances may lead to voltage spikes, which may trigger the undervoltage lockout threshold of the individual highside driver section.

The voltage of bootstrap capacitor is approximately

$$V_{CBS} \approx V_{CC} - V_{FBS} \quad (1)$$

A current limiting resistor R_{Lim} reduces the peak of the pulse current during the turn-on of transistor T2. The pulse current will occur at each turn-on of transistor T2, so that with increasing switching frequency the capacitor C_{BS} is charged more frequently. Therefore a smaller capacitor is suitable at higher switching frequencies. The bootstrap capacitor is mainly discharged by two effects: The highside quiescent current and the gate charge of the transistor to be turned on. The calculation of the bootstrap capacitor results in

$$C_{BS} = \frac{i_{QBS} \cdot t_P + Q_G}{\Delta v_{BS}} \cdot 1.2 \quad (2)$$

with i_{QBS} being the quiescent current of the highside section, t_P the switching period, Q_G the total gate charge and Δv_{BS} the voltage drop at the bootstrap capacitor within a switching period. An additional margin of 20% is added for the case of tolerances for the bootstrap capacitor.

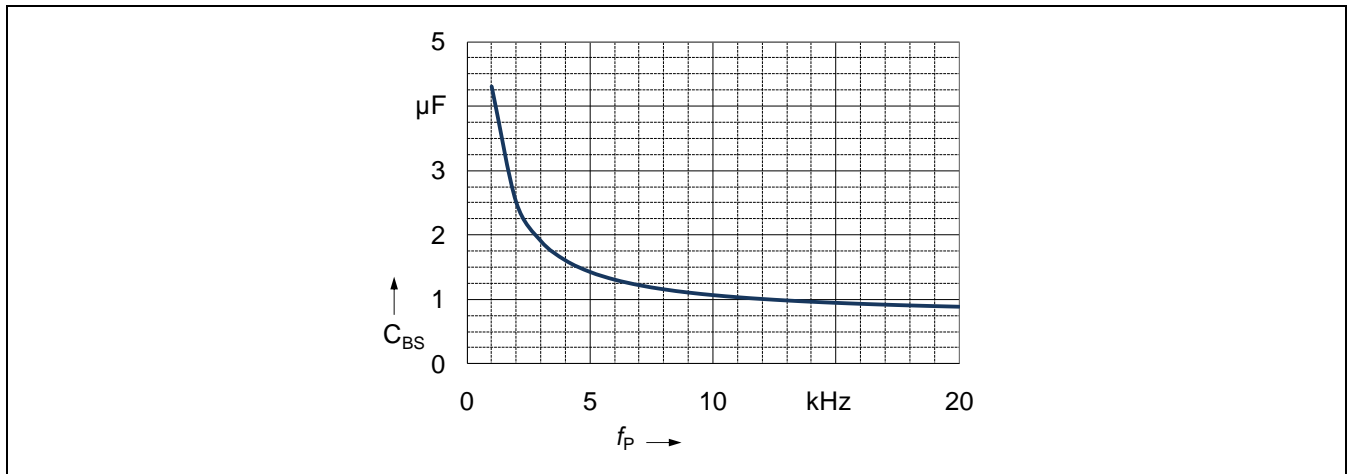


Figure 11 Size of the bootstrap capacitor as a function of the switching frequency f_P for driving IKD10N60R according to equ. (2) with a voltage ripple of 0.1 V

Figure 11 shows the curve corresponding to equ. (2) for a continuous sinusoidal modulation, if the voltage ripple $\Delta v_{BS} = 0.1$ V. The recommended bootstrap capacitance is therefore in the range up to 4.7 μF for most switching frequencies. The performance of the integrated bootstrap diode supports the requirement for small bootstrap capacitances. It is therefore not recommended to exceed a maximum capacitance of $C_{BS} = 47 \mu F$.

Please note here, that equ. (2) is valid for continuous switching operation according to the switching frequency. The use of space vector modulations can cause periods up to 60° (electrical), in which no switching of the low side transistor of a halfbridge occurs and must be considered separately. This effects the bootstrap capacitor size, especially for low output current (motor current) frequencies. In this case the variable t_P must be set to the longest period of no switching.

3.7 Protection

3.7.1 Overcurrent protection (ITRIP)

The current signal of the DC-link reference is measured in order to recognize overcurrent or halfbridge short circuit events. A shunt resistor generates a voltage drop. A small RC-filter for attenuating voltage spikes is recommended. Such spikes may be generated by parasitic elements in the practical layout. It is highly recommended as considerations of good layout to avoid any joint PCB track of the ITRIP signal with the low side emitter track or the COM track (see also section 3.10). If the voltage drop over the shunt is higher than typically $V_{IT,TH+} = 0.445\text{ V}$, then the internal comparator is triggered according to Figure 12. This results in a trigger current of

$$I_{ITRIP} = \frac{V_{IT,TH+}}{R_{SH}} \quad (3)$$

where R_{SH} is the value of the shunt resistor.

The output of the comparator passes a noise filter, which inhibits an overcurrent shutdown caused by parasitic voltage spikes. The typical filter time of the noise filter is $t_{TRIPMIN} = 210\text{ ns}$. A set-dominant latch stores the overcurrent event until it is reset by the signal provided from the RCIN circuit.

The ITRIP-comparator switches the discharging NMOS-FET at pin RCIN. The $R_{DS(on)}$ of the FET is typically $54\ \Omega$, so that there is a characteristic discharge curve in respect of the external capacitor C_{RCin} . The time constant is defined by the external capacitor C_{RCin} and the $R_{DS(on)}$ of the FET. The discharge phase ends, when the comparator is low again. This corresponds to a voltage level at the comparator of $V_{IT,TH+} - V_{IT,HYS} = 445\text{ mV} - 70\text{ mV} = 375\text{ mV}$, where $V_{IT,HYS} = 70\text{ mV}$ is the hysteresis of the ITRIP-comparator.

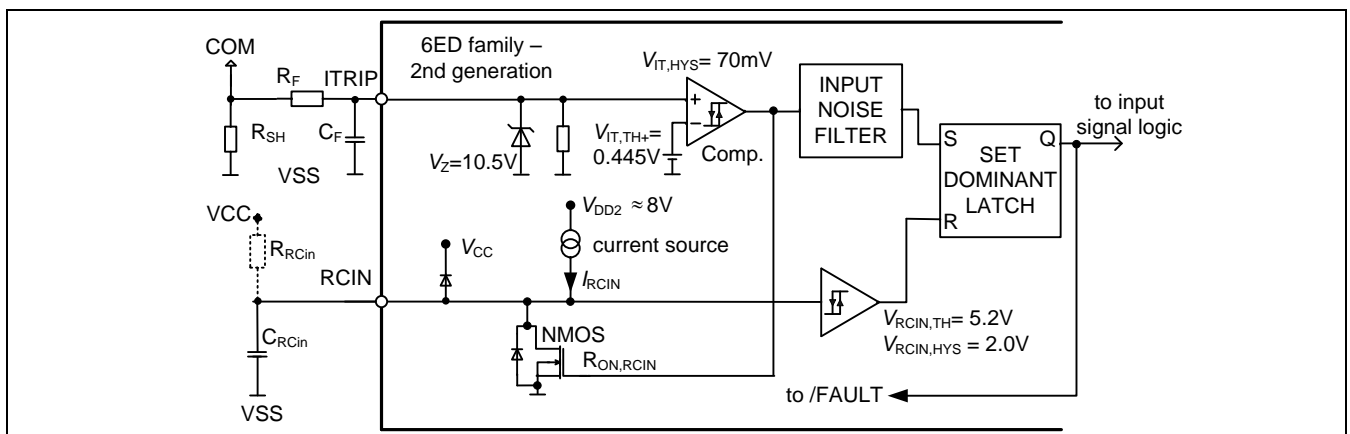


Figure 12 Internal structure of the ITRIP and RCIN sections

It is important to note here, that due to a large external capacitance at pin RCIN and rather short occurrence of overcurrent, the voltage at the capacitor C_{RCin} is not below the threshold of the RCIN Schmitt-Trigger. The threshold of the Schmitt-Trigger $V_{RCIN,TH} - V_{RCIN,HYS} = 5.2\text{ V} - 2\text{ V} = 3.2\text{ V}$ lead to the result, that the set-dominant latch is still in active reset and the IC might restart operation as soon as the voltage at pin ITRIP is in the operative range again, which is $V_{IT,TH+} - V_{IT,HYS}$. If the trigger level at pin ITRIP is set closely to the maximum operative current, then this behaviour acts as a soft overcurrent limitation. As long as the voltage at pin RCIN does not hit the 3.2 V level of the Schmitt-trigger, the gate drive section restarts immediately after the overcurrent vanishes. This may be after some pulse periods.

3.7.2 Failure reset (RCin)

The external circuit at pin RCIN defines the overcurrent recovery of the drive system. This circuit can consist of a single capacitor C_{RCin} according to Figure 12. There is also the option for a path to the supply voltage V_{CC} via resistor R_{RCin} . The fault-clear time t_{FLTCLR} is dependent on the re-charging of C_{RCin} , because the system

recovers, when the threshold of the integrated Schmitt-trigger according to Figure 12 is reached. This means that the resistor to V_{CC} is not mandatory, but it may help to precisely adjust the fault-clear time.

The datasheet specifies the typical fault clear time $t_{FLTCLR} = 1.9$ ms which the current source needs to charge an external capacitor of 1 nF without pull up resistor. This parameter can be scaled linearly to any other capacitor value and results immediately in the according fault clear time. This means that e.g. a 4.7 nF capacitor will realize a fault clear time of $4.7 * 1.9$ ms = 8.9 ms.

The design must guarantee that the voltage at capacitor C_{RCin} reaches the lower threshold of the RCin-Schmitt-trigger for the delay time of the input noise filter at pin ITIRP. It is recommended to reach this threshold within 500ns and to use capacitor values which are smaller than 10nF. Otherwise, the flip-flop releases the gate sections again, so that the IGBT is turned on, which may damage the IGBT.

3.7.3 Deadtime & Shoot Through Prevention

The 6ED family – 2nd generation prevents shoot through and generates a fixed deadtime between the individual IGBT of each half bridge. The deadtime is typically $DT = 310$ ns. However, it is necessary to check the transient times of the driven IGBT. These times are the turn-on delay $t_{d(on)}$, the rise time t_r , the turn-off delay time $t_{d(off)}$ and the fall time t_f . They are defining the timing and the deadtime which is mandatory for the prevention of shoot through. A deadtime of 1 μ s to 1.5 μ s is sufficient for most applications.

3.7.4 Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) of the highside sections act directly on the output gate drive flipflop according to Figure 13, so that an immediate shut down is provided. The UVLO is independent in respect of all three highside gate drive sections. The levels are V_{CCUV+} for the control side and V_{BSUV+} for the high side sections. Please refer to the correct absolute level in respect to the individual type of the 6ED family. Please refer to section 3.4 for further information.

In case of an UVLO shut down of an output section, it is necessary to reach the start-up levels of V_{CCUV+} and V_{BSUV+} again as described in section 3.4. The independent UVLO functions of low and high side sections enable a restart of the affected highside section in case of a bootstrapping supply, because the switch mode operation of the lowside transistor pumps continuously charges into the according bootstrap capacitor, which increases the bootstrap voltage V_{BS} .

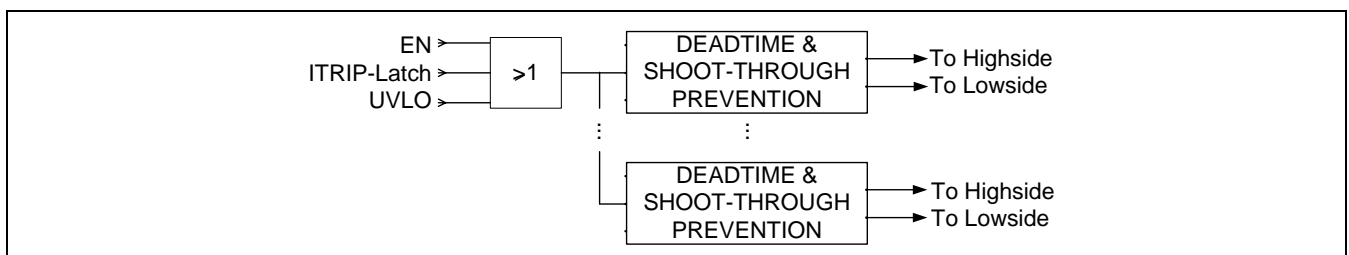


Figure 13 Structure of a lowside UVLO

The UVLO for the lowside gate drive sections is common for all three output circuits and acts on a triple input OR-gate according to Figure 13. The output of this gate is fed into the deadtime and shoot through prevention of the IC. Please note here, that a lowside UVLO is also affecting the highside outputs. Hence, all the gate drives will be shut down in case of a lowside UVLO.

3.8 Calculation of power dissipation and thermal aspects

The 6ED family – 2nd generation is available in two packages, the PG-DSO-28 and the PG-TSSOP-28. Both packages are RoHS compliant. Please refer to section 3.9 for further information in respect to the insulation coordination. It is essential to assure, that the component is not thermally overloaded. This can be checked by means of the thermal resistance junction to ambient and the calculation or measurement of the dissipated power. The thermal resistance is given in the datasheet (section 5) and refers to a specific layout. Changes of this layout may lead to an increased thermal resistance, which will reduce the total dissipated power of the driver IC. One should therefore do temperature measurements in order to avoid thermal overload under application relevant conditions of ambient temperature and housing.

The maximum chip temperature T_j can be calculated with

$$T_j = P_d \cdot R_{th(j\bar{a})} + T_{amb,max} \quad (4)$$

where $T_{amb,max}$ is the maximum ambient temperature.

The dissipated power P_d is a combination of several sources. The following items contribute to the total power dissipation:

- the quiescent current (high side and low side) of the IC (P_{d1VCC} , P_{d1BS})
- the output section (P_{d2on} , P_{d2off})
- the input sections of the IC (P_{d3})
- the leakage losses between any high side section to the control section (P_{d4})

The individual items can be calculated for a worst case by means of the following cooking recipe:

1. Measure the operating current I_{CC} for maximum switching frequency of the application. Connect all three high side control pins and low side control pins and do not connect power transistors.

$$P_{d1VCC} = I_{CC,max} \cdot V_{CC,max} \quad (5)$$

Each high side section generates a continuous power dissipation in respect of the quiescent current. This is given as

$$P_{d1BS} = 3 \cdot I_{QBS} \cdot V_{BS,max} \quad (6)$$

2. Calculate the losses of the output section by means of the total gate charge of the power transistor Q_{Gtot} , the supply voltage V_{CC} , the switching frequency f_P , and the ext. gate resistor. Different cases for turn-on and turn-off must be considered, because many designs use different resistors for turn-on and turn-off. This leads to a specific distribution of losses in respect to the external gate resistor $R_{Gxx,ext}$ and the internal resistance of the output section.

$$P_{d2on} = \frac{6}{2} Q_{G,tot} \cdot V_{CC} \cdot f_P \cdot \frac{36\Omega}{R_{Gon,ext} + 36\Omega} \quad , \text{ for turn-on} \quad (7)$$

$$P_{d2off} = \frac{6}{2} Q_{G,tot} \cdot V_{CC} \cdot f_P \cdot \frac{11\Omega}{R_{Goff,ext} + 11\Omega} \quad , \text{ for turn-off} \quad (8)$$

Both portions P_{d2on} and P_{d2off} together are the output section losses.

3. The input sections generate losses by means of their input structures. These are either pull down resistors (types: 6EDL04I06PT, 6EDL04N06PT, 6EDL04N02PR) or pull up resistor (types: 6EDL04I06NT, 6ED003L06-F2 / 6ED003L02-F2). A duty cycle of 50% is considered:

$$P_{d3neg} = \frac{6}{2} \cdot \left(\frac{(V_{CC} - V_{in})^2 + V_{CC}^2}{70k\Omega} \right) \quad , \text{ for types 6EDL04I06NT, 6ED003L06-F2 / 6ED003L02-F2} \quad (9)$$

$$P_{d3pos} = \frac{6}{2} \cdot \frac{V_{in}^2}{5k\Omega} \quad , \text{ for types 6EDL04I06PT, 6EDL04N06PT, 6EDL04N02PR} \quad (10)$$

4. The leakage losses are given by the current, which crosses the insulation barrier. The relevant parameters are the leakage current I_{LVS} of any high side and the DC bus voltage V_{DC} of the application. The high side section is either on the positive bus potential or at the negative bus potential during operation. It is therefore in principle half the product of these two values. However, there can be a static status of operation, where all three high side sections are on high potential. Thus, we get

$$P_{d4} = 3 I_{LVS} \cdot V_{DC,max} \quad (11)$$

All remaining contributions can be estimated as approximately 20% of the sum of the above mentioned portions. The final power dissipation during operation is then the sum of both contributions

$$P_d = 1.2 (P_{d1VCC} + P_{d1QBS} + P_{d2on} + P_{d2off} + P_{d3} + P_{d4}) \quad (12)$$

The datasheet shows specific layouts, for which the given thermal resistance junction to ambient ($R_{th(j-a)}$) is valid. The thermal resistance which is given in the datasheet is specified for equal operation of all 6 power transistors. It is important to know, that different layouts may lead to different thermal resistances. It is therefore always good engineering praxis to examine additionally the package temperature by experiment.

3.9 Creepage

The clearance distance of the DSO-28 package is 1.52mm according to the package drawing. The related parameter for TSSOP products is 0.7 mm. It depends on the individual application standard, such as [6] or [7], as well as the application conditions, such as pollution degree, etc. to identify the relevant requirements for the system.

The mentioned standards and similar ones describe in detail the relevant considerations for an appropriate calculation of the creepage distance for the target system.

3.10 Layout considerations

Parasitic inductances the ground circuit or in the gate circuits exist by means of PCB track loops. They can lead to oscillations in the according tracks. This can be the root cause of unnormal function of the IC. Figure 14 shows these inductances and track loops.

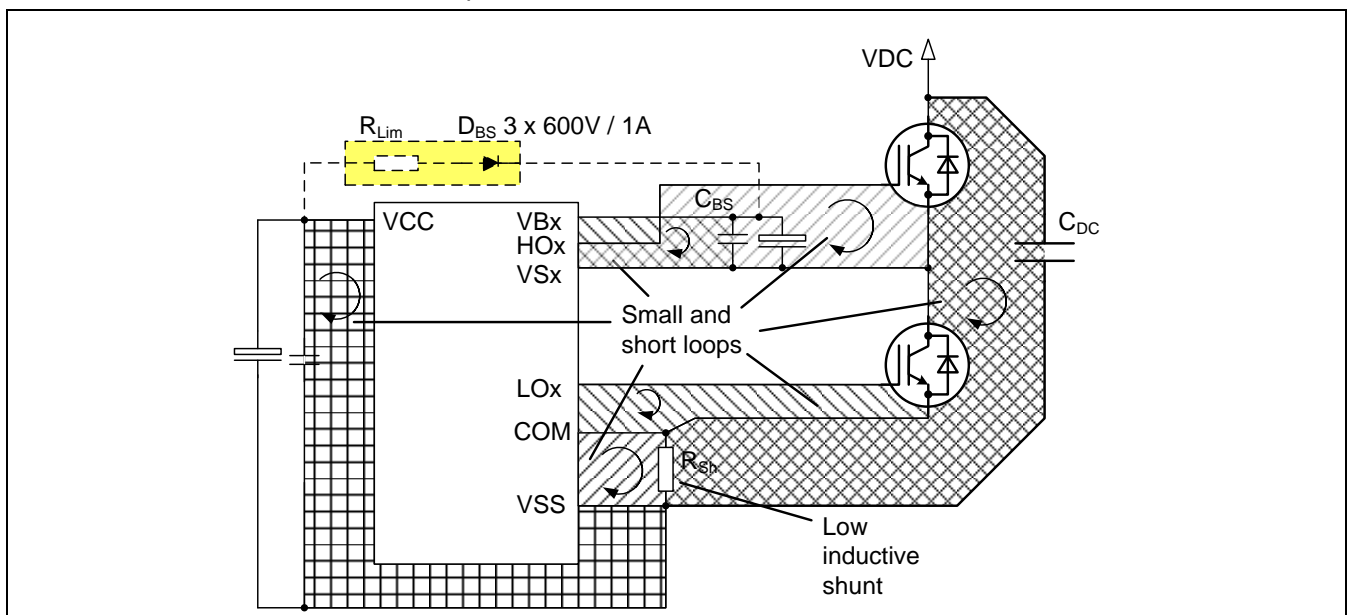


Figure 14 Parasitic inductances in the layout

First of all, the gate tracks, which connect the pins HOx and LOx with the according gate terminal of the power transistor and the tracks connecting the emitter / source terminals of the power transistor with the VSx or COM of the IC must be as short as possible. The area of these tracks must be minimized. This ensures, that the switching speed of the high side transistor and the low side transistor are similar or even equal. The loop, which consists of pin COM, the shunt resistor and pin VSS should be as well minimized. Figure 14 shows the case of a single shunt design. Some systems may use one shunt in each phase of the drive, which is located between source / emitter of the low side transistor and the pin COM. The pin COM and pin VSS are shorted in these cases. The driver IC is usually stabilized by means of a low impedance capacitor, which may be a ceramic type. The loop between pin VCC, the capacitor and VSS should also be as small as possible. This helps to minimize the gate circuit inductances as well as the bootstrap circuit inductances. Figure 14 shows with dashed lines an optional bootstrap circuit, which is mandatory for 6ED003L06-F2 and 6ED003L02-F2. All other types have an integrated bootstrap diode. However, the minimization of this loop is nevertheless important.

A similar consideration must be done for the high side supply circuit. The loop of pins VBx, the bootstrap capacitor C_{BS} , and the pin VS must also be small. Otherwise, there may be inductive voltage drops during the gate charging process of turn-on, which may result in spontaneous undervoltage lockout events at the high side section.

Finally, the inductances of the DC link tracks can be partially cancelled, if one places a low impedance film capacitor between the positive and negative rail closely to the transistor terminals as shown in Figure 14 with C_{DC} .

Glossary and general terms

4 List of used parameters

4.1 General

big letters

small letters

italic letters

upright letters

Time constant parameters

Time varying parameters

physical parameters

components in circuits

Table 2 Used parameters

Parameter	Description	Parameter	Description
<i>A</i>	area	<i>p, P</i>	power
<i>b, B</i>	flux density	<i>r, R</i>	resistance
<i>C</i>	capacitance	<i>t, T</i>	time, time intervals
<i>d, D</i>	duty cycle	<i>v, V</i>	voltage
<i>f</i>	frequency	<i>w, W</i>	energy
<i>i, I</i>	current	η	efficiency
<i>l, L</i>	inductance		
C	capacitor	L	inductor
D	diode	R	resistor
IC	integrated circuit	TR	transformer
AC	alternating current value	i	running variable
avg	average	in	input value
DC	direct current value	max	maximum value
BE	basis-emitter	min	minimum value
C	collector value	off	turn-off / off-state value
E	emitter value	on	turn-on / on-state value
G	gate value	out	output value
P	primary side value	p	pulsed
Pk	peak value		
S	secondary side value		

References

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