EiceDRIVER™

Dual channel 5 A, high-speed, low-side gate driver with high negative input voltage capability and advanced reverse current robustness

Replacement guide

2EDN752x / 2EDN852x

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Application Note

About this document

Scope and purpose

This replacement guide is a step-by-step introduction on how to use the industry pin-out compatible 2EDN752x / 2EDN852x low-side gate drivers as a replacement for other dual LS Drivers on the market.

Intended audience

This document is intended for experienced hardware engineers who already have a basic knowledge of gate drivers.

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1 Introduction

Initial criteria for the designer to consider when selecting a suitable gate driver IC technology will include current capabilities, switching speeds, form factor, level of integration (e.g. how many driver channels are available and what safety features are built in), and how well the process and package technologies are matched to the efficiency and thermal performance requirements of the target application. When exchanging components in such a design, the solution must exactly match these criteria to the original design.

This low-side gate driver provides two independent, non-isolated, low-side gate drivers, each offering a 5 A peak source or sink current. Both channels operate with typical rise and fall times of just 5 ns. Despite the high current, the output stage still offers a very low on resistance, meaning that there is very low power dissipation in the driver even if a very small (or no) external gate resistor is used.

These extended parameters make it possible to replace a wide range of drivers.

2 Description 2EDN752x / 2EDN852x

The 2EDN752x/2EDN852x is an advanced dual-channel driver. It is suited to drive logic and normal level MOSFETs and supports OptiMOS™ , CoolMOS™ , Standard Level MOSFETs, Superjunction MOSFETs, as well as IGBTs and GaN Power devices.

The control and enable inputs are LV-TTL compatible (CMOS 3.3 V) with an input voltage range from -5 V to +20 V. The robustness of the -10 V input pin protects the driver against latch-up or electrical overstress that can be induced by parasitic ground inductances. This greatly enhances system stability.

The 4.2 V and 8 V UVLO (Under Voltage Lock Out) options ensure instant MOSFET and GaN protection under abnormal conditions. Under such circumstances, this UVLO mechanism provides crucial independence if other supervisor circuitries detect abnormal conditions.

Each of the two outputs is able to sink and source 5 A currents utilizing a true rail-to-rail stage. This ensures very low on resistance of 0.7 Ω up to the positive rail and 0.55 Ω down to the negative rail. Very tight channel to channel delay matching, typ. 1 ns, permits parallel use of two channels, leading to a source and sink capability of 10 A. An industry leading reverse current robustness eliminates the need for Schottky diodes at the outputs and reduces the component count and cost.

The pinout of the 2EDN family is compatible with the industry standard footprint. Two different control input options, non-inverted and inverted, offer high flexibility. Three package variants, DSO 8-pin, TSSOP 8-pin, WSON 8-pin, allow optimization of PCB board space usage and thermal characteristics.

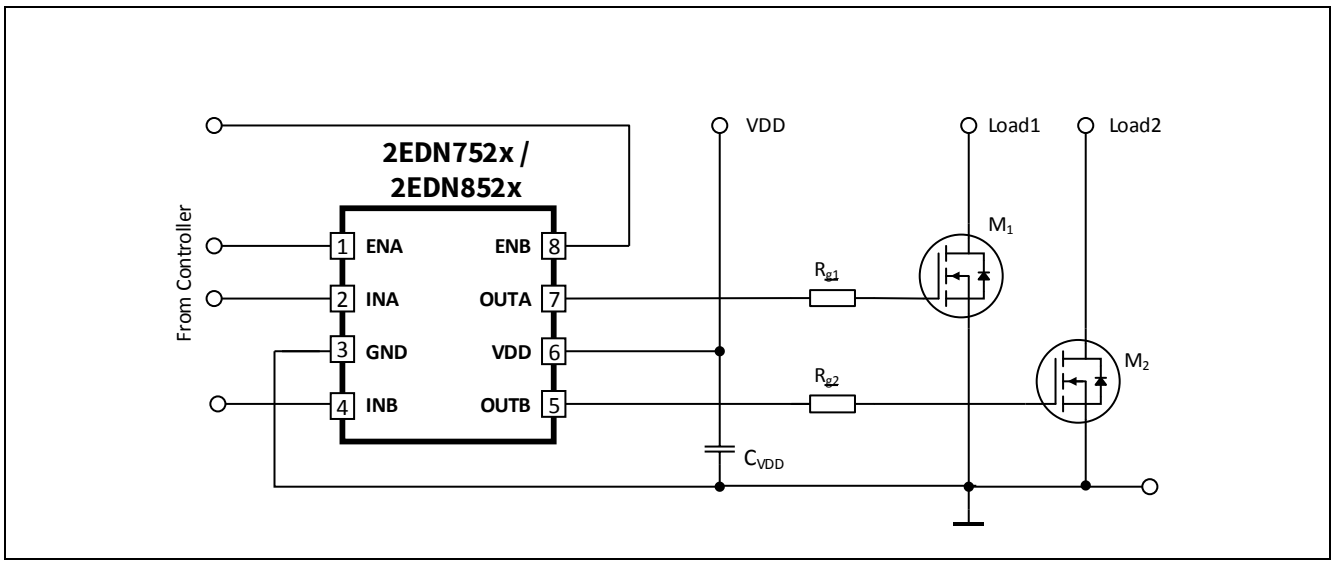

Figure 1 Typical application

3 Replacement step-by-step

3.1 First step: Preparation

Before replacing a device, we recommend to measure and check key parameters in the initial design. In some cases an adjustment after replacement is necessary.

3.1.1 Supply voltage

The maximum supply voltage is 20 V. This high voltage can be valuable in order to exploit the full current capability of 2EDN752x / 2EDN852x when driving very large MOSFETs.

The minimum operating supply voltage is set by the undervoltage lockout function to a typical default value of 4.2 V or 8V. This lockout function protects power MOSFETs from running into linear mode with subsequent high power dissipation.

The 2EDN752x / 2EDN852x have a strong output stage. We recommend a capacitor of > 22 nF close to pin 3 (GND) and pin 6 (VDD).

Please measure power supply parameters at pin 3 (GND) to pin 6 (VDD) as described in table 1.

Table 1 Supply voltage parameter

Parameter	Symbol	Note
Positive supply voltage	V_{VDD}	4.5 V to 20 V; min defined by UVLO
VDD quiescent current	I_{VDDqu1} / I_{VDDqu2}	Power supply has to support more than 0.7 mA under quiescent conditions (no switching).
VDD current max	$I_{VDD\ max}$	Current consumption at VDD pin 6 with max switching frequency and max voltage V_{VDD}

3.1.2 Inputs

The 2EDN752x / 2EDN852x are available in 2 different configurations with respect to the logic configuration of the 4 input pins (input plus enable).

The enable inputs are internally pulled up to a logic high voltage, i.e. the driver is enabled with these pins left open. The standard PWM inputs are internally pulled down to a logic low voltage. This prevents a switch-on event during power up and a non-driven input condition. The version with the inverted PWM input has an internal pull up resistor to prevent unwanted switch-on.

All inputs are compatible with LVTTL levels and provide a hysteresis of 1 V (typ.). This hysteresis is independent of the supply voltage.

All input pins have an extended negative voltage range. This prevents cross current over single wires during GND shifts between signal source (controller) and driver input.

Please measure pin 1 (ENA), pin 2 (INA), pin 4 (INB) and pin 8 (ENB) to pin 3 (GND) as described in table 2.

Table 2 Input parameters

Parameter	Symbol	Note
Input/Enable low level	V_{INL} , V_{ENL}	Max voltage level, inclusive noise floor, should have a space to input voltage threshold for transition high-low. Recommended safety margin to (0.8V) > 200mV
Input/Enable high level	V_{INH} , V_{ENH}	Min voltage level, inclusive noise floor, should have space to input voltage threshold for transition low-high. Recommended safety margin to (2.3V) > 200mV
Input/Enable rise/fall time	T_{INRISE}, T_{INFALL}	If channels A and B run in parallel mode, the rise/fall time has to be faster than 100 ns (10%-90%) to avoid cross current on output stages

3.1.3 Output

The two rail-to-rail output stages realized with complementary MOS transistors are able to provide a 5 A (typ.) sourcing and sinking current. This output stage has shoot through protection and current limiting behavior. The output impedance is very low with a typical value below 0.7 Ω for the sourcing p-channel MOS and 0.5 Ω for the sinking n-channel MOS transistor. The use of a p-channel sourcing transistor is crucial for achieving true rail-to-rail behavior and avoiding a source follower's voltage drop.

Gate Drive Outputs are held active low in the case of floating inputs on ENx, INx or during startup or power down once UVLO is not exceeded. Under all conditions the startup, UVLO or shutdown, outputs are held in defined states.

Often for replacements, the original device could have a different output stage topology internally. This includes different internal impedance, slew rates and timing behavior. It is a good idea to measure the MOSFET gate voltage reaction (B) according to the input signal (A) as described below (see figure 2). Adjusting resistor R_g can bring the signal as close as possible to the original time and slope.

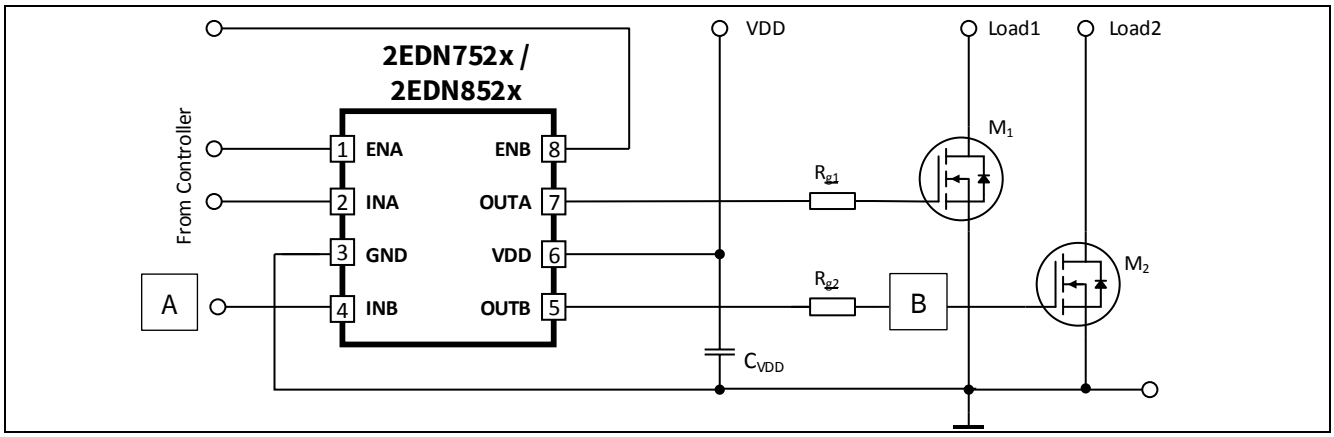

Figure 2 Transfer signal measurement

3.1.4 Footprint

Some original devices have no enable input signals. In this case, pins 1 and 8 need careful observation as described in table 1..

Table 3 Footprint enable pins

Status	Behavior	Note
Pads for pin 1 and 8 are not connected to any network	Floating	No action needed. New device has an internal pull-up resistor (400 k) to enable driver.
Pads for pin 1 and 8 are connected to VDD	Static voltage on Vdd	No action needed. New device is enabled.
Pads for pin 1 and 8 are connected to GND	Static GND potential	Pads or PCB need rework. Without modification, the driver will not enable the output

3.2 Second step: Device selection

3.2.1 Cross reference table

Infineon offers a cross-reference table on the Infineon homepage to help with the first selection.

To use the list, first search for the gate driver currently being used. If the current device is not on the list, then please look for a device which has a parameter set as close as possible to the device being used.

Choose the linked Infineon EiceDRIVER™ from the list.

The cross-reference list is a good starting position with the important parameters, but the datasheet is the final reference for any decision. Once an initial selection is made, please carefully compare the original driver datasheet with the new device datasheet.

- It is recommended to check the package drawings between original device and new device.
- Compare your findings and parametric data from earlier testing with the new device datasheet. Power supply, inputs, outputs, timings and footprint have to be within limits.
- If these parameters are checked, you are ready to move ahead with the right Infineon EiceDRIVER™.

3.3 Third step: Power-up

3.3.1 Before power-up

After carefully reworking and adding a new EiceDRIVER™, please check the parts around the driver as detailed in table 4.

Table 4 Blocking Capacitor and gate resistor

Part	Note
Blocking capacitor between pins 3 and 6	Please use a ceramic capacitor > 22 nF
Gate resistor Rg on each channel	If precise MOSFET timing is necessary, please adjust the gate resistor according the new driver output impedance.

3.3.2 After power-up

Even after the basic checks are complete the application can have feedback from (or interaction with) other components. We recommend controlling all components based upon parametric limits and temperature.

If needed, it is possible to adjust R_g to get the same slew rate on the power MOSFET. This may be needed to fulfill the EMI requirements.

4 Summary

After the changes are completed, the application will normally have a better performance due to the lower losses resulting from faster MOSFET switching and lower output stage impedance.

Finally, it should be noted that as well as the gate driver ICs themselves, Infineon is also providing comprehensive development and prototyping support in the form of application-specific evaluation boards and reference designs. Built around the 2EDNx52x drivers and the new CoolMOS™ C7 600 V MOSFETs, these evaluation and development tools include a 130 kHz 800 W CCM PFC board, a 3.5 kW PFC design, and a halfbridge 600 W LLC board with a 12 V, 50 A output.

[1] References https://www.infineon.com/2EDN

Revision History

Major changes since the last revision

Page or Reference	Description of change
--	First release

www.infineon.com

Edition 2015-10-07

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about any aspect of this document?

Email: erratum@infineon.com

Document reference

AN_2015010_PL52_001

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