EiceDRIVER™ Compact

High voltage gate drive IC

2EDL family

Technical description

Application Note

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1 Scope and product family

The 2EDL family is a high voltage half bridge gate drive IC up to a maximum blocking voltage of 600V. Typical applications are consumer and industrial drives, fans, pumps, induction cooking equipment or switch mode power supplies. The converters can be used for example in drives applications which are basing on induction machines (IM) or brushless DC motors. The 2EDL family is designed in silicon-on-insulator-technology (SOI). This technology provides an excellent ruggedness against negative voltage spikes and noise.

This application note gives an overview of the technological characteristics. It also describes the most important sections in terms of the application and gives design recommendations for a proper operation of the device in the application. This document covers the following products:

Table 1 Members of 2EDL family

Sales Name	EN-/FLT	deadtime & interlock	typ. UVLO-Thresholds	Bootstrap diode	Package
2EDL05I06PF, 2EDL05I06PJ	No	Yes	12.5 V / 11.6 V	Yes	DSO-8 DSO-14
2EDL05I06BF	No	No	12.5 V / 11.6 V	Yes	DSO-8
2EDL05N06PF 2EDL05N06PJ	No	Yes	9.1 V / 8.3 V	Yes	DSO-8 DSO-14
2EDL23I06PJ	Yes	Yes	12.5 V / 11.6 V	Yes	DSO-14
2EDL23N06PJ	Yes	Yes	9.1 V / 8.3 V	Yes	DSO-14

The 2EDL family provides positive control logic as well as different under voltage lockout levels for MOSFET and IGBT. The pin designations, control signals, thresholds and parameters described in this application note must be understood according to the individual part.

In this application note, the parameter values for 2EDL 0.5A version (2EDL05I06PF, 2EDL05I06PJ, 2EDL05I06BF, 2EDL05N06PF and 2EDL05N06PJ) are referred to 2EDL 0.5A datasheet, and the parameter values for 2EDL 2.3A version (2EDL23I06PJ and 2EDL23N06PJ) are referred to 2EDL 2.3A datasheet.

Target applications are all cost sensitive applications in the consumer and low end industrial area. All devices are therefore compatible even to microcontrollers with a supply voltage of 3.3 V. The 2EDL is compatible to the same footprint as a number of other gate drive IC in the market. Nevertheless, many features are built in, which provide an add-on value to the application. Please refer here also to the product specifications of 2EDL family.

2 Technology Characteristics

SOI is the abbreviation of **S**ilicon-**O**n-**I**nsulator and is an advanced technique for MOS/CMOS fabrications. It differs from the conventional bulk process by placing the active transistor layer on the top of an insulator, as shown in **Figure 1**.

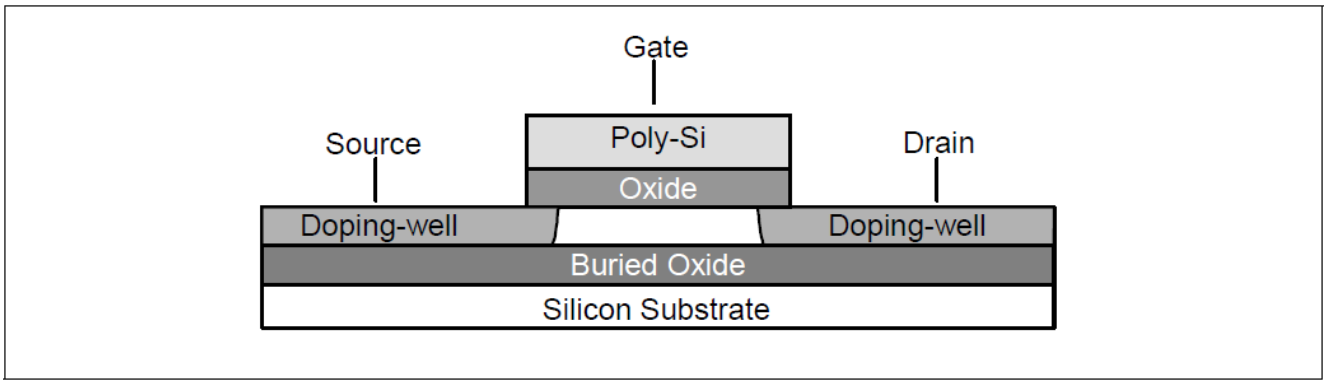

Figure 1 Cross section of a FET in SOI-technology

The silicon is separated by a buried silicon oxide layer to one layer on the top and the other on the bottom. The one on the top, which is the silicon film, is used to produce the transistor and the one on the bottom is used as the silicon substrate. The buried silicon oxide provides an insulation barrier between the active layer and silicon substrate and hence reduces the parasitic capacitance tremendously. Moreover, this insulation barrier disables leakage or latch-up currents between adjacent devices.

A major technological advantage of the Thin-Film-SOI technology is the easy way of lateral insulation of elements inside the silicon film. The thin film technology allows each device to be separated from all other devices by a simple local oxidation (LOCOS) process. Thus, there is no need for CMOS-wells for preventing the "latch-up" effect and reducing the chip size.

The small size of PN-junctions inside the thin silicon film leads to higher switching speed, lower leakage currents and consequently higher temperature stability. In order to obtain a proper body contact for the thin SOI-MOS transistor the channel doping is extended and connected to a common source contact (split source contact). Hence the thin-film SOI-MOS transistor exhibits an anti-paralleled diode that safeguards the device in case of polarity reversal.

In spite of the thin drift regions inside the silicon films, reasonable low on-resistance per area is achieved. This allows a cost effective layout of the output driver transistors.

The SOI technology is also implemented for the 600 V level-shift transistors and high-voltage diodes. The 600V-NMOSFET is based on the low-voltage SOI-NMOSFET structure in conjunction with a very long Drain-extension. The buried oxide insulation barrier cuts off parasitic current paths between substrate and silicon film. This prevents the latch-up effects in case that the voltage at any pin is either negative or exceeds the supply voltage $V_{DD.}$ Even in case of high dv/dt switching or under elevated temperature the IC operates stable and hence provides improved robustness.

Besides these improvements, the thin-film SOI-technology provides additional benefits like lower power consumption and higher immunity to radioactive radiation or cosmic rays.

3 Technical description of the 2EDL family

3.1 Control input section

All control input pins (HIN, LIN, PGND, EN) contain clamping diodes to the supply voltage VDD. The purpose of these diodes is ESD protection. Therefore they are designed to manage low energy single pulse stresses only. A continuous operation above the absolute maximum ratings is forbidden. A hard pull-up to the supply voltage VDD with a pull-up resistance of 0 Ω is possible, but it injects additional power dissipation into the IC. Please note, that this causes additional losses and must be considered in the losses calculation.

3.1.1 High side input pins (HIN), Low side input pins (LIN)

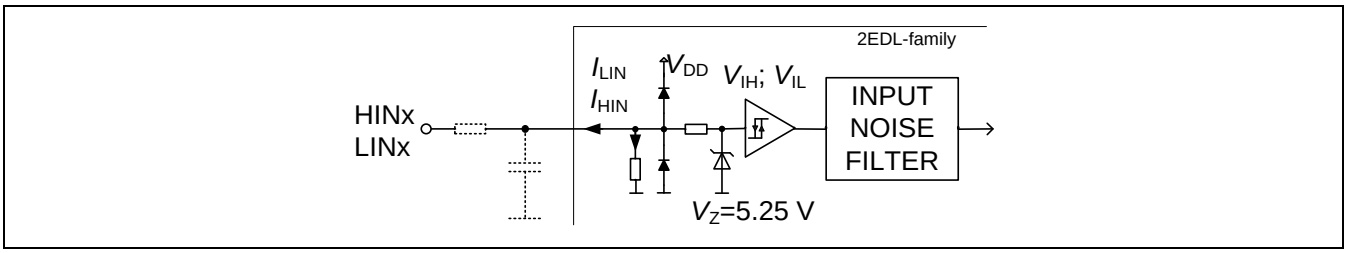

Figure 2 Control input pin structure

All gate control input pins are equipped with an integrated diode clamp which is activated, when the input signal is higher than the voltage at pin VDD according to Figure 2. It must be guaranteed by application design, that these diodes are not overstressed by excessive voltages larger than VDD. Anyway, voltage spikes by crosstalk or other low-energetic injections can be clamped to VDD. Please note that the integrated zener diode is decoupled by a series resistor and is for internal protection than for protection against overvoltages. The HIGH levels of the input Schmitt-trigger is typically V_{IH} = 2.1 V and the LOW level is V_{IL} = 0.9 V. This setting of levels provides a full compliance to LSTTL- and 3.3V-CMOS-levels, so that the 2EDL family is compatible to common microcontroller output pins. Some competitor's components do not provide the full compliance to these voltage levels, so that the connectivity to the microcontroller is a major concern. Electromagnetic interference (EMI) may cause distortions of the control signals, so that a RC-filtering of the input pins can improve the signal integrity of the system. The RC filter must not distort the control signal, so that the edges are still steep. A good design is therefore to use a resistor of 100 Ω and a capacitor of 1 nF. Please note here, that the impedance of the RC filter must follow the I/O-pin specifications of the microcontroller, so that the controller can drive the RC-filter sufficiently.

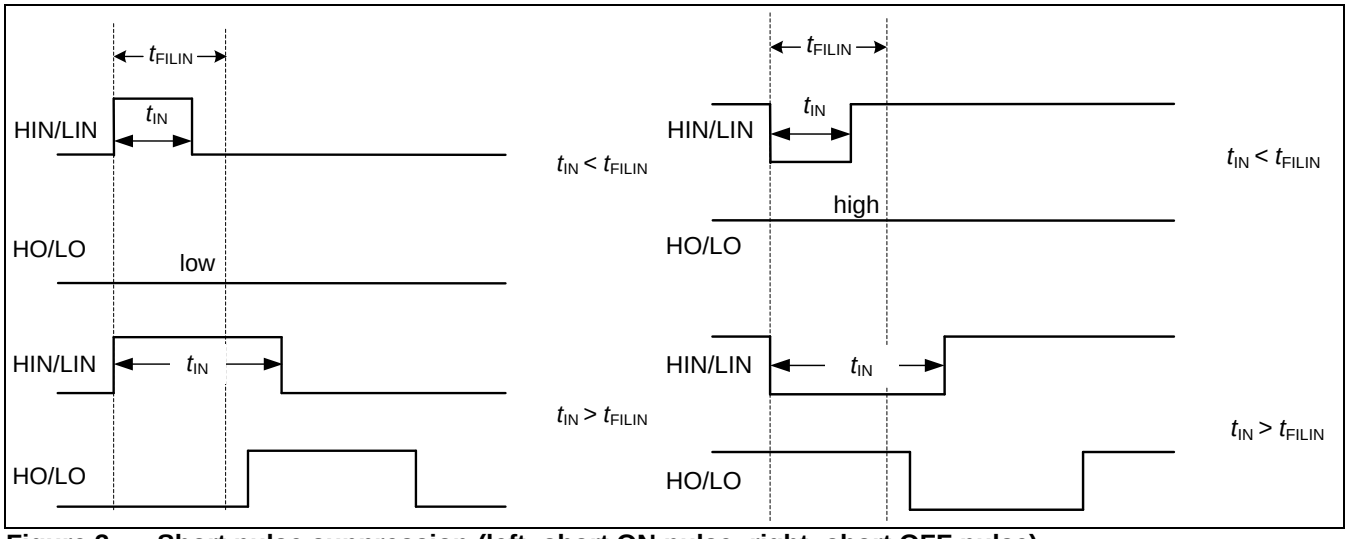

Figure 3 Short pulse suppression (left: short ON pulse; right: short OFF pulse)

Both input sections (HIN and LIN) contain as well a pull-down resistor. However, this resistor is high-ohmic (approx. 100 kΩ) and is considered as a protection against PCB track cracks, so that the device keeps its outputs off in these cases.

The input noise filter suppresses short pulses and prevents the driven power transistor from excessive switching losses due to linear operation of the switching transistors. The input noise filter time at input LIN or HIN is about t_{FILIN} =190 ns for IGBT types. For MOSFET types, it is 100ns for high side input HIN and 150ns for low side input LIN. This means, that an input signal must stay on its level for this period of time in order to process the state change correctly according to Figure 3. Please note, that there is a slightly higher signal distortion between input and output, when the input pulse duration is similar as the filter time. However, it is recommended for IGBT anyway to stay above a minimal pulse duration of 0.8 µs in order to obtain the specified behavior of the IGBT.

Please note that unused input pin (LIN or HIN) must be biased to GND for safety consideration.

3.1.2 Enable and fault pin (EN-/FLT, 2EDL23x06PJ only)

This pin is available for 2EDL23x06PJ devices only. It is a bidirectional open drain output pin, which can shut down the IC in input mode and which indicates either under voltage lockout (UVLO) or overcurrent in output mode.

The signal applied to pin EN controls directly the output sections, when used in input mode. All outputs are set to LOW, if this signal is lower than V_{EN-} = 0.9 V typically and operation is enabled with signal levels higher than typical V_{EN+} = 2.1 V. The internal structure of this pin is similar as b) in Figure 2. The pull-down resistor has a value of typ. 73 kΩ. The typical propagation delay time from EN to the output sections is t_{EN} = 550 ns.

The IC is steadily enabled, when the EN pin is pulled up to the logic section supply voltage (i.e. +5V / +3.3V). In this case, an external pull-up resistor (R_{pu} in Figure 4) in the range of a few kΩ (e.g. 4.7 kΩ) is necessary to bias this open drain pin. It is recommended to use a pull-up resistor of min. 20kΩ, when pulling up this pin to VDD (i.e. +15V). This pin can also be used as a redundant way to shut down the application in case that a (double) failure occurs or a first shut down mechanism (e.g. PGND) fails by incident.

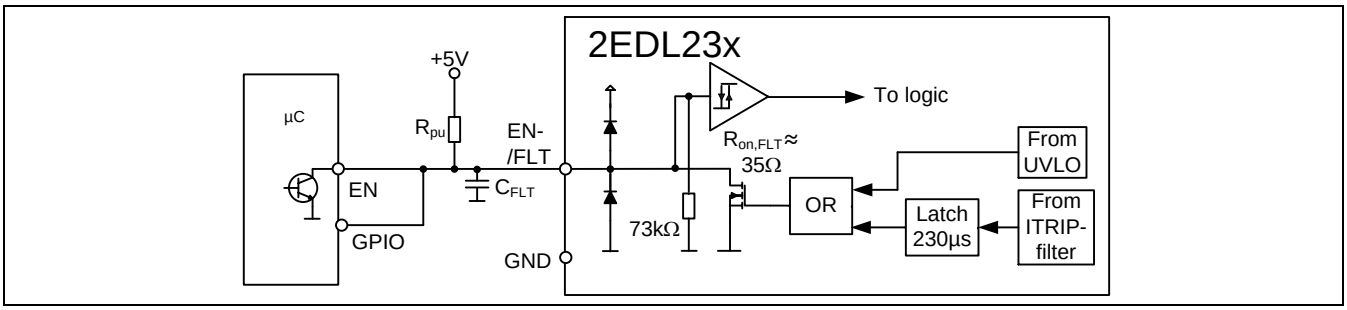

Figure 4 Schematic of the structure of the EN-/FLT pin

This pin indicates the failure status of the IC. The level of this pin is LOW in case of undervoltage lockout or triggering of the overcurrent protection. The voltage at this pin is internally clamped to VDD, as one can see in the internal structure according to Figure 4. The internal pull-down FET has a typical resistance of $R_{on,FLT}$ = 35 Ω. The delay time from the overcurrent trigger event to the change of status at the EN-/FLT-pin is t_{FLT} = 2.1 µs typically according to the timing diagram shown in Figure 5.

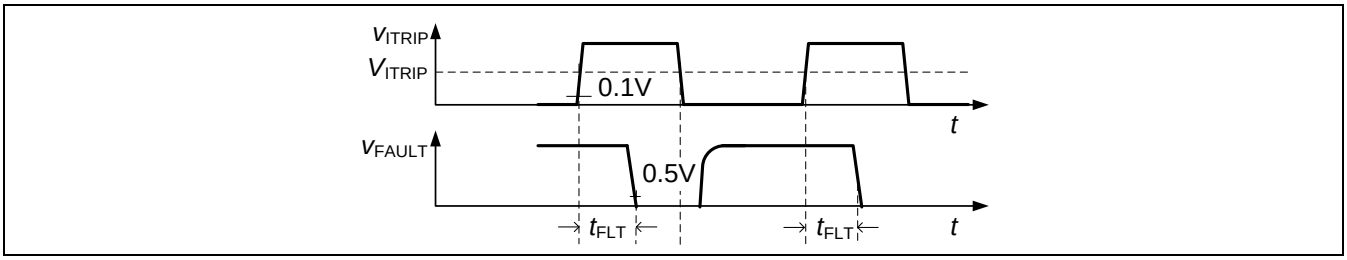

Figure 5 Timing diagram for ITRIP to FAULT propagation delay

3.2 IC supply section

The IC is supplied by the pins VDD and GND for the input side and the pins VB and VS for the high side section.

The 2EDL family supports the operation of IGBT as well as power MOSFET. There is a considerable difference between both types of power transistors in respect of driving their gates. IGBT usually have a gate threshold voltage $V_{GE(th)}$ = 4.5 V … 5 V, where power MOSFET have a gate threshold of $V_{GS(th)}$ = 3 V … 4 V. As a consequence, MOSFET are usually driven sufficiently with a gate source voltage of V_{GS} = 10 V without losing conduction performance, where IGBT need a recommended gate emitter voltage of V_{GE} = 15 V. This difference is considered in the two different undervoltage lockout (UVLO) levels of the 2EDL family. The absolute maximum rating is in all cases $V_{DD,max}$ = 20 V regardless of the undervoltage lockout levels. Please note that the decoupling capacitor for the driver IC supply should be put as close as possible to the supply pins (VDD and VB), it should be ceramic type and µA range is expected as minimum.

3.2.1 IGBT types

The supply voltage V_{DD} of the IC must reach initially at least a typical voltage of V_{DDUV+} for the low side (input side) and V_{BSUV+}, respectively for the high side supply, before the IC gets into an operational state. The levels are asymmetric, which has advantages for bootstrapping when using the integrated bootstrap diode. The levels of these parameters are V_{DDUV+} = 12.5 V and V_{BSUV+} = 11.6 V according to Figure 6. It is recommended to have a margin of at least 1 V in respect to V_{DDUV+} and V_{BSUV+} in order to avoid unintended shut-down caused by noise. The shutdown levels of the UVLO function are also asymmetric. The IC shuts down the individual gate sections, when the related supply voltage is below typ. V_{DDUV-} = 11.6 V or typ. V_{BSUV-} = 10.7 V. This prevents the driven transistors from critically low gate voltage levels during on-state and therefore from excessive power dissipation. Please refer to section 3.5.3 for further information.

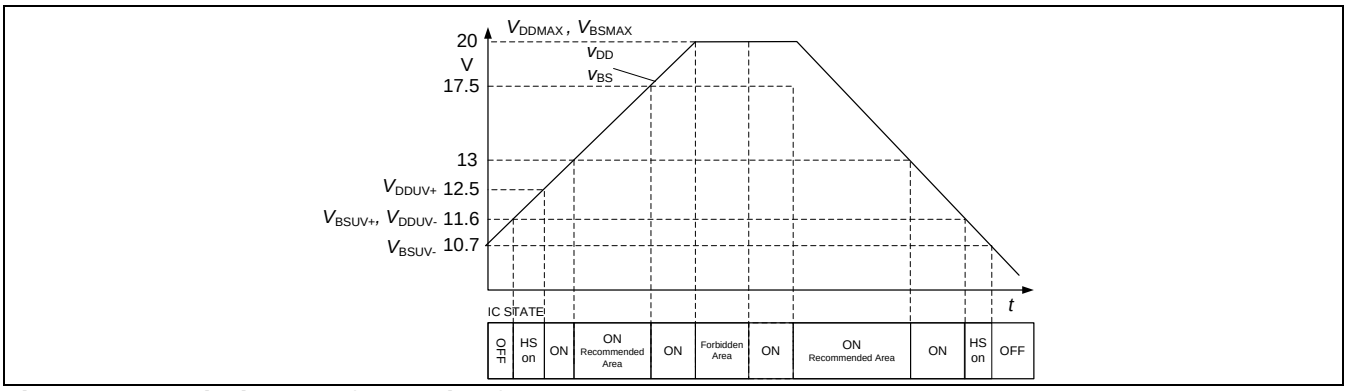

Figure 6 Typical areas of operation for IGBT types

3.2.2 MOSFET types

MOSFET types do not have the asymmetric UVLO levels. The turn-on levels of the UVLO function are V_{DDUV+} = V_{BSUV+} = 9.1V for the low side and high side supply. The IC shuts down the individual gate sections, when the related supply voltage is below V_{DDUV-} = V_{BSUV-} = 8.3 V. Please refer to section 3.5.3 for further information.

Figure 7 shows the IC states and the correlated areas of operation concerning the supply voltages for both the low side supply voltage V_{DD} and the high side supply voltages v_{BS}. There are different limits for IGBT and MOSFET type driver IC. The forbidden area is for supply voltages above 20 V, because here the internal clamping structures begin to break through and the IC is endangered to be damaged by locally excessive power dissipation.

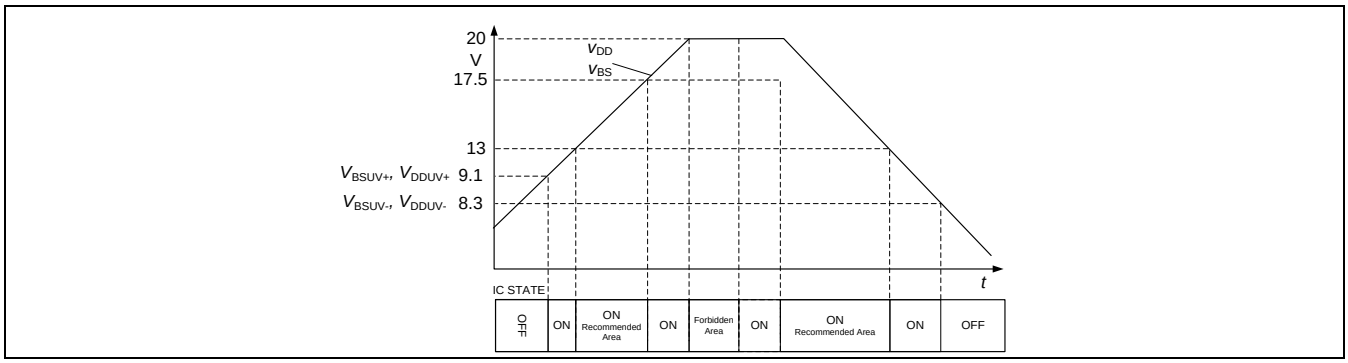

Figure 7 Typical areas of operation for MOSFET types

3.3 Output sections

3.3.1 Low side gate drive

The low side gate drive sections contain FET in push-pull configuration. The source transistor is p-channel type and the sink transistor is n-channel type, so that rail-to-rail behavior is implemented. The typical turn-on current is I_{O+} = 230 mA and a typical turn-off current of I_{O-} = 480 mA for the 0.5A types. The versions with large output currents have typically I_{O+} = 1800 mA and a typical turn-off current of I_{O-} = 2300 mA. There is a level shift structure included in the 2EDL family between PGND and GND levels in order to allow a proper gate drive referenced to pin PGND (2EDL23x06PJ) or GND (others).

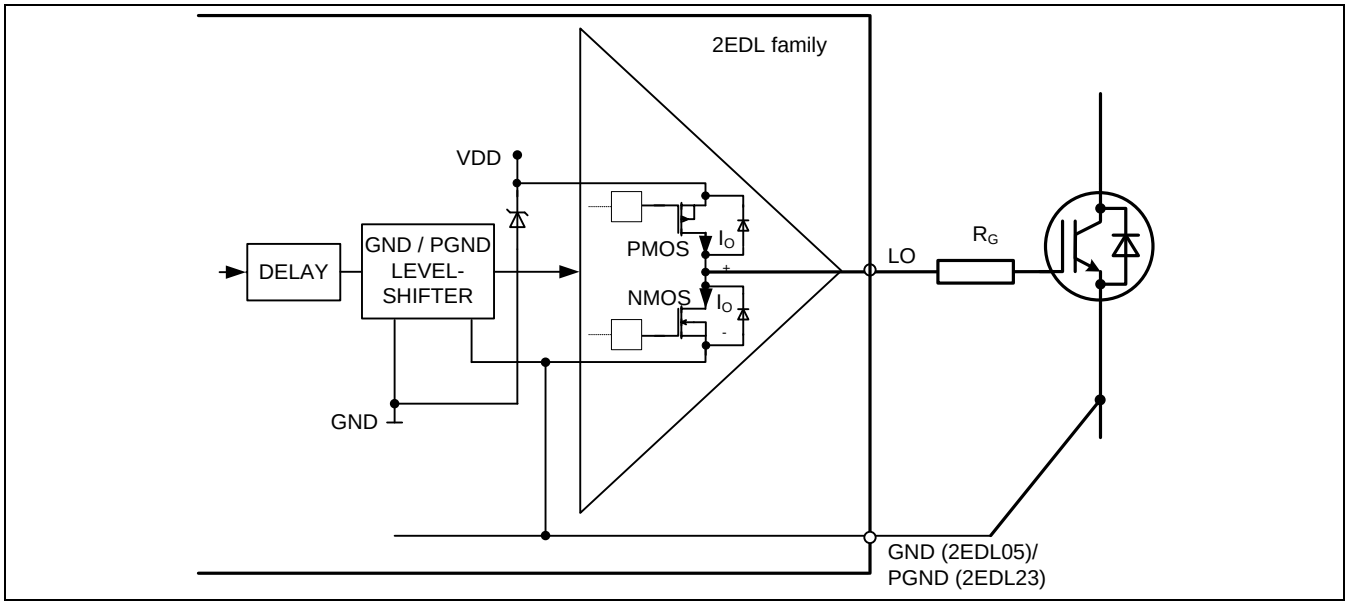

Figure 8 Structure of the low side gate drive section

The output pin LO is clamped to the supply voltage VDD of the IC via the body diodes of the FET. This prevents the output pins from excessive pulse voltages, which may be coupled into the gate track. There is also an internal zener clamp of the push-pull circuit between GND and VDD.

3.3.2 High side section

The high side gate drive section is shown in Figure 9. The control signal passes the high voltage level shift section and is stored in the gate drive flip-flop latch. The output gate drive signal HO is clamped internally by integrated diodes to the reference voltage (pin VS) and the bias voltage (pin VB), which is identical to the low side sections.

Please note, that there is a parasitic connection from high side to the low side control area. It must be guaranteed by the design of the individual application, that there are no negative voltages lower than -50 V referred to GND at pin VS, which last longer than 500ns according to the maximum rating of the datasheet of 2EDL family. The negative voltages can also affect the signal transmission over the level shift structure. There is no signal transmission possible, when the voltage at pin VB is smaller than 7V with reference to GND, i.e. V_{BGND} < 7.0 V.

All members of the 2EDL family contain an integrated bootstrap diode. Please refer to section 3.4 for further information about the integrated bootstrap diode.

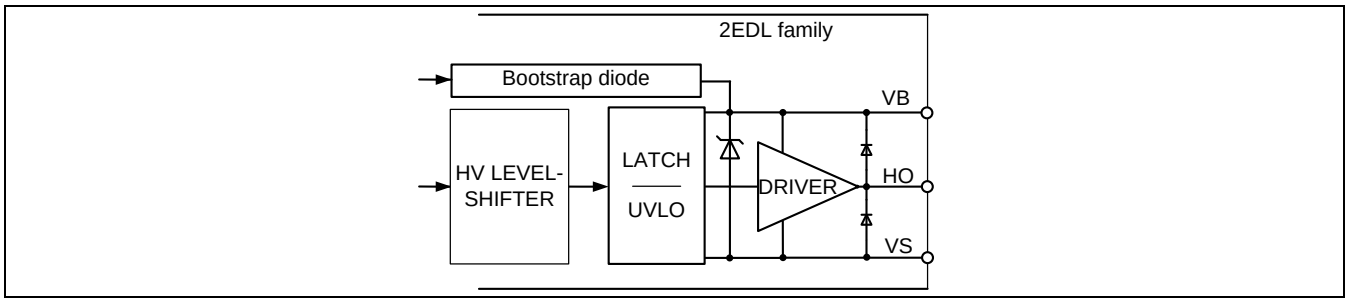

Figure 9 Structure of the low side gate drive section

3.3.3 Negative transients at high side reference (pin VS)

The 2EDL family is very robust against negative transient voltages thanks to the inherent oxide insulation of the SOI-technology. Therefore, the minimum voltage at the pins VS is specified to -50 V for a period of time of 500 ns. This duration is long enough to cover the usual requirement for this stress in drives and switch mode power supply applications. However, it must be the target of any design to avoid such negative voltages at all.

Parasitic inductances can induce voltages, so that the potential at pin VS becomes negative in respect to pin GND. It is a well-known failure mechanism of other driver IC technologies that these negative voltages force current through the substrate material. The substrate currents can lead to a latch of the high side gate driver or other malfunction, which is then insensitive to any control signal. The result is, that the IGBT are operated in short circuit, which leads to excessive power dissipation and also to system breakdown.

The negative voltage can also increase the pulse current through the internal bootstrap diode or to an increased / excessive bootstrap voltage in general. The design target is therefore to avoid such negative transient voltage at all or to keep at least the absolute maximum ratings.

3.4 Bootstrapping

3.4.1 Temperature stability of bootstrap diode and application range

All parts of the 2EDL family contain integrated bootstrap diodes and low ohmic current limiting resistors. Especially the low ohmic current limiting resistors provide essential advantages over other competitor devices with high ohmic bootstrap structures. A low ohmic resistor such as in the 2EDL family allows faster recharching of the bootstrap capacitor during periods of small duty cycles on the low side transistor. Such points of operation occur e.g. during low speed operation of drives at high torque, which can be excellently controlled with field oriented control of induction, permanent magnet synchronous or BLDC motors. There is usually no complete recharging possible any more during small duty cycles, so that the bootstrap voltage at the bootstrap capacitor C_{BS} sinks. The design must ensure, that the gate is always supplied properly in order to avoid excessive conduction losses and hence IGBT damage. A low ohmic current limiting resistor such as in the 2EDL family leads to sufficient bootstrap supply, when the LS transistor is operated at 2% duty cycle according to Figure 10. The solid lines represent the PWM modulated ripple at room temperature. It is assumed as a rule of thumb, that the $R_{ds(on)}$ of any bootstrap FET is doubled, when the temperature increases by 100°C. The resulting curves at 125°C are shown as dashed lines. It is easy to see that the situation gets even more severe at 125°C with competitor devices, which use FET structures. A sufficient supply is here only possible with duty cycles above approx. 10% or even higher. A diode, which is used in the 2EDL family is much more temperature robust. Hence, the 2EDL family can be still used at high temperatures with a duty cycle of the low side transistor of 2%!

The bootstrap diode is usable for all kind power electronic converters. The bootstrap diode is a real pn-diode and not a FET structure of a similar workaround. The bootstrap diode of the 2EDL-family is applicable for all

control modes of modern power electronics, such as trapezoidal or sinusoidal drives control, continuous or discontinuous PWM schemes. No restrictions do limit designs or PWM schemes, when using the integrated bootstrap diode.

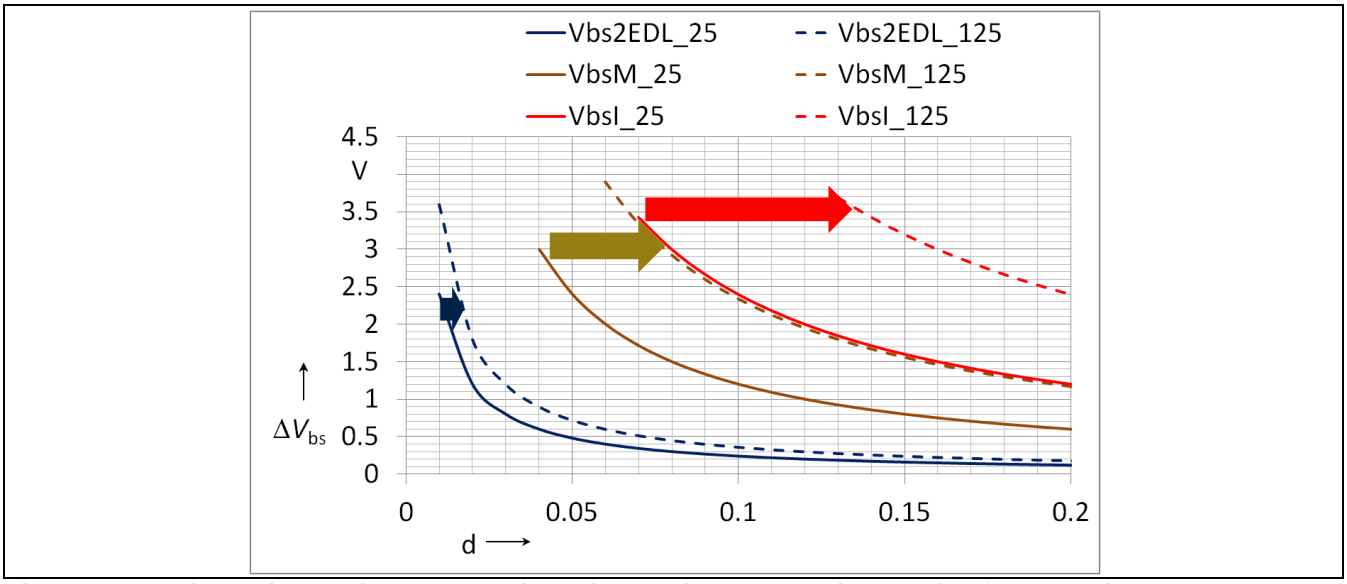

Figure 10 Voltage drop of bootstrap voltage in steady state vs. duty cycle of LS transistor

3.4.2 Supply voltage range calculation

The UVLO limits for IGBT types are designed in a way, that they support both, a proper start up as well as a save operation in PWM. It is the initial charging of the bootstrap capacitor during startup which must ensure, that the maximum limit of V_{BSUV+} is exceeded, so that the high side section is ready to operate. This means that the bootstrap capacitor C_{BS} according to Figure 11 is not charged, when the low side transistor T2 turns on. The related equation for the minimum supply voltage of IGBT types at the end of the charging cycle is

$$V_{DDminIGBT} = V_{BSUV+max} + V_{FBSmax} + V_{CE,LS} = 12.4\,V + 1.2\,V + 0.5V = 14.1\,V \quad (1)$$

where $V_{BSUV+max}$ is the maximum value for the positive going UVLO level of the high side section, V_{FBSmax} is the maximum bootstrap voltage and $V_{CE,LS}$ is the low side IGBT voltage. A shunt voltage can be neglected for initial charging. It can easily be seen, that a supply voltage of V_{DD} = 15 V is sufficient.

For MOSFET types there is

$$V_{DDminMOSFET} = V_{BSUV+max} + V_{FBSmax} = 9.9\,V + 1.2\,V = 11.1\,V \quad (2)$$

which means, that a supply voltage of $V_{DD} \approx$ 12 V is sufficient.

Another point of operation, which occurs in drive systems, is the operation at full load and low speed. It can be assumed for the case that the PWM frequency is much larger than the motor frequency (i.e. $f_p \gg f_{Mot}$), that there are periods of time, where the low side IGBT is almost continuously on. The IC should not go into UVLO protection there. The calculation is

$$\begin{aligned} V_{BS,IGBT} &= V_{VDD} - 1.2\,V - V_{CE,LS}(I_{nom}) - V_{Sh} = \\ &= 15\,V - 1.2\,V - 1.8\,V - 10A \cdot 20m\Omega = 11.8\,V > V_{BSUV-max} \end{aligned} \quad (3)$$

This equation goes with the assumption, that a shunt resistance of R_{Sh} = 20 mΩ is used for a 10A-IGBT.

In case $V_{BS,IGBT} < V_{BSUV-max}$, the V_{VDD} value should be chosen to have a value higher than 15V accordingly.

3.4.3 Calculating the bootstrap capacitance C_{BS}

Bootstrapping is a common method of pumping charges from a low potential to a higher one. With this technique a supply voltage for the floating high side sections of the gate drive can be easily established according to Figure 11. This circuit is shown for one of the three half bridges of a drives application.

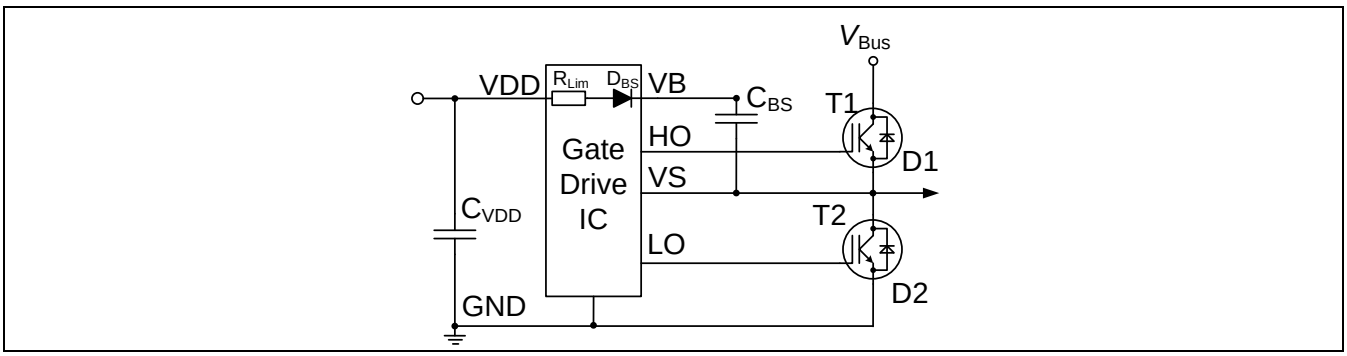

Figure 11 Bootstrap circuit for one half bridge

The first pulse of transistor T2 will force the potential of pin VS to GND. The existing difference between the voltage of the bootstrap capacitor V_{CBS} and V_{DD} results in the charging current i_{BS} into the capacitor C_{BS}. The current i_{BS} is a pulse current and therefore the ESR of the capacitor C_{BS} must be very small in order to avoid losses in the capacitor that result in lower lifetime of the capacitor.

This pin is on high potential again after transistor T2 is turned off and either T1 or D1 is conducting current. But now the bootstrap diode D_{BS} blocks a reverse current, so that the charges on the capacitor cannot flow back to the capacitor C_{VDD}. The bootstrap diode D_{BS} also takes over the blocking voltage between pin VB and VDD. It is good engineering to choose the same blocking voltage of power transistor T1 and external bootstrap diode. The voltage of the bootstrap capacitor can now supply the high side gate drive sections.

It is a general design rule for the location of bootstrap capacitors C_{BS}, that they must be placed as close as possible to the IC. Otherwise, parasitic resistors and inductances may lead to voltage spikes, which may trigger the undervoltage lockout threshold of the individual high side driver section. However, all parts of the 2EDL family, which have the UVLO for IGBT also contain a filter at each supply section in order to actively avoid such undesired UVLO triggers.

The voltage of bootstrap capacitor is approximately

$$V_{\mathrm{CBS}} \approx V_{\mathrm{DD}} - V_{\mathrm{FBS}} - V_{\mathrm{CE,LS}} \tag{4}$$

A current limiting resistor R_{Lim} according to Figure 11 reduces the peak of the pulse current during the turn-on of transistor T2. The pulse current will occur at each turn-on of transistor T2, so that with increasing switching frequency the capacitor C_{BS} is charged more frequently. Therefore a smaller capacitor is suitable at higher switching frequencies. The bootstrap capacitor is mainly discharged by two effects: The high side quiescent current and the gate charge of the transistor to be turned on. The calculation of the bootstrap capacitor results in

$$C_{\mathrm{BS}} = \frac{i_{\mathrm{QBS}} \cdot t_{\mathrm{P}} + Q_{\mathrm{G}}}{\Delta v_{\mathrm{BS}}} \cdot 1.2 \tag{5}$$

with i_{QBS} being the quiescent current of the high side section, t_P the switching period, Q_G the total gate charge and Δv_{BS} the voltage drop at the bootstrap capacitor within a switching period. An additional margin of 20% is added for the case of tolerances for the bootstrap capacitor. Please note, that the value Q_G may vary to a maximum value and the capacitor shows voltage dependent derating behavior of its capacitance. Equation (5) is valid for pulse by pulse considerations. It is easy to see, that higher capacitance values are needed, when operating continuously at small duty cycles of T2 or D2, e.g. in discontinuous conduction mode.

Figure 12 shows the curve corresponding to equ. (5) for a continuous sinusoidal modulation, if the voltage ripple Δv_{BS} = 0.1 V. The recommended bootstrap capacitance is therefore in the range up to 4.7 µF for most switching frequencies. The performance of the integrated bootstrap diode supports the requirement for small bootstrap capacitances. It is therefore recommended not to exceed a maximum capacitance of C_{BS} = 47 µF.

Please note here, that equ. (5) is valid for continuous switching operation according to the switching frequency. The use of space vector modulations can cause periods up to 60° (electrical), in which no switching of the low side transistor of a half bridge occurs and must be considered separately. This effects the bootstrap capacitor

size, especially for low output current (motor current) frequencies. In this case the variable t_P must be set to the longest period of no charging.

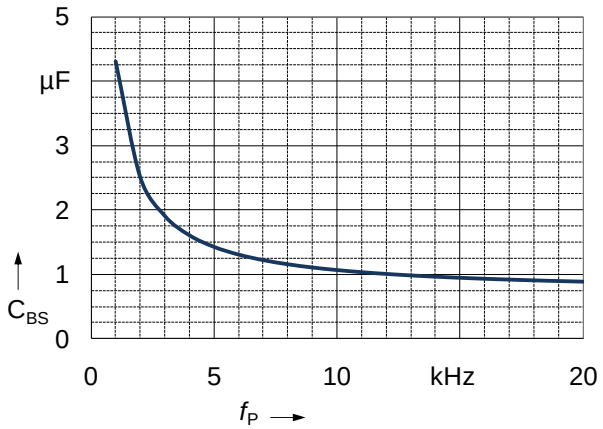

Figure 12 Size of the bootstrap capacitor as a function of the switching frequency f_P for driving IKD10N60R according to equ. (5) **with a voltage ripple of 0.1 V**

3.5 Protection

3.5.1 Overcurrent protection (OCP, 2EDL23x06PJ only)

The current signal of the DC-link reference is measured in order to recognize overcurrent or half bridge short circuit events. A shunt resistor generates a voltage drop, which triggers a comparator with a threshold of $V_{ITRIP,TH+}$ = 0.46 V according to Figure 13. An integrated filter with a time constant of 1.8 µs suppresses potential voltage spikes caused by non-optimal layout or by reverse recovery events, when commutating on the diode of a low side switch.

This triggering current is calculated with

$$I_{ITRIP} = \frac{V_{IT,TH+}}{R_{SH}} \quad (6)$$

where R_{SH} is the value of the shunt resistor.

It is generally recommended as good engineering to use low inductive SMD shunts (maximum allow power should not be violated). These shunts are wide spread in the market and generate only small inductive transient voltages. Such voltages can disturb e.g. the current sensing signal, but also a proper operation of current sensing amplifiers or comparators. Other shunt solutions generally have more disadvantage comparing with SMD shunts so that it is not prefered. The maximum allowed voltage level at pin PGND (as shown in Figure 13) must be fulfilled under any circumstance. In case big overvoltage due to noise or paracistic effect can be observed, measures need to be taken to protect the PGND pin, e.g. back to back connected zener diodes or decoupling capacitor which are tied between PGND and GND.

The output of the comparator passes a noise filter, which inhibits an overcurrent shutdown caused by parasitic voltage spikes. The typical filter time of the noise filter is $t_{FILITRIP}$ = 1.8 µs. This is a large filter, but the connection of the shunt sense track to pin PGND, which is the return path of the gate current, does not allow any external filtering. A set-dominant latch stores the overcurrent event for typically 230 µs until it is reset either by the external pull up resistor or by a signal provided from the microcontroller. The reset is realized by pulling the voltage at pin EN-/FLT higher than the input high level voltage V_{IH}.

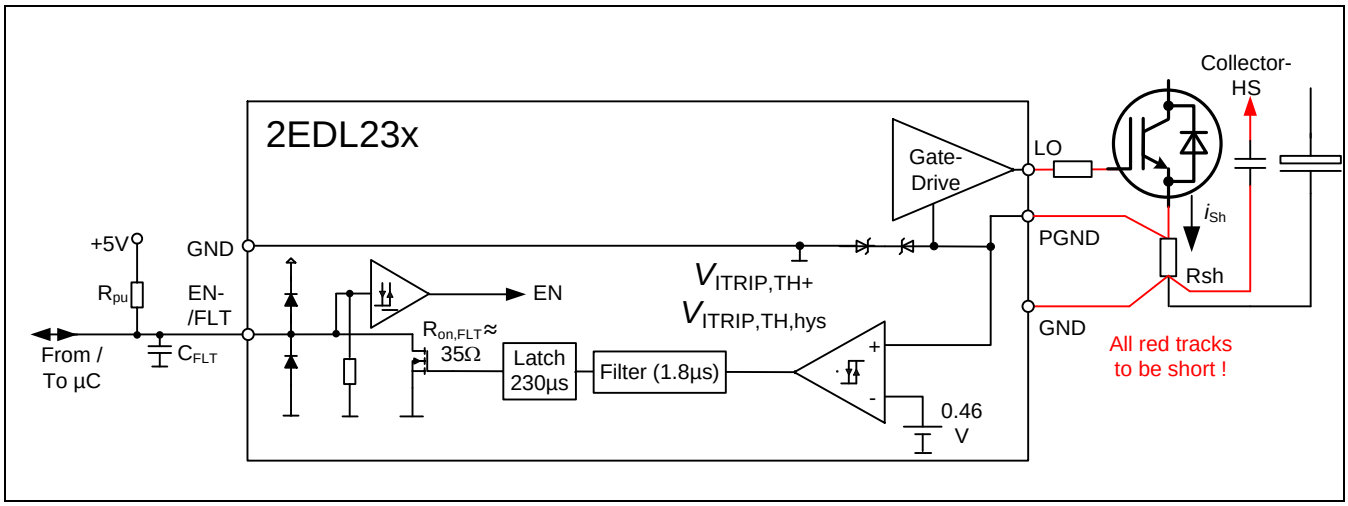

Figure 13 Internal structure of the ITRIP and EN-/FLT sections

The ITRIP-latch activates the discharging NMOS-FET at pin EN-/FLT. The $R_{DS(on)}$ of this FET ($R_{on,FLT}$) is typically 35 Ω, so that there is a characteristical discharge curve in respect of the external capacitor C_{FLT}. The time constant is defined by the external capacitor C_{FLT} and the $R_{on,FLT}$. The discharge phase ends, when the comparator is low again. This corresponds to a voltage level at the comparator of $V_{IT,TH+}$ - $V_{IT,HYS}$ = 460 mV – 70 mV = 390 mV, where $V_{IT,HYS}$ = 70 mV is the hysteresis of the ITRIP-comparator.

To avoid repetitively switching on and off of driver IC and power devices during a continuously ITRIP events (e.g. real short circuit), each ITRIP event should trigger the blanking logic which will block the input signal. To achieve this, the voltage at pin EN-/FLT must be reduced (by discharging external C_{FLT}) lower than the minimal $V_{EN,TH-}$ (0.7V for this product) value inside the 230µs latch time, which follows the equation

$$V_{EN} = V_0 * e^{\frac{-t}{R_{on,FLT}C_{FLT}}} < V_{EN,TH-\_min} \quad (7)$$

here, the V_0 is the voltage at pin EN-/FLT which is defined by the external pull-up power supply (+5V in this example). The value of C_{FLT} must be carefully chosen according to this equation, so that too big capacitor can be avioded.

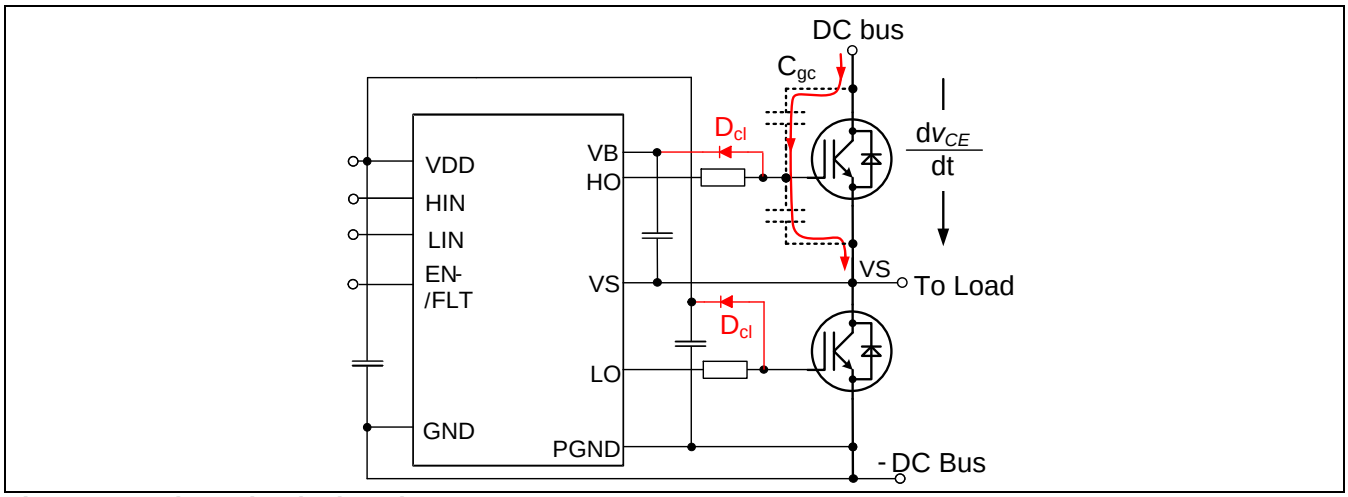

Figure 14 Short circuit clamping

Another issue should be noticed that, when short circuit or over current happens (e.g. VS short to ground) as shown in Figure 14, due to the high dv/dt across the power device there will be displacement current going through the Miller capacitor, the gate voltage will be further lifted up. In this case the current of the power device will be further increased which could easily damage the power device. To prevent this, an external clamping diode (D_{cl}) between gate of power device and the supply pin of driver IC (VB) is recommended. The same theory also applies to low side circuit, here the gate of power device need to be clamped to VDD.

3.5.2 Deadtime & Shoot Through Prevention

The 2EDL family prevents shoot through and generates a fixed deadtime between the individual power devices of each half bridge. The deadtime is typically DT = 380 ns for IGBT version and DT = 75 ns for MOSFET version. However, it is necessary to check the transient times of the driven power devices. These times are the turn-on delay $t_{d(on)}$, the rise time t_r, the turn-off delay time $t_{d(off)}$ and the fall time t_f. They are defining the timing and the deadtime which is mandatory for the prevention of shoot through. A deadtime of 1 µs to 1.5 µs is sufficient for most applications. Please note, that especially the transient behavior of power transistors can limit the minimum dead time depending on junction temperature, collector current and gate resistance.

It is only the type 2EDL05I06BF, which does not have any dead time and interlocking implemented. This part is the optimal driver IC for switched reluctance motors (SRM), welding systems using two-transistor-forward topology and other applications, where it is required to turn on the high side output simultaneously to the low side output.

3.5.3 Undervoltage Lockout (UVLO)

Both output sections are shut down in case of an undervoltage condition on the pin VDD by blocking the signals to the low side and the high side section. There is an additional undervoltage detection for the high side only, so that the high side section can also be shut down independently from the low side. The levels are V_{DDUV+} for the control side and V_{BSUV+} for the high side sections. Please refer to the correct absolute level in respect to the individual type of the 2EDL family. Please refer to section 3.2 for further information.

In case of an UVLO shut down of an output section, it is necessary to reach the start-up levels of V_{DDUV+} and V_{BSUV+} again as described in section 3.2. The independent UVLO functions of the low and high side section enable a restart of the affected high side section in case of a bootstrapping supply, because the switch mode operation of the low side transistor pumps continuously charges into the according bootstrap capacitor, which increases the bootstrap voltage V_{BS}.

All IGBT type driver IC of the 2EDL family contain a filter (approx. 1.5µs) for the supply voltage level V_{DD} and the high side supply voltage level V_{BS}. This avoids undervoltage events, which are caused by noise or crosstalk as it is shown in Figure 15. The outputs shut down in any case, when V_{DD} or V_{BS} drops below 7.5 V. The type 2EDL23I06PJ and 2EDL23N06PJ indicates the UVLO by pulling the pin EN-/FLT down to ground. The types 2EDL05I06PF and 2EDL05I06PJ also filter the supply levels, but don´t indicate this by a specific pin.

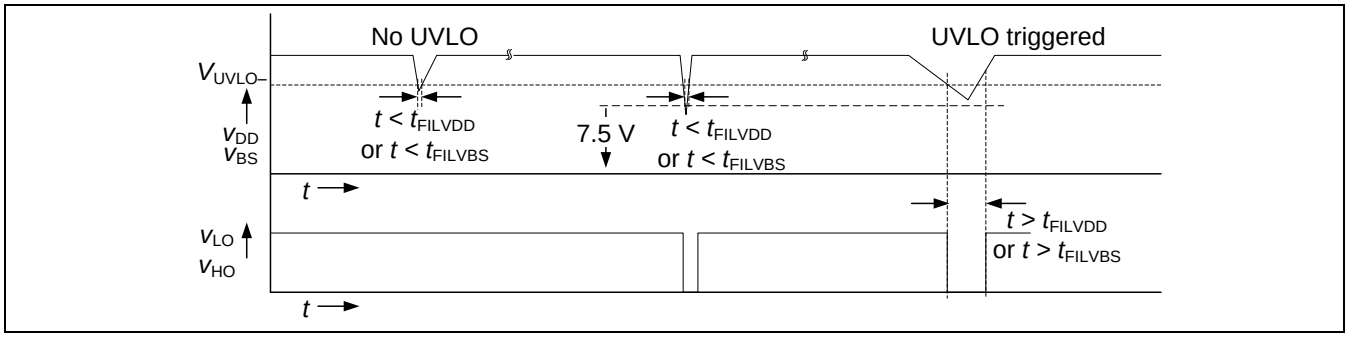

Figure 15 UVLO filter time

All MOSFET types (2EDL23N06PJ and 2EDL05N06PF) have a filter time for UVLO in the range of approx. 150 ns.

3.6 Calculation of power dissipation and thermal aspects

The 2EDL family is available in two packages, the PG-DSO-8 and the PG-DSO-14. Both packages are RoHS compliant. Please refer to section 3.7 for further information in respect to the insulation coordination. It is essential to assure, that the component is not thermally overloaded. This can be checked by means of the thermal resistance junction to ambient and the calculation or measurement of the dissipated power. The thermal resistance is given in the datasheet (section 4) and refers to a specific layout. Changes of this layout may lead to an increased thermal resistance, which will reduce the total dissipated power of the driver IC. One should therefore do temperature measurements in order to avoid thermal overload under application relevant conditions of ambient temperature and housing.

The maximum chip temperature T_j can be calculated with

$$T_j = P_d \cdot R_{th(ja)} + T_{amb,max} \quad (8)$$

where $T_{amb, max}$ is the maximum ambient temperature.

The dissipated power P_d is a combination of several sources. The following items contribute to the total power dissipation:

- the quiescent current (high side and low side) of the IC (P_{d1VDD}, P_{d1BS})
- the output section (P_{d2on}, P_{d2off})
- the input sections of the IC (P_{d3})
- the leakage losses between any high side section to the control section (P_{d4})

The individual items can be calculated for a worst case by means of the following cooking recipe:

1. Measure the operating current I_{DD} for maximum switching frequency of the application. Connect both control pins and do not connect power transistors.

$$P_{d1VDD} = I_{DD,max} \cdot V_{DD,max} \quad (9)$$

Each high side section generates continuous power dissipation in respect of the quiescent current. This is given as

$$P_{d1BS} = I_{QBS} \cdot V_{BS,max} \quad (10)$$

2. Calculate the losses of the output section by means of the total gate charge of the power transistor Q_{Gtot} , the supply voltage V_{DD}, the switching frequency f_P ,and the ext. gate resistor. Different cases for turn-on and turn-off must be considered, because many designs use different resistors for turn-on and turn-off. This leads to a specific distribution of losses in respect to the external gate resistor $R_{Gxx,ext}$ and the internal resistance of the output section. When we take 2EDL 0.5A version as an example

$$P_{d2on} = \frac{2}{2} Q_{G,tot} \cdot V_{DD} \cdot f_P \cdot \frac{22.5\Omega}{R_{Gon,ext} + 22.5\Omega} \quad \text{, for turn-on} \quad (1)$$

$$P_{d2off} = \frac{2}{2} Q_{G,tot} \cdot V_{DD} \cdot f_P \cdot \frac{6.5\Omega}{R_{Goff,ext} + 6.5\Omega} \quad \text{, for turn-off} \quad (2)$$

If the 2EDL 2.3A version is used

$$P_{d2on} = \frac{2}{2} Q_{G,tot} \cdot V_{DD} \cdot f_P \cdot \frac{7\Omega}{R_{Gon,ext} + 7\Omega} \quad \text{, for turn-on} \quad (3)$$

$$P_{d2off} = \frac{2}{2} Q_{G,tot} \cdot V_{DD} \cdot f_P \cdot \frac{5\Omega}{R_{Goff,ext} + 5\Omega} \quad \text{, for turn-off} \quad (4)$$

Both portions P_{d2on} and P_{d2off} together are the output section losses.

3. The input sections generate losses by means of their input structures. These are pull-down resistors of approx. 100 kΩ

$$P_{d3} = \frac{2}{2} \cdot \frac{V_{in}{}^2}{100k\Omega} \quad (5)$$

4. The leakage losses are given by the current, which crosses the insulation barrier. The relevant parameters are the leakage current I_{LVS} of any high side and the DC bus voltage V_{DC} of the application. The high side section is either on the positive bus potential or at the negative bus potential during operation. It is therefore in principle half the product of these two values. However, there can be a static status of operation, where all three high side sections are on high potential. Thus, we get

$$P_{d4} = I_{LVS} \cdot V_{DC,max} \quad (6)$$

All remaining contributions can be estimated as approximately 20% of the sum of the above mentioned portions. The final power dissipation during operation is then the sum of both contributions

$$P_{\mathrm{d}} = 1.2\left(P_{\mathrm{d1VDD}} + P_{\mathrm{d1QBS}} + P_{\mathrm{d2on}} + P_{\mathrm{d2off}} + P_{\mathrm{d3}} + P_{\mathrm{d4}}\right) \quad (7)$$

The datasheet shows specific layouts, for which the given thermal resistance junction to ambient ($R_{\mathrm{th(j\text{-}a)}}$) is valid. The thermal resistance which is given in the datasheet is specified for equal operation of both power transistors. It is important to know, that different layouts may lead to different thermal resistances. It is therefore always good engineering praxis to examine additionally the package temperature by experiment.

3.7 Creepage

The creepage distance of the DSO-8 package (2EDL05I06PF, 2EDL05N06PF and 2EDL05I06BF) is **2.140 mm** according to the package drawing. The related parameter for 2EDL05I06PJ is **2.865 mm,** for 2EDL23I06PJ and 2EDL23N06PJ it is **2.105 mm**. It depends on the individual application standard, such as [3] or [4], the safety concept of the end device as well as the application conditions, such as pollution degree, etc. to identify the relevant requirements for the system.

The mentioned standards and similar ones describe in detail the relevant considerations for an appropriate calculation of the creepage distance for the target system.

3.8 Design considerations

Please note, in no circumstance the driver IC can be used in parallel (it is not allowed to connect several driver ICs in parallel).

3.9 Layout considerations

Parasitic in inductances the ground circuit or in the gate circuits exist by means of PCB track loops. They can lead to oscillations in the according tracks. This can be the root cause of abnormal function of the IC. Figure 16 shows these inductances and track loops.

First of all, the gate tracks, which connect the pins HO and LO with the according gate terminal of the power transistor and the tracks connecting the emitter / source terminals of the power transistor with the VS or PGND of the IC must be as short as possible. The area of these tracks must be minimized. This ensures, that the switching speed of the high side transistor and the low side transistor are similar or even equal. The loop, which consists of pin PGND, the shunt resistor and pin GND should be as well minimized. Figure 16 shows the case of a single shunt design. Some systems may use one shunt in each phase of the drive, which is located between source / emitter of the low side transistor and the pin PGND. The driver IC is usually stabilized by means of a low impedance capacitor, which may be a ceramic type. The loop between pin VDD, the capacitor and GND should also be as small as possible. This helps to minimize the gate circuit inductances as well as the bootstrap circuit inductances.

A similar consideration must be done for the high side supply circuit. The loop of pins VB, the bootstrap capacitor C_{BS}, and the pin VS must also be small. Otherwise, there may be inductive voltage drops during the gate charging process of turn-on, which may result in spontaneous undervoltage lockout events at the high side section.

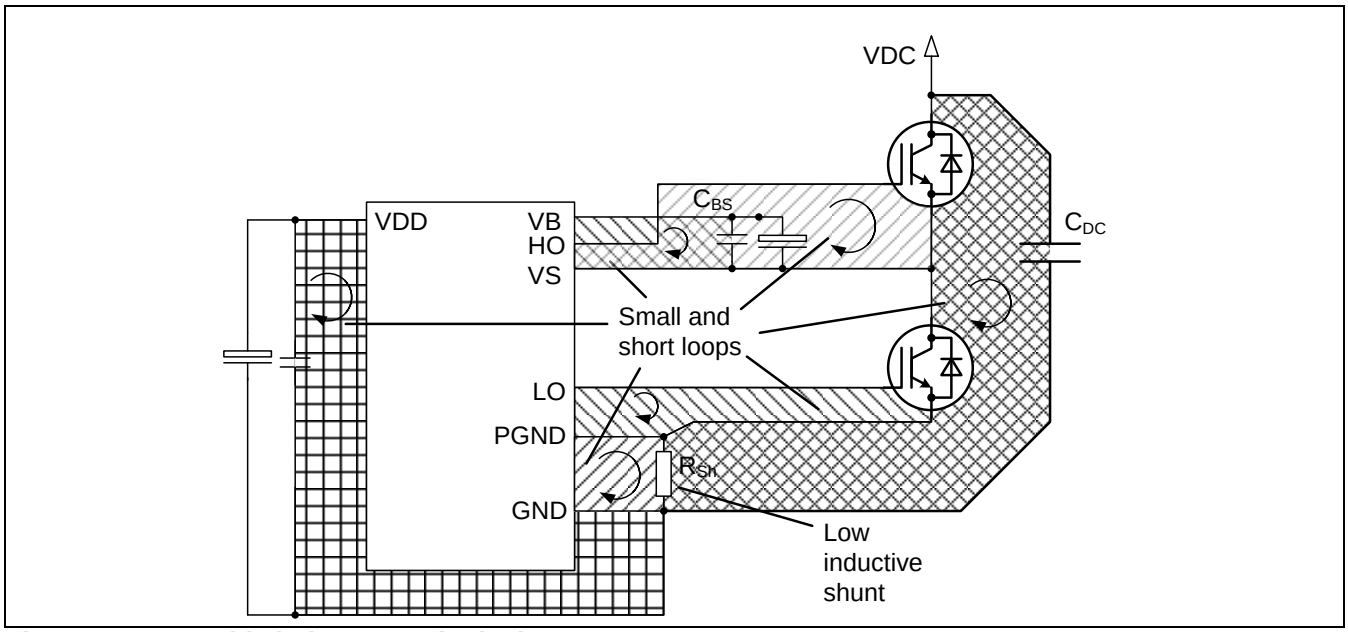

Figure 16 Parasitic inductances in the layout

Finally, the inductances of the DC link tracks can be partially cancelled, if one places a low impedance film capacitor between the positive and negative rail closely to the transistor terminals as shown in Figure 16 with C_{DC}.

4 List of used parameters

4.1 General

big letters — Time constant parameters
small letters — Time varying parameters
italic letters — physical parameters
upright letters — components in circuits

Table 2 Used parameters

Parameter	Description	Parameter	Description
A	area	*p, P*	power
b, B	flux density	*r, R*	resistance
C	capacitance	*t, T*	time, time intervals
d, D	duty cycle	*v, V*	voltage
f	frequency	*w, W*	energy
i, I	current	η	efficiency
l, L	inductance		
C	capacitor	L	inductor
D	diode	R	resistor
IC	integrated circuit	TR	transformer
AC	alternating current value	i	running variable
avg	average	in	input value
DC	direct current value	max	maximum value
BE	basis-emitter	min	minimum value
C	collector value	off	turn-off / off-state value
E	emitter value	on	turn-on / on-state value
G	gate value	out	output value
P	primary side value	p	pulsed
Pk	peak value		
S	secondary side value		

References

[1] KOA corporation: “Handling precautions for flat chip resistors”, Revision B 1.1, application note, KOA corporation, Japan, 2007

[2] KOA corporation: “Flat chip thick film resistors general purpose RK73B”, Revision 10.11.2006, data sheet, KOA corporation, Japan, 2006

[3] IEC 60335-1: "Household and similar electrical appliances – Safety – Part 1: General requirements”, Ed. 4, 2001-05; International Electrotechnical Commission; Geneva, Switzerland, 2001

[4] IEC 664-1: "Insulation coordination for equipment within low-voltage systems – Part 1: Principles, requirements, tests”, Ed. 1, 1992-10; International Electrotechnical Commission; Geneva, Switzerland, 1992

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