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Preventing ESD Induced Failures in Small Signal MOSFETs

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Table of contents

1 Introduction

This application note is intended to explain the most commonly accepted ESD standards and tests, ESD induced failures and basic ESD protection for Small Signal MOSFETs.

2 ESD in semiconductor devices

Downscaling, together with the increase of doping levels, results in a dramatic reduction of the gate oxide layer thickness and the width of the pn-junction in semiconductor devices. This, in combination with denser circuit population, increases the susceptibility of the devices to ESD.

The subsequent failures of electronic equipment can be identified as hard failures, latent damage or temporary malfunction. Hard failures are easier to spot, and in general require the failed device to be replaced. Failures leading to temporary malfunction of equipment or latent failures are quite common and very difficult to detect or trace in the field.

Even with better ESD protection, an ESD strike represents a permanent threat to device reliability as it can easily find a way to bypass the protection and be injected into the chip.

One of the most common causes of ESD damage is the direct transfer of charges through a significant series resistor from the human body or a charged material. This sudden release of charge into a device can produce high voltage or current that can result in irreversible transformation and destruction.

3 ESD standards and tests

There are two basic mechanisms of ESD that occur within a device. The first mechanism is emulated by the Human Body Model (HBM). In this model, charge is transferred to the device via the human body. The second mechanism is simulated by the Charge Device Model (CDM). In this model the device is charged and allowed to discharge to a grounded body. Although the word “model” is used, these are actually different tests to determine the ESD robustness of a particular device. These models are used to qualify products and a number of standards exist to outline each testing method.

HBM is the most widely accepted ESD test. With HBM testing the failure modes typically comprise junction damage, melting of metal layers and damage of the gate oxides. These failure modes are explained in the next section. The set up for the test procedure is shown in Figure 1 below.

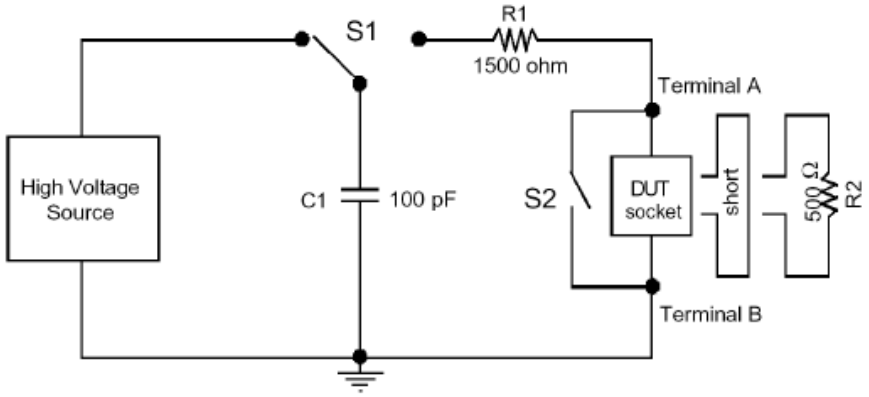

Figure 1: HBM test setup

The capacitor C1 is initially charged to different voltages based on the ESD standard. This capacitor is then discharged through a Device Under Test (DUT). The highest voltage level that a device can survive is used to classify the ESD sensitivity. This classification is shown in Table 1.

Class	Description
0	Any device that fails after exposure to an ESD pulse of 250V or Less
1A	Any device that passes after exposure to an ESD of 250V but fails up to an ESD pulse of 500V
1B	Any device that passes after exposure to an ESD of 500V but fails up to an ESD pulse of 1000V
1C	Any device that passes after exposure to an ESD of 1000V but fails up to an ESD pulse of 2000V
2	Any device that passes after exposure to an ESD of 2000V but fails up to an ESD pulse of 4000V
3A	Any device that passes after exposure to an ESD of 4000V but fails up to an ESD pulse of 8000V
3B	Any device that fails after exposure to an ESD pulse of 8000V

Table 1: ESD sensitivity classification for HBM

The figure below shows a typical oscilloscope readout with an initial current spike when the capacitor starts discharging and ramps down until it approaches 0A at approximately 500 nano seconds in an HBM test.

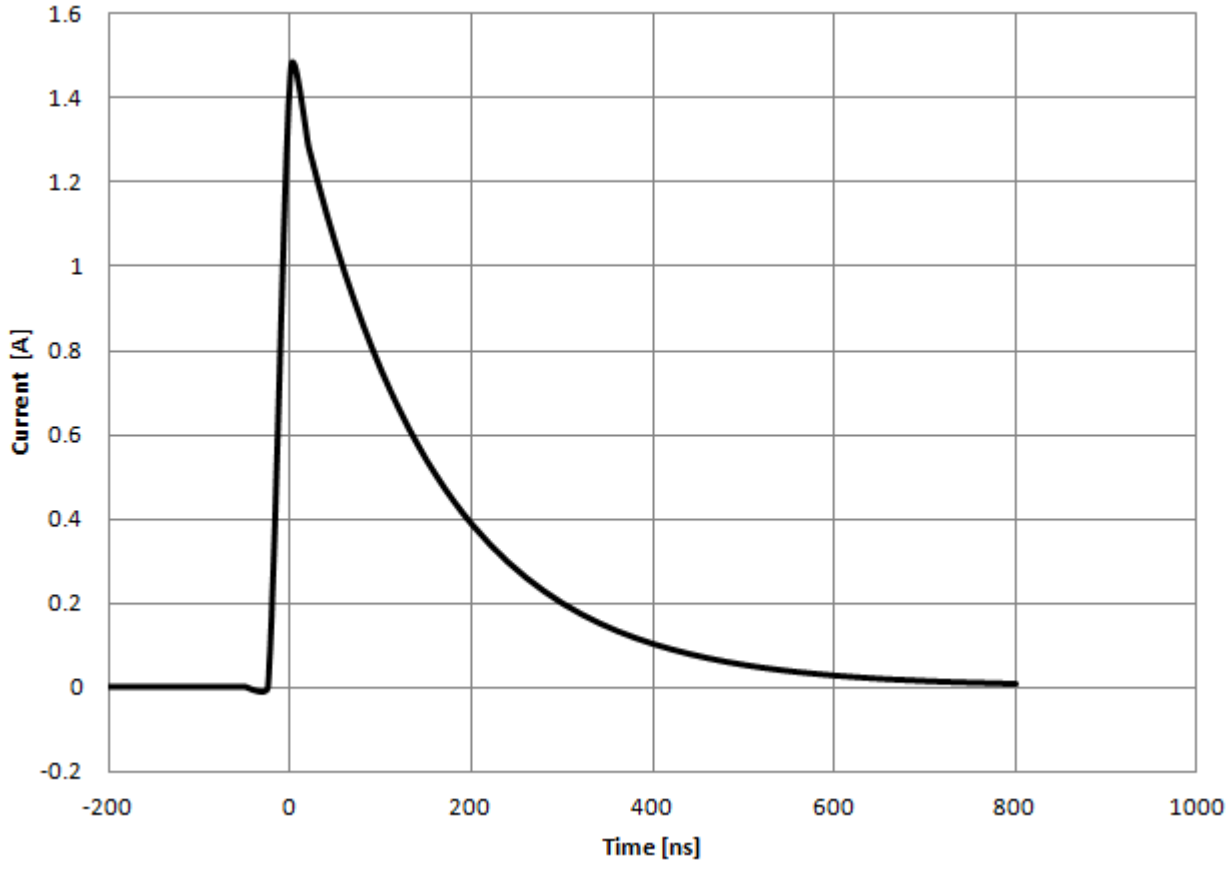

Figure 2: A typical oscilloscope readout in a HBM test

4 ESD failure of MOSFETs

In MOSFETs, there are three basic ESD induced failures; junction damage, gate oxide damage and metallization burnout. These failures are thermally induced, indicating that damage occurs once the temperature of the local area exceeds a critical value, often the melting point of the material.

4.1 Junction damage

The most common HBM failure is junction damage. Junction damage is caused by the injection of an ESD transient of sufficient energy and duration to force the junction into secondary breakdown. Junction damage is often characterized by high reverse bias leakage current or a total short.

Failure analysis of a damaged junction has revealed that two types of junction burnout failure exist: soft failure and hard failure. Soft failures are small spikes along the gate edge. Hard failures are where severe damage extends across the complete channel length of the device. Soft failures exhibit a slight increase in the junction leakage, but the MOSFET is still functional. Devices experiencing hard failures are often not functional, exhibiting very high leakages. The electrical signature of the failure is often a resistive short across the drain and source terminals.

4.2 Gate oxide damage

Gate oxide damage is the major category of ESD damage. It occurs when the gate is subjected to an ESD pulse of high enough magnitude to cause the gate oxide to breakdown. Tests have shown that the gate oxide breaks down in the area where it is subjected to the greatest electric field strength.

For MOSFETs, the gate oxide is extremely thin resulting in varying degrees of ESD sensitivity. The electric field (E) across the gate oxide thickness (t_{ox}) when a voltage (V) is applied is given by $E = V/t_{ox}$.

For smaller t_{ox}, the electric field E can exceed the breakdown fields for relatively small voltages. In the short transient domain of an ESD event, the voltage applied to the gate must be very large to initiate gate oxide breakdown.

Another very common event under HBM is the accumulation of trapped charge in the gate oxide, leading to a shift of the threshold voltage of the MOSFET. This shift of threshold voltage may cause a functional failure.

4.3 Metallization burnout

Metallization burnout exists in metal interconnects or contacts. It occurs if the current flowing through the metal forces a temperature rise (due to the I^2R power losses) high enough to reach the melting point of the material. Metallization burnout is often a secondary effect, occurring after the initial junction or gate oxide failure.

5 ESD protection

To protect a MOSFET from ESD, the main objective is to clamp the gate to source voltage from reaching the destructive voltage.

A typical ESD protection device clamps the voltage to a lower value at the occurrence of the ESD strike to minimize the voltage seen at the gate of MOSFET. The protection device shunts current to ground and away from the protected gate. During this period the clamping voltage and residual current seen at the gate depends upon the breakdown voltage and the dynamic resistance of the protection device. Once the ESD strike is fully dissipated, the ESD protection device attempts to return to a high impedance state. There are several types of ESD protection devices available today, but most commonly used are TVS and Zener diodes (also available from Infineon).

However, the first and foremost line of defence is at the time of assembly of the device. Conductive packing materials and boxes are preferred for transportation and storage since they not only prevent charge build-up but also provide shielding from external electrical fields.

Thus the basic concept of complete static protection is the prevention of static charge build-up and removal of already existing charges to protect the device from ESD induced failures.