Design Guide for LLC Converter with ICE2HS01G

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Design Guide for LLC Converter with ICE2HS01

Revision History:	**2011-07**	V1.0
Previous Version:	NA	

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1 Abstract

ICE2HS01G is our 2nd generation half-bridge LLC controller designed especially for high efficiency with its synchronous rectification (SR) control for the secondary side. With its new driving techniques, SR can be realized for half-bridge LLC converter operated with secondary switching current in both CCM and DCM conditions. No individual SR controller IC is needed at the secondary side.

A typical application circuit of ICE2HS01G is shown in Figure 1. For best performance, it is suggested to use half-bridge driver IC in the primary side with ICE2HS01G.

Figure 1   Typical application circuit

In this application note, the design procedure for LLC resonant converter with ICE2HS01 is presented, together with an example of a 300W converter with 400VDC. Detailed calculation of the values of the components around the IC is also included, together with tips on the PCB layout.

2 Design Procedure

2.1 Target Specifications

The design example is based on the typical application circuit in Figure 1, where individual resonant choke is implemented. The target specifications are summarized in Table 1.

Input voltage V_{in}	400VDC
Output voltage and current V_o, I_o	12VDC, 25A
Output power P_{in}	~ 300W
Efficiency η	>96% at 100% load >97% at 50% load >96% at 20% load
Resonant frequency f_r	85kHz
Hold up time T_h	20ms
Bulk capacitor C_{out}	270uF

Table 1   Target application specifications

2.2   Design of Power Stage

2.2.1   System specifications

The maximum input power can be calculated as:

$$P_{in} = \frac{V_O * I_O}{\eta} = \frac{12 * 25}{0.96} = 312.5W \qquad [1]$$

Based on the required 20ms hold-up time, the minimum input voltage can be given as:

$$V_{in\_min} = \sqrt{V_{in\_nom}^2 - \frac{2P_{in}T_h}{C_{out}}} = \sqrt{400^2 - \frac{2 * 312.5 * 20 * 10^{-3}}{270 * 10^{-6}}} = 337.2V \qquad [2]$$

2.2.2   Selection of resonant factor m

In order to achieve the highest efficiency possible, the value of resonant factor $m = \dfrac{L_p}{L_r} = \dfrac{L_m + L_r}{L_r}$ is to

be set as big as possible, so that the magnetizing inductance L_m is big and therefore magnetizing current is small, which results in low core loss and conduction loss. On the other hand, the magnetizing current should be big enough to discharge the C_{ds} of primary side MOSFET during the transitions, to realize ZVS to ensure safe switching and save switching loss. In this design example, $m = 13$ is selected as a start. The ZVS of primary side MOSFET will be confirmed later with the determination of the deadtime of switching.

2.2.3 Voltage gain

It is for efficiency optimization to operate the LLC converter around the resonant frequency at nominal input voltage, where the voltage gain $M_{nom} = 1$, on condition that the secondary-side leakage inductance is neglected due to the implementation of individual resonant choke.

The worst case we need to consider for resonant network and transformer design is the full load operation at minimum input voltage V_{in_min}. The maximum voltage gain at V_{in_min} can be calculated as:

$$M_{max} = \frac{V_{in\_nom}}{V_{in\_min}} M_{nom} = \frac{400}{337.2} * 1 = 1.19 \qquad [3]$$

2.2.4 Transformer turns ratio

Assuming the drain-source voltage drop of secondary-side MOSFET $V_f = 0.1V$, the transformer turns ratio will be:

$$n = \frac{V_{in\_nom}}{2(V_o + V_f)} M_{nom} = \frac{400}{2 * (12 + 0.1)} * 1 = 16.5 \qquad [4]$$

2.2.5 Effective load resistance

The effective load resistance can be given as:

$$R_{eff} = \frac{8}{\pi^2} n^2 \frac{V_o}{I_o} = \frac{8}{\pi^2} * 16.5^2 * \frac{12}{25} = 106\Omega \qquad [5]$$
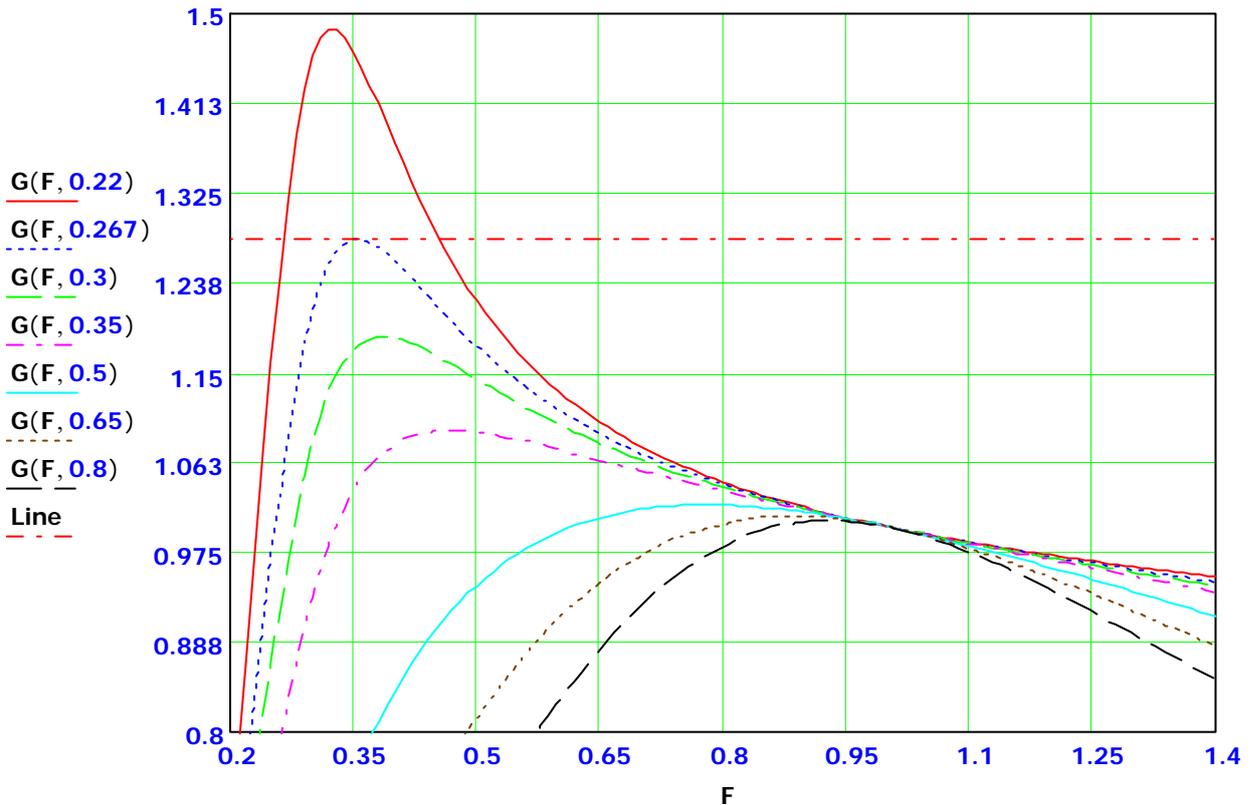
2.2.6 Resonant network

Defining the normalised frequency to f_r is $F = \dfrac{f}{f_r}$, the load factor of the LLC converter is $Q = \dfrac{\sqrt{L_r / C_r}}{R_{eff}}$, the voltage gain of the converter can be written as:

$$Mj(F,Q) = \frac{F^2(m-1)}{(F^2 m - 1) + jF(F^2 - 1)(m-1)Q} \qquad [6]$$

Its magnitude is:

$$G(F,Q) = \sqrt{\text{Re}(Mj(F,Q))^2 + \text{Im}(Mj(F,Q))^2} \qquad [7]$$

The graph of voltage gain G Vs F for different Q can be plotted based on [7] with Mathcad:

Figure 2   Voltage gain G Vs normalized frequency F

Among the curves, we find that the one with $Q = 0.267$ can achieve the required peak gain G_{pk}, which is 8% higher than M_{max} for design margin, i.e.

$$G_{pk} = 1.08 M_{max} = 1.28$$

From the curve, the corresponding $F_{min} = 0.35$ can be located where $G_{pk} = 1.28$ is achieved.

Having found the proper Q, we can calculate the C_r, L_r and L_p as follows:

$$C_r = \frac{1}{2\pi * Q * f_r * R_{eff}} = \frac{1}{2\pi * 0.268 * 85 * 10^3 * 106} = 66nF \qquad [8]$$

$$L_r = \frac{1}{(2\pi * f_r)^2 * C_r} = \frac{1}{(2\pi * 85 * 10^3)^2 * 66 * 10^{-9}} = 53uH \qquad [9]$$

$$L_p = mL_r = 690uH$$

2.2.6.1   Resonant choke design

The minimum rms voltage across the resonant network is:

$$V_{in\_rms\_min} = \frac{\sqrt{2}}{\pi} V_{in\_min} = \frac{\sqrt{2}}{\pi} * 337.2 = 151.79V \qquad [10]$$

Then the corresponding rms current flowing through the resonant choke L_r can be calculated as:

$$I_{in\_rms\_max} = \frac{P_{in}}{\eta * V_{in\_rms\_min}} = \frac{300}{0.96 * 151.79} = 2.06A \qquad [11]$$

The peak current is $I_{r\_pk} = \sqrt{2} * I_{r\_rms} = 2.91A$. The OCP level is set with about 20% margin:

$$I_{ocp\_pk} = 1.2 * I_{r\_pk} = 3.49A$$

The actual leakage inductance (L_{leak}) measured at primary side with one of the secondary side winding shorted is around 13uH. Therefore, the inductance for the independent resonant choke is:

$$L_{r\_choke} = L_r - L_{leak} = 40uH$$

If a magnetic core with specs of RM10/PC95 is selected, where $A_{e\_min} = 90mm^2$, and B_{max} is selected to be 0.08T to reduce core loss, the minimum turns can be given as:

$$N_{L\min} = \frac{L_{r\_choke} \cdot I_{r\_pk}}{B_{L\max} \cdot A_{L\min}} = \frac{40*10^{-6}*3.49}{0.08*90*10^{-6}} = 19.4 \qquad [12]$$

2.2.7   Transformer design

From Figure 2, the normalized frequency $F_{\min} = 0.35$ has been located to achieve maximum gain $G_{pk} = 1.28$. Accordingly the actual minimum frequency $f_{\min}$ is:

$$f_{\min} = F * f_r = 0.35 * 85 * 10^3 = 30kHz$$

The voltage across the primary winding can be calculated as $V_p = n(V_o + V_f)$. The half switching cycle period is around: $t = \dfrac{1}{2 f_{\min}}$. According to Faraday's law:

$$\frac{n(V_o + V_f)}{2 f_{\min}} = N_p A_e \Delta B$$

The minimum number of turns at primary side can be found:

$$N_{p\min} = \frac{n(V_o + V_f)}{2 f_{\min} * A_e \Delta B} \qquad [13]$$

Where $A_e = 161mm^2$ with PQ3230 core. $\Delta B = 0.62T$ is selected to avoid magnetic saturation.

Then $N_{p\min}$ can be calculated as:

$$N_{p\min} = \frac{16.5*(12+0.1)}{2*30*10^3*161*10^{-6}*0.62} = 33$$

The number of turns at primary side is selected as $N_{p\min} = 33$. The secondary side turns can be calculated accordingly:

$$N_s = \frac{N_p}{n} = 2$$

2.2.8   SR MOSFET

The voltage stress on the drain-source of the MOSFET is:

$$V_{ds} = (V_o + V_f) * 2 = 24.2V$$

The RMS value of the current flowing through each MOSFET is:

$$I_{d\_rms} = \frac{\pi}{4} I_o = 19.63A$$

2.3   Design of Control Parameters and Protections

2.3.1   Frequency setting:

The IC internal circuit provides a regulated 2V voltage at FREQ pin. The effective resistance presented between the FREQ pin and GND, determines the current flowing out of the FREQ pin, which in turn defines the switching frequency.

Figure 3 shows the curve illustrating the relationship of Switching Frequency $FREQ$ Vs Effective Resistor R_{FREQ} connected between the FREQ pin and gound.
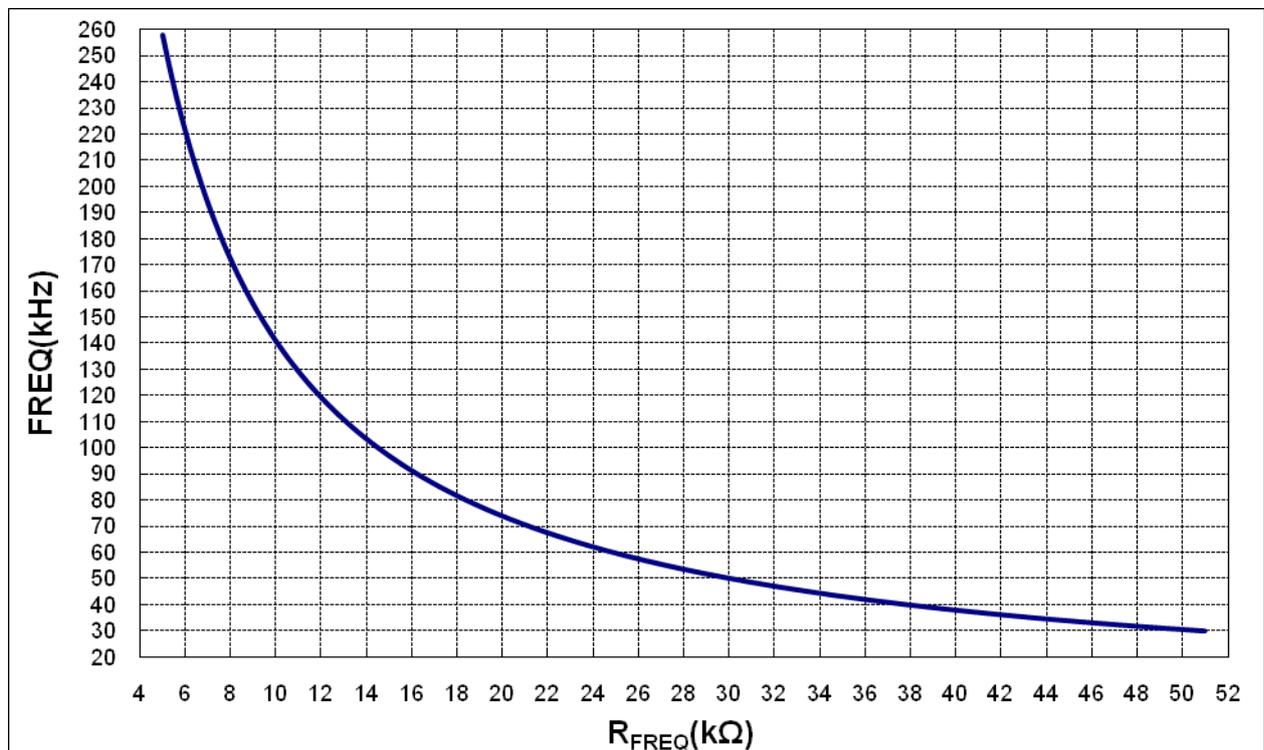

Figure 3 $FREQ$ **Vs Effective Resistor** R_{FREQ}

2.3.2   Minimum/Maximum frequency setting:

As discussed in section 2.2.7, the lowest switching $f_{\min}$ will be seen in full load operation at $V_{in\_\min}$. In this section, how the $f_{\min}$ is actually set by the IC is explained.

Based on the definition of oscillator as in the datasheet and the external circuit around pin FREQ in Figure 1, the minimum switching frequency will be achieved when pin SS is 2V (usually after softstart), opto-coupler transistor is open and only $R_{F\min}$ is connected to pin FREQ. For $f_{\min} = 30kHz$, the corresponding R_{FREQ} found from Figure 3 is 50kΩ. A standard value resistor of 51kΩ is selected for $R_{F\min}$.

The maximum operation frequency can possibly be seen when maximum input voltage, say 425V, is applied, and the converter run in no load condition ($Q = 0$), if burst mode is disabled. The gain in this condition can be given as:

$$M_{\min} = \frac{V_{in\_nom}}{V_{in\_\max}} M_{nom} = \frac{400}{425} * 1 = 0.94$$

[14]

From the gain equation, we get:

$$G(F,Q) = \frac{F^2(m-1)}{(F^2 m - 1)} = M_{\min}, (Q = 0)$$

[15]

The corresponding normalized frequency $F_{\max}$ can be found by:

$$F = \sqrt{\frac{1}{1 - m + mM_{\min}}} = 2.13$$

Therefore $f_{\max} = F * 85kHz = 180kHz$.

For 180 kHz switching frequency, the corresponding equivalent resistance R_{eq} at FREQ pin is 7.5kΩ according to Figure 3. Under no load normal operation, pin SS is already 2V after soft start, and collector of opto-coupler transistor is pulled to ground, therefore

$$R_{eq} = R_{FMIN} \,//\, R_{reg}$$

The R_{reg} is calculated to be 8.8kΩ. A standard value resistor of 8.2kΩ is selected for the actual design.

2.3.3 Frequency setting for OCP:

Assuming the maximum rms current during over-current should be limited by the IC to 1.2 times the maximum normal operation, i.e.

$$I_{ocp\_rms} = 1.2 I_{in\_rms\_\max} = 1.2 * 2.06 = 2.47A$$

The corresponding impedance of the resonant network during over-current can be estimated as:

$$Z_{ocp} = \frac{V_{in\_rms}}{I_{ocp}} = \frac{400 * \sqrt{2}}{\pi * 2.47} = 73\Omega$$

[16]

During over-current, the load impedence is considered to be shorted, and thereofore the impedance of the resonant network can be calculated as:

[17]

$$Z_{ocp} = \left| j * 2\pi f_{ocp} * L_r + \frac{1}{j * 2\pi f_{ocp} * C_r} \right| = 2\pi f_{ocp} * L_r - \frac{1}{2\pi f_{ocp} * C_r}$$

Solve the equation and find $f_{ocp} = 250kHz$

Then R_{eq} is 5kΩ according to Figure 3. According to the definition of over-current protection,

$$R_{eq} = R_{FMIN} // R_{ocp},$$

Then R_{ocp} can be found as 5.6kΩ.

2.3.4 Dead time

The dead time selection should ensure ZVS of two primary-side MOSFET IPA60R199CP at maximum switching frequency, where the magnetizing current to charge and discharge C_{ds} is the minimum. The magnetizing current at the end of each switching cycle can be calculated as:

$$I_{mag\,min} = \frac{(V_O + V_{ds}) * N_e}{4 L_p f_{ocp}} = \frac{(12 + 0.1) * 16.5}{4 * 690 * 10^{-6} * 250 * 10^3} = 0.288A \qquad [18]$$

The required time to charge and discharge the C_{ds} is:

$$T_{DEAD} = \frac{2 C_{ds} V_{innom}}{I_{mag\,min}} = \frac{2 C_{ds} V_{innom}}{I_{mag\,min}} = \frac{2 * 160 * 10^{-12} * 400}{0.288} = 440ns \qquad [19]$$

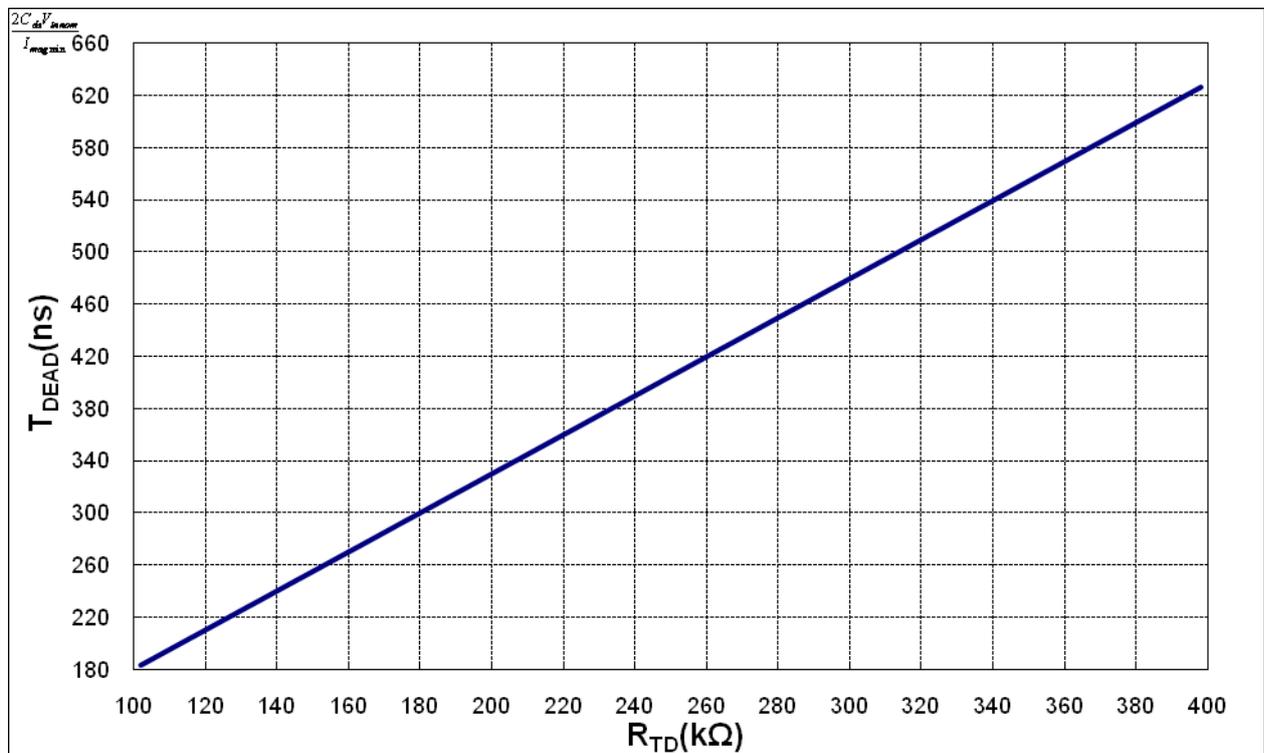Then R_{TD} is around 270kΩ according to Figure 4.

Figure 4 T_{DEAD} Vs R_{TD}

2.3.5 Softstart time, OLP blanking time and auto-restart time

According to the definition of the softstart of the IC in the datasheet, soft start is implemented by sweeping the operating frequency from an initial high value until the control loop takes over. The softstart time depends on a few components, such as the $R_{F\min}$, the value of R_{ocp} and the value of C_{SS}. For a 20ms target rising time of the output voltage, the customer can start with $C_{SS} = 2.2uF$.

The Timer pin is used to set the blanking time T_{OLP} and restart time $T_{restart}$ for over load protection. The RC parallel circuit, C_T and R_T, are connected to this pin. Based on the definition in the datasheet, the OLP blanking time with $R_T = 1M\Omega$ and $C_T = 1uF$ can be calculated as:

$$T_{OLP} = 20ms - R_T * C_T * \ln(1 - \frac{V_{TH}}{R_T * I_{BL}}) = 20 - 1000 * 10^6 * 10^{-6} * \ln(1 - \frac{4}{10^6 * 20 * 10^{-6}}) = 240ms$$

The restart time can be calculated as:

$$T_{restart} = -R_T * C_T * \ln(\frac{V_{TL}}{V_{TH}}) = -10^6 * 10^{-6} * \ln(\frac{0.525}{4}) * 1000 = 2030ms$$

2.3.6 Load pin setting

One of the functions of the LOAD pin is to detect the over-load or open-loop faults. Once the voltage at this pin is higher than 1.8V, IC will start internal and external timer and determine the entering of protection mode. The resistor divider R_{FT1} and R_{FT2} should be designed properly to ensure OLP is functional as required. The bottom resistor R_{FT2} connected to GND pin should be far bigger than the R_{FMIN}, in order not to affect normal regulation. As an example, assuming $R_{FT2} = 2M\Omega$, the target voltage at Load pin is 1.82V when overload happens. The reference voltage at frequency pin is 2V. Then the voltage at LOAD pin

$$V_{LOAD} = \frac{R_{FT2}}{R_{FT1} + R_{FT2}} * 2 = 1.82V \qquad [20]$$

We can find $R_{FT1} = 0.2M\Omega$. A small capacitor of 1nF is usually connected to decouple noise at LOAD pin.

2.3.7 Current sense
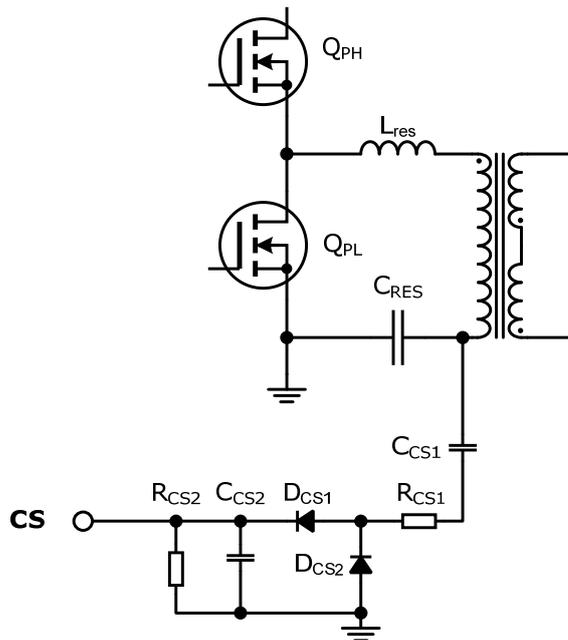
Figure 5   Current sense circuit

Assuming capacitive current divider is adopted as current sense circuit. So C_{cs1} is chosen to be far less than C_r ,e. g, around $C_r/100$, say 470pF. R_{cs1} is normally of a few hundred Ω for filtering purpose, say 200Ω.

We can obtain the following equation considering C_{cs1} and C_r as current divider:

$$I_{C_{cs1}} = I_{ocp}\frac{C_{cs1}}{C_{cs1}+C_r} \approx I_{ocp}\frac{C_{cs1}}{C_r} \qquad\qquad [21]$$

One major design criterion for the current sense is to ensure Over-Current Protection (OCP). Accordingly, we can also obtain:

$$I_{C_{cs1}} = \frac{\pi}{2}I_{R_{cs2}} = \frac{\pi}{2}*\frac{0.8}{R_{cs2}} \qquad\qquad [22]$$

where 0.8V is the OCP first level.

Then we get:

$$R_{cs2} = \frac{0.8\pi}{2*I_{ocp}}*\frac{C_r}{C_{cs1}} = \frac{0.8\pi}{2*2.47}*\frac{66*10^{-9}}{470*10^{-12}} = 70\Omega \qquad\qquad [23]$$

Rcs2 is chosen as 68Ω.

C_{cs2} is selected so that the current loop speed is fast enough and the ripple on CS pin is around 20% of the average value. $R_{cs2}*C_{cs2}$ is around $\frac{1}{f_{min}}$.

$$C_{cs2} \approx \frac{1}{R_{cs2}*f_{min}} = \frac{1}{68*30*10^3} = 490nF$$

2.3.8 VINS pin setting

The minimum operation input voltage needs to be specified for LLC resonant converter with the Vins pin. The typical circuit of mains input voltage sense and process is shown Figure 6.
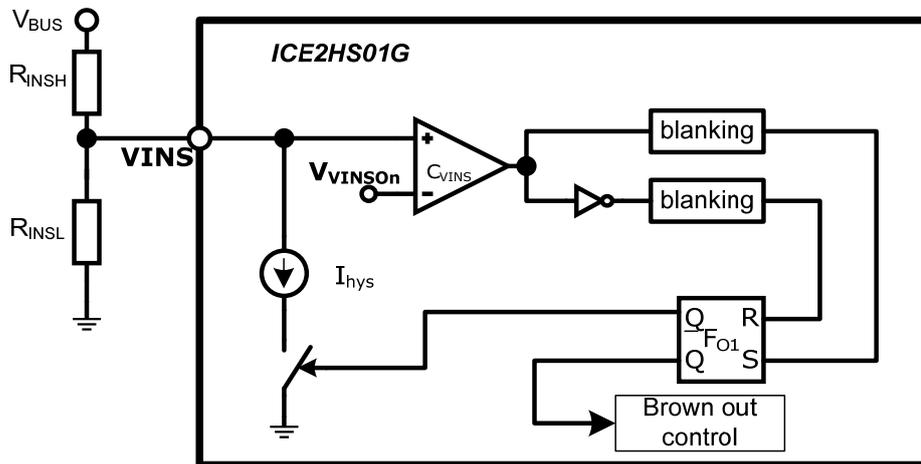

Figure 6   Mains input voltage sense

The mains input voltage is divided by R_{INSH} and R_{INSL}. With the internal current source I_{hys} is connected between VINS and Ground, an adjustable hysteresis between the on and off input voltage can be created as

$$V_{hys} = I_{hys} * R_{INSH}$$ [24]

Assuming the turn-on bus voltage V_{INon} is 380V typically and the turn-off bus voltage V_{INoff} is 320V typically. The R_{INSH} and R_{INSL} can be calculated as:

$$R_{INSH} = \frac{V_{INon} - V_{INoff}}{I_{INS}} = \frac{380 - 320}{10 * 10^{-6}} = 6M\Omega$$ [25]

$$R_{INSL} = \frac{V_{th} R_{INSH}}{V_{inoff} - V_{th}} = \frac{1.25 * 6 * 10^6}{320 - 1.25} = 23.5k\Omega$$ [26]

A standard resistor value for R_{INSL} is 24kΩ.

The blanking time for leaving brown-out is around 500µs and for entering brown-out is around 50µs. Please note that the calculation above is based on typical specification values of the IC.

2.3.9 Latch off function and burst mode selection

Internally, the EnA pin has a pull-up current source of 100µA. By connecting a resistor outside from this pin to ground, certain voltage level is set up on this pin. If the voltage level on this pin is pulled down below certain level during operation, IC is latched. If the external resistor has a negative temperature coefficient, this pin can be used to implement over- temperature protection (OTP). In this design, R_{EnA} is selected at 1MΩ to set the pin voltage to be 2V level and no OTP is designed.

In addition to the latch-off enable function, this pin is also built for the selection of burst mode enable or not during configuration before softstart. If the burst mode is enabled, the gate drives will be disabled if LOAD pin voltage falls below 0.12V. However, if burst mode is not selected, the gate drives will not be stopped by LOAD pin voltage.

The selection block works only after the first time IC VCC increases above UVLO. After CVCC is higher than turn on threshold, a current source I_{sele}, in addition to the I_{EnA}, is turned on to charge the capacitor C_{EnA}. After 26μs, IC will compare the voltage on EnA pin and 1.0V, if voltage on EnA pin is higher than 1.0V, the burst mode function will be enabled. As the voltage on EnA pin depends on R_{EnA} and C_{EnA}, by selecting different capacitance value, whether this IC works with burst mode can be decided. With $R_{EnA} = 1M\Omega$ and $C_{EnA} = 1nF$, the voltage at EnA pin at the time of 26us can be calculated as:

$$V_{EnA} = I_{sele} * R_{EnA}(1 - e^{-\frac{26*10^{-6}}{RC}}) = 100*10^{-6}*10^6*(1 - e^{-\frac{26*10^{-6}}{10^6*10^{-9}}}) = 2.56V > 1.0V$$

Therefire burst mode will be enabled. If C_{EnA} is set to be 10n F, $V_{EnA} = 0.26V < 1.0V @ 26us$ thus burst mode will be disabled.

After the selection is done, the current source I_{sele} is turned off. A blanking time of 320μs is given before IC starts to sense the EnA pin voltage latch off enable purpose. This blanking time is used to let the EnA pin votlage be stablized to avoid mistriggering of Latch-off Enable function.

2.4 Design of Synchronous Rectification (SR) control

Synchronous Rectification (SR) in a half-bridge LLC resonant converter is one of the key factor to achieve high efficiency. SR control is a major benefit we offer with our new LLC controller IC ICE2HS01G.

Before going into details of SR control of the IC, it's necessary to understand the ideal SR switching mechanism for two typical working conditions, i.e. when operation frequency(f_{sw}) is below ($f_{sw} < f_r$) and above the resonant frequency ($f_{sw} > f_r$).Figure 7 illustrates the waveforms of V_{HG} (primary high side gate), V_{LG} (primary low side gate), V_{SHG} (secondary high side gate), V_{SLG} (secondary low side gate), I_{SH} (current flowing through secondary high side MOSFET), I_{SL} (current flowing through secondary low side MOSFET) and I_{PRI} (current flowing through primary resonant tank).
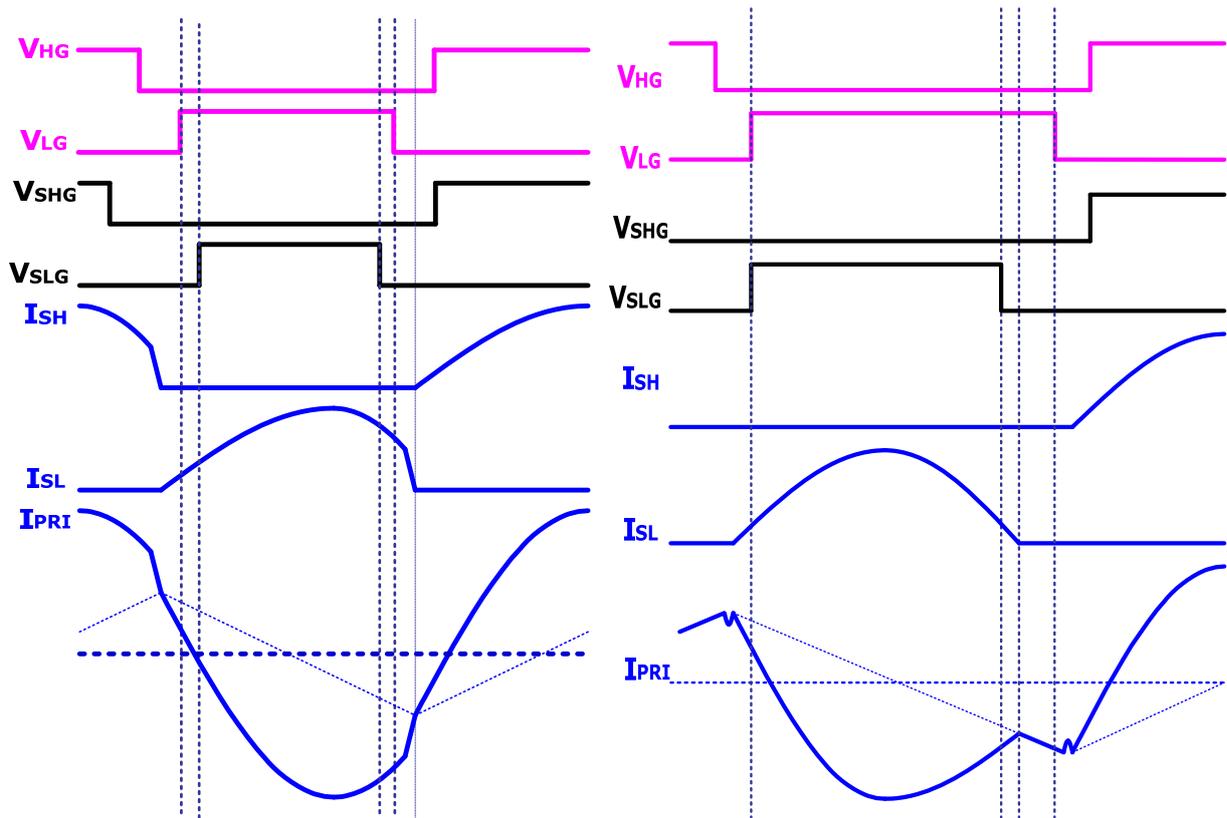
Figure 7   Waveforms for LLC converter with $f_{sw} > f_r$ (left) and $f_{sw} < f_r$ (right)

It can be seen from the waveforms in Figure 7 (left) that to ensure safe switching, the switch-on of the SR MOSFET (see V_{SLG}) need to be a certain time AFTER the switch-on of the primary side switch(see V_{LG}); while switch-off of the SR MOSFET(see V_{SLG}) needs to be certain time BEFORE the switch-off of primary side switch(see V_{LG}), in order to compensate the propagation delay of the gate signals from IC to the actual MOSFET. In this operation condition ($f_{sw} > f_r$), the SR MOSFET conduction period (on-time) depends on the primary gate switching frequency.

From Figure 7 (right), the current flowing through the SR MOSFET (see I_{SL}) goes to zero before the switch-off of the primary switch. To avoid the current going into negative, the SR MOSFET need to be turn off just before the current goes to zero. In this condition, the SR MOSFET on-time is almost constant and nearly half of the resonant period.

The control of SR in ICE2HS01G consists of four main parts: on-time control, turn-on delay, advanced turn-off delay and protections, with the block diagram shown in Figure 8.

Figure 8   Synchronous rectification control block diagram

2.4.1   On-time control - SRD pin and CL pin

With ICE2HS01's control scheme, SR MOSFET 's turning-off depends on two conditions - turning-off of the primary gate and the "off" instruction from SR on-time block, where the maximum on-time T_{on_max} is preset. Whichever "off" instruction comes first will trigger the turn-off of the SR MOSFET.

As illustrated in the previous chapter, the T_{on_max} depends on the resonant frequency when LLC converter operates below resonant frequency ($f_{sw} < f_r$). Considering the primary side dead time T_{DEAD} and the SR gate turn-on delay T_{on_delay} (will be discussed later section 2.4.2), we can preset T_{on_max} with a safe value as below:

$$T_{on\_max} < \frac{1}{2f_{res}} - T_{DEAD} - T_{on\_delay} = 5.88 - 0.32 - 0.25 = 5.31us \qquad [27]$$

To achieve higher efficiency, a bigger T_{on_max} is an advantage, because bigger on-time means longer SR MOSFET conduction time and less body diode conduction time, which reduces conduction loss. In actual design, T_{on_max} can be fine-tuned by looking at the similar waveforms in Figure 7, as long as safe switching is guaranteed.

From Figure 9 below, R_{SRD} is selected to be 66kΩ to achieve $T_{on\_max} = 5.31us$. Usually customer should start with a smaller SR on time for safety and then adjust it to achieve higher efficiency.
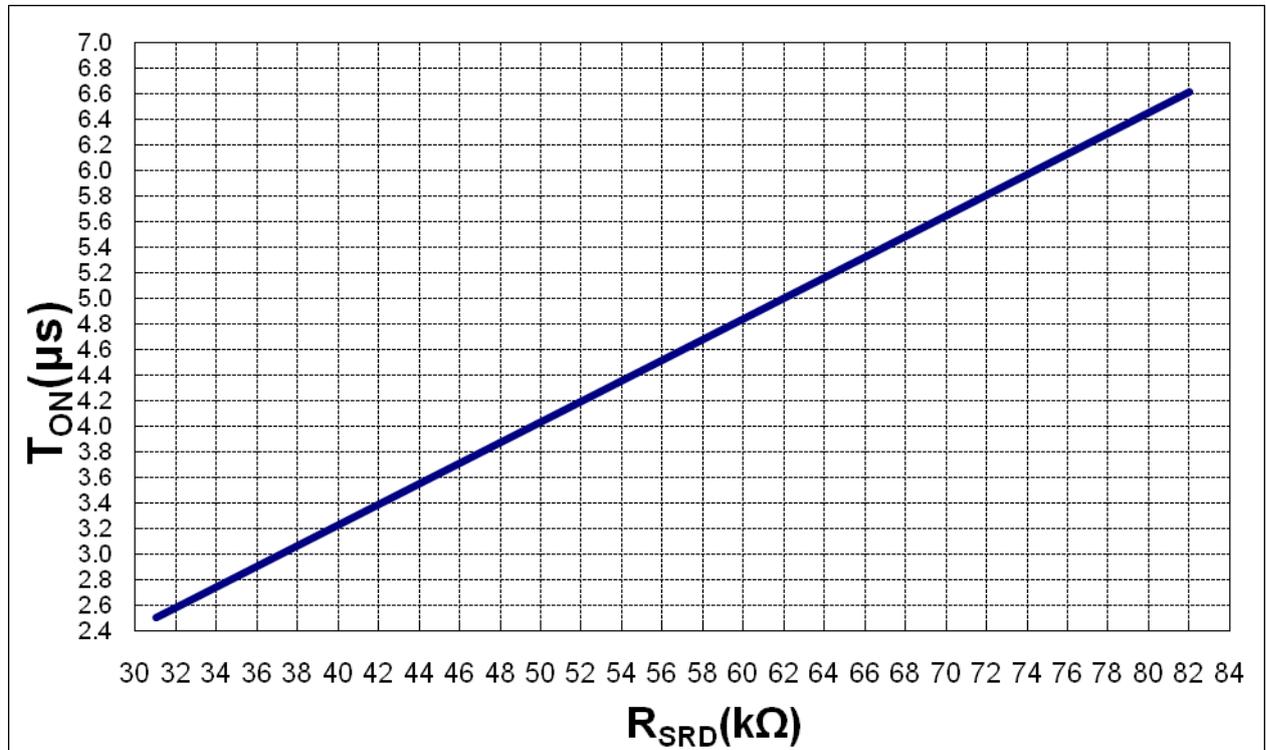
Figure 9   SR on time versus SRD resistance

A simple constant on time control does not provide the best efficiency of LLC HB converter for the whole load range. In fact, the actual resonant period of secondary current reduces when the output load decreases or input voltage increases. The primary winding current can reflects this change. The current sense circuit can be designed to get such information and input to CS pin. In ICE2HS01G, a function called current level (CL) pin is implemented. During heavy load and low input voltage, the CL pin voltage (V_{CL}) is clamped at same voltage of SRD pin, 2V. Therefore, the SR on time in such conditions is determined by R_{SRD} only and is equal to T_{on_max}. In case of light load, with low CS voltage(V_{CS}), the V_{CL} is reduced to be lower than 2V and extra current will be drawn from SRD pin, thereby the actual SR on time is reduced. The relationship between V_{CS} and V_{CL} is shown in Figure 10(top). The resistor R_{CL} can be adjusted to find the suitable reducing speed of SR on time for either better reliability or better efficiency. R_{CL} is normally around 10 times R_{SRD}, which is 680kΩ in this design. Below is the detailed calculation for the 300W design example:

We obtain the V_{CS} for full load condition, based on the circuit in Figure 5:

$$V_{cs} = \frac{2R_{cs2} * I_{in\_rms\_max}}{\pi} * \frac{C_{cs1}}{C_r} = \frac{2*68*2.06}{\pi} * \frac{470*10^{-12}}{66*10^{-9}} = 0.635V$$

The corresponding V_{CL} is clamped at 2V according to Figure 10(top) and the SR on time is T_{on_max}.

Then for V_{CS} = 0.4V where V_{CL} is exactly 2V, the corresponding load is 63% of the full load, which is around 16A output current(Figure 10, bottom).

With V_{CS} < 0.4V, V_{CL} starts to drop below 2V, extra current is drawn from SRD pin, thereby the actual SR on time is reduced with the load decreased.

For filter purpose, C_{CL} is chosen to be 47nF.
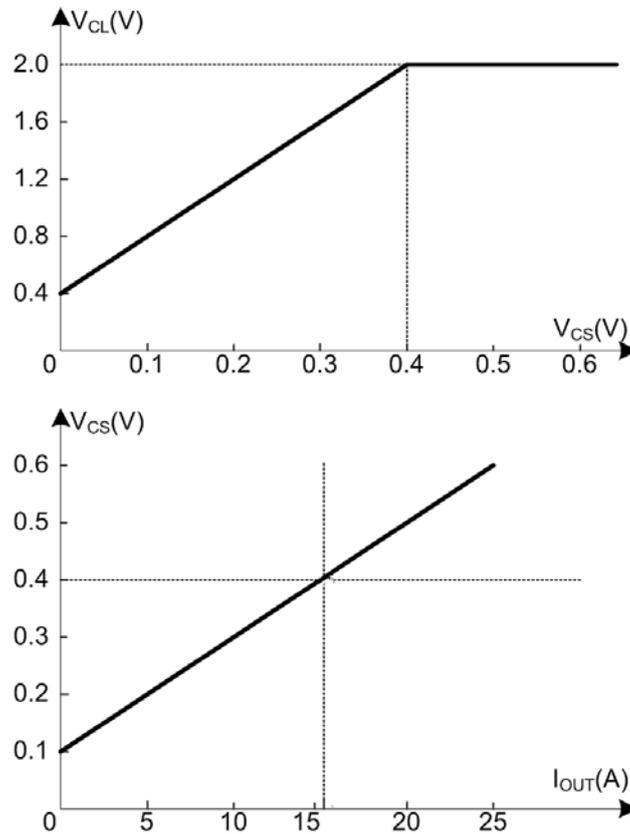
Figure 10   SR on time versus SRD resistance

2.4.2   Turn-on delay T_{on_delay} - Vres pin

When the input voltage is higher than resonant voltage, the LLC converter secondary switches are working in CCM condition. Certain recovery time of the SR MOSFET body diode is required depending on the current to turn-off. For better performance, the other SR MOSFET should be turn on after the recovery phase. The turn-on delay function is built in ICE2HS01G for such purpose. When the sensed input voltage at VINS pin is higher than the reference voltage set by Vres pin according to the resonant voltage, SR turn-on delay is added, i.e, the SR MOSFETs are turn on 250ns after the corresponding primary MOSFETs are turned on.

The nominal bus voltage at resonant point is:

$$V_{res} = 2n*(V_O + V_f) = 2*16.5*(12 + 0.1) = 399.3V$$ [28]

The corresponding voltage at VINS pin is 1.59V. To allow the turn-on delay for input voltage above this resonant point, we can set the voltage divider R_{res1} and R_{res2} connected at VRES pin accordingly. We select $R_{res1} = 12k\Omega$, and R_{res2} can be calculated to be 5.2kΩ. To disable the turn-on delay during normal operation, we can set the voltage at V_{res} to be 1.07x1.59=1.7V. Accordingly, $R_{res1} = 12k\Omega$, and $R_{res2} = 6.2k\Omega$.

2.4.3 Advanced Turn off delay T_{off_delay} - Delay pin

Advanced turn-off delay time of the SR MOSFET T_{off_delay}, normally is determined by the propagate delay and transition time in the actual converter system. The value of T_{off_delay} can be set by the Delay pin. For example, if the delay time required is 220ns, a $R_{delay} = 33k\Omega$ need to connect at Delay pin according to the curve below.
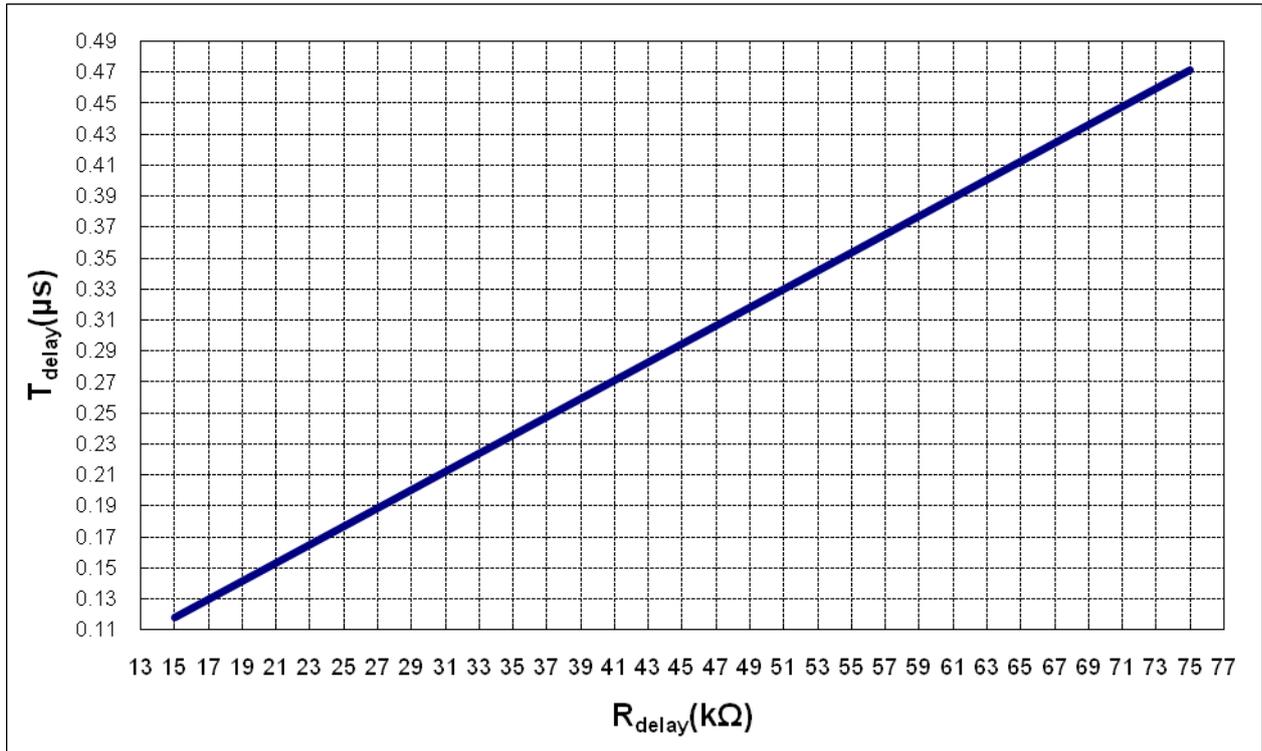

Figure 11   Turn-off delay time versus Rdelay

2.4.4 A review of the control scheme

After all the SR related parameters have been set, such as maximum on-time T_{on_max}, turn-on delay T_{on_delay}, advanced turn-off delay T_{off_delay}, simplified typical waveforms can be drawn in Figure 12 for the two conditions when $f_{sw} > f_r$ and $f_{sw} < f_r$.

From the waveforms on the left, the switch-on of the SR MOSFET is T_{on_delay} after the switch-on of the primary side switch; while switch-off of the SR MOSFET is in advance with T_{off_delay} to the switch-off of primary side switch. Under this operation condition, the SR MOSFET's on-time changes with the primary side MOSFET gate switching.

From the waveforms on the right, the SR MOSFET on-time is almost **constant** and equal to T_{on_max}, which is independent of the primary side MOSFET turn-off.

In actual operation, the f_{sw} doesn't have to be monitored. SR MOSFET will be turned off by whichever signal comes first – the turning-off of the primary gate, or the falling edge of T_{on_max}.
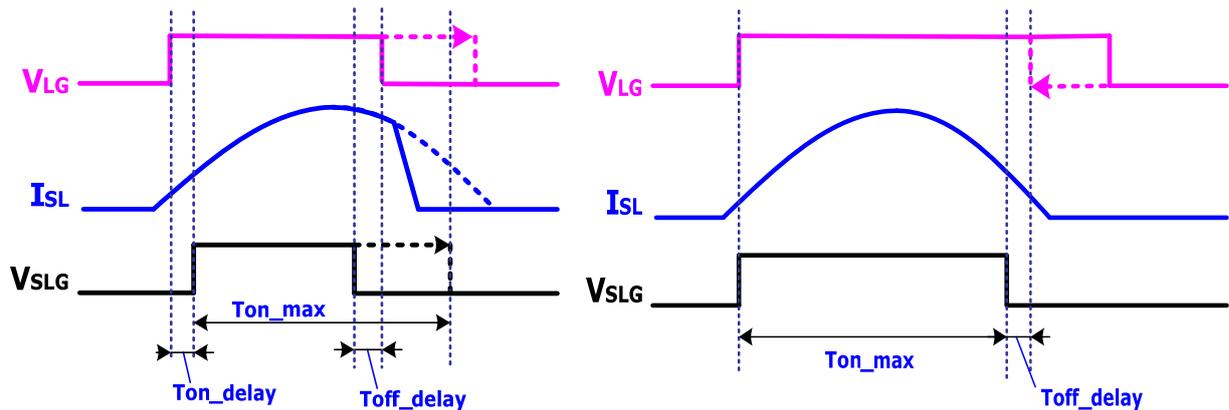
Figure 12 **Waveforms for LLC converter with** $f_{sw} > f_r$ **(left) and** $f_{sw} < f_r$ **(right)**

2.4.5 SR Protections

As the SR control in ICE2HS01G is realized with indirect method, there are some cases that the SR can not work properly. In this cases, the SR gate drive will be disabled. Once the condition is over, IC will restart the SR with SRSoftstart.

During softstart, the SR is disabled.When the softstart pin voltage is higher than 1.9V for 20ms, SR will be enabled with SRSoftstart.

When LOAD pin voltage is lower than 0.2V, IC will disable the SR immediately. If LOAD pin voltage is higher than 0.7V, IC will resume SR with SRSoftstart.

During over-current protection phase, if the softstart pin voltage is lower than 1.8V, SR will be disabled. The SR will resume with softstart 10ms after SS pin voltage is higher than 1.9V again.

In over-current protection, if the CS pin voltage is higher than 0.9V, SR is disabled. SR will be enabled with SRSoftstart after CS pin voltage is lower than 0.6V.

All the above four conditions are built inside the IC. If IC detects such a condition, IC will disable SR and pull down the voltage on SRD pin to zero.

When the CS voltage suddenly drops from 0.55V to below 0.30V within 1ms, the SR gate is turned off for 1ms, after 1ms, SR operation is enabled again with SRsoftstart.

If some fault conditions are not reflected on the four conditions mentioned above but can be detected outside with other measures, the SR can also be disabled and enabled with softstart from outside. This is implemented on SRD pin as well. The internal SRD reference voltage has limited current source capability. If a transistor QSRD is connected as shown in typical application circuit, the voltage on SRD pin can be pulled to zero if this transistor is turned on, which will stop the SR. If the SRD voltage is released and increases above 1.75V, SR is enabled with softstart.

2.5 Design summary

Figure 13 and 14 show the final schematic for the power stage and control circuit for the 300W LLC converter.
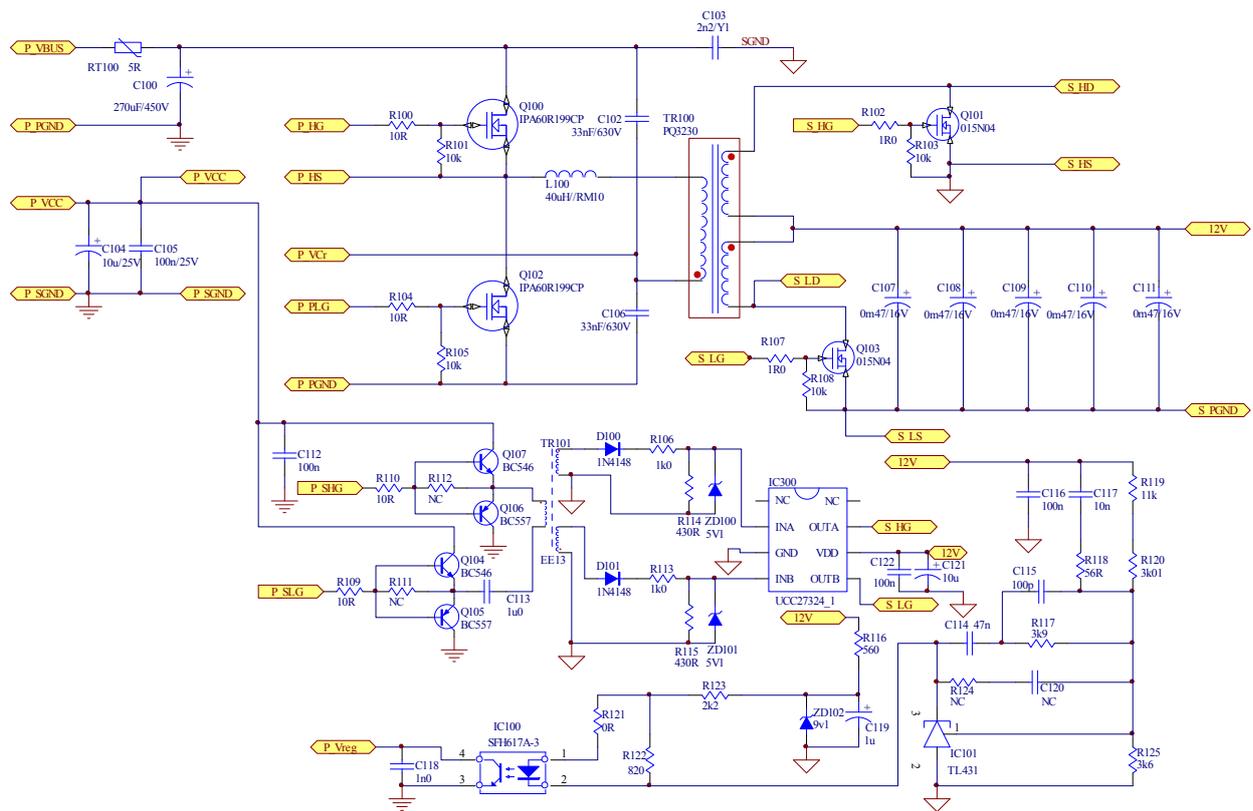
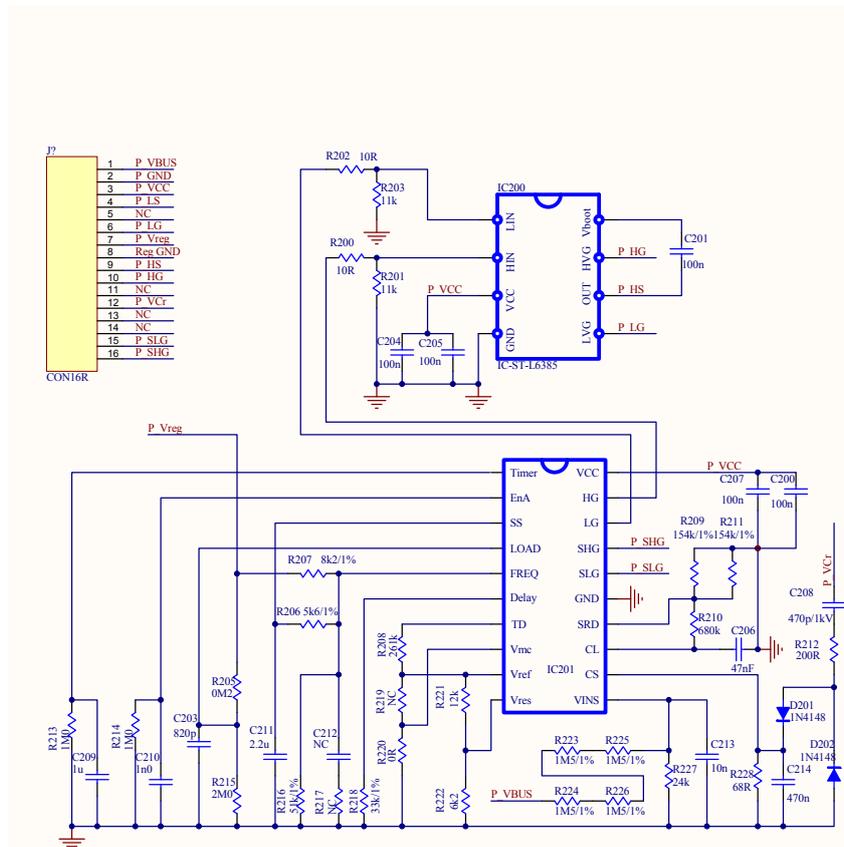**Figure 13   Power stage circuit of the half-bridge LLC converter**

Figure 14   Control circuit of the half-bridge LLC converter

3 Tips on PCB layout

In order to avoid crosstalk on the board between power and signal path, and to keep the IC GND pin as "clean" from noise as possible, the PCB layout must be taken care of properly. Below are some suggestions as reference and customer can modify based on their own experience.

3.1 Star connection for Power stage

1. Connect IC VCC Ecap ground to both buck cap. ground and IC VCC ground (please refer to the red curves in the circuit diagram below)

2. Connect driver IC input ground to IC VCC Ecap ground

3. Connect driver IC output ground to low side MOS source with short path

4. A 100nF filtering cap should be located just near IC VCC & IC GND (refer to the purple arrow)

5. The 100nF filtering cap ground should be inserted between VCC Ecap ground and IC ground

6. Connect driver IC VCC to VCC Ecap(refer to the green curve)

7. Connect driver IC high side output source to half bridge midpoint directly with short path

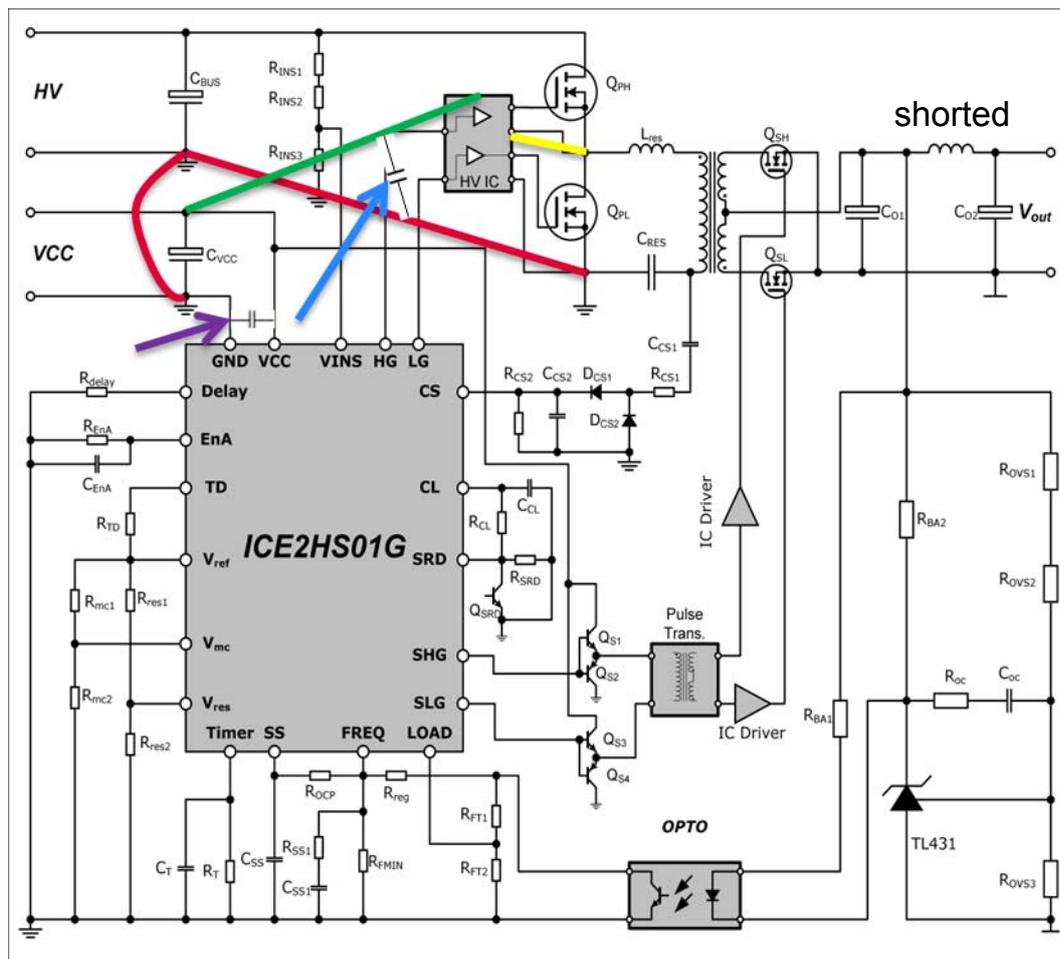8. A 100nF filtering cap should be located just near driver IC VCC and IC GND(refer to the blue arrow)

Figure 15 PCB layout tips

3.2   Star connection for IC

1. Connect the following ground directly back to Vcc 100nF cap ground (please refer to the red curves in the circuit diagram below)

    - FREQ pin resistor ground

    - Delay pin resistor ground

    - SRD resistor ground

2. Connetc the following ground with $R_{F\min}$ ground(refer to the green curves)

    - SS cap ground

    - Opto-coupler ground

3. Connect SR pulse transformer and driving circuit ground to VCC Ecap ground(refer to the yellow curve)

4. Put 100nF ceramic cap to driver supply (refer to the blue arrow)

5. Connect all other ground using ground plane or ground track back to IC VCC 100nF cap ground or VCC E cap ground
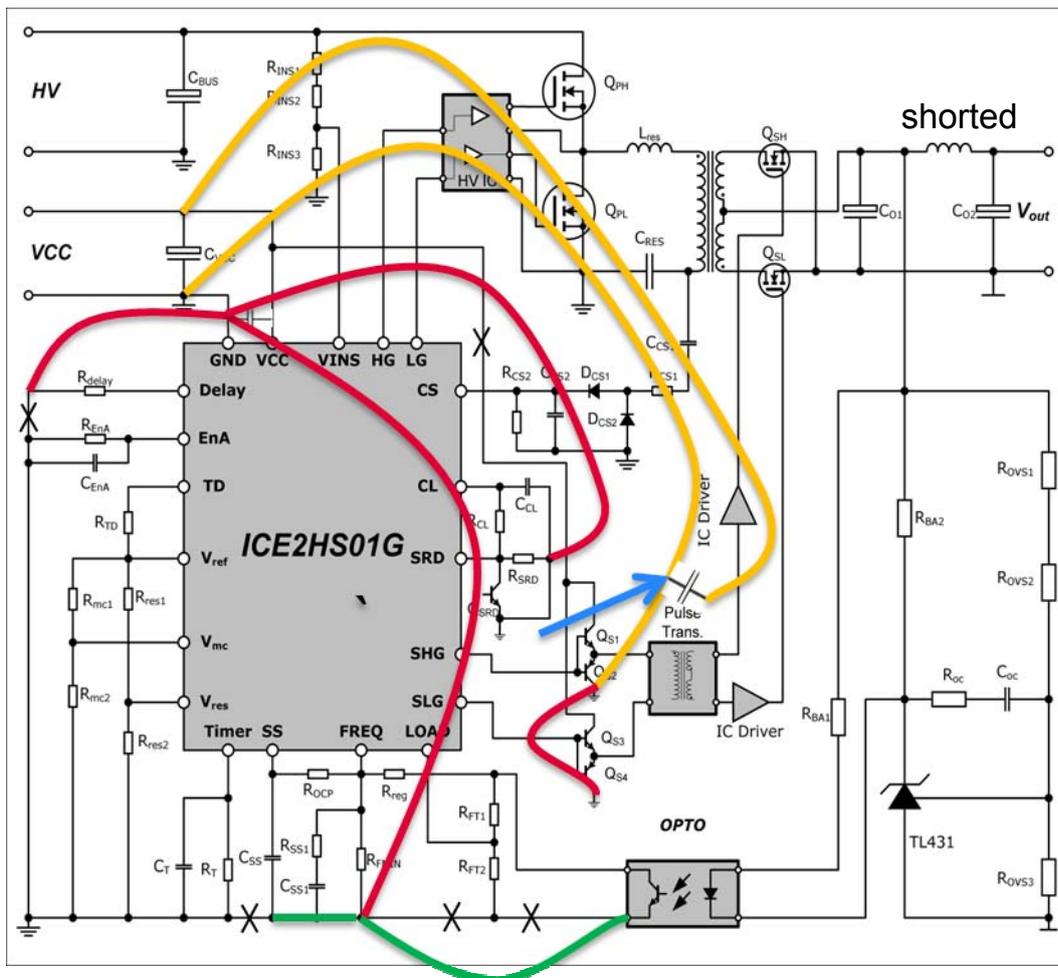

Figure 16   PCB layout tips

References

[1]   Infineon Technologies: ICE2HS01 - High Performance Resonant Mode Controller for Half-bridge
       LLC Resonant Converter; datasheet Ver 2.0; Infineon Technologies; Munich; Germany; May. 2010.