Never stop thinking

Infineon® Power LED Driver

TLD5095 / TLD5098 DC-DC Multitopology Controller IC

Dimensioning and Stability Guideline - Theory and Practice

Application Note

Application Note
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Automotive Power

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1 Introduction

Note: The following information is provided only as a guide for the implementation of the device and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

The aim of this application note is to provide a dimensioning guideline for TLD5095/98 applications. A 10-step approach has been developed to guide the reader through the calculation of external components and stability considerations (**Chapter 2** and **Chapter 3**). Furthermore, an efficiency and power loss summary (**Chapter 4**) completes the picture. To put the theory into practice, a typical example of application has been chosen, which should improve the understanding of the equations used. **Chapter 5** provides an overview of tools and further information, which could be very valuable for design-in activities and detailed evaluation of TLD5095/98 applications.

Note: The following considerations focus on the TLD5095/98 for a standard boost to GND application in constant current mode (CCM).

1.1 The 10-step approach for your TLD5095/98 application

We have developed a 10-step approach to help you find your way through the maze of formulas and equations. We proceed step by step to develop a stable switching and energy-efficient application considering all the application-specific boundary conditions. **Figure 1** displays the flow chart for the 10-step approach.

Note: The "10-step approach" is the one used to dimension a TLD5095/98 boost application. To optimize and further improve the system response, the entire procedure may be repeated several times! Thus, it is clear that this is an iterative procedure and, at times, more than one dimensioning cycle is required.

STEP 1: Get Application Information

Get in touch with your customer and obtain the boundary conditions for the specific application. Think carefully about the worst case conditions and try to avoid mapping worst case scenarios over worst case scenarios. Very detailed knowledge about the real application ensures greater flexibility for the dimensioning of the system. In our example, the boundary conditions are defined in **Chapter 2.1**.

STEP 2: Defining the Switching Frequency - f_{SW}

A DC/DC converter is also called a switched mode power supply (SMPS). Thus, switching is its main job. The selection of the system switching frequency is important for the selection of the external components (inductor and capacitor size). The system efficiency and the EMC performance are directly related to one another. The RF spectrum has some free areas in the 100 kHz to 500 kHz band. In our example, we switch at f_{SW} = 400 kHz. The TLD5095/98 features two different control options for fixing the switching frequency f_{SW}. Refer to **Chapter 2.2** for more details.

STEP 3: Calculating the Switching Duty Cycle - D

The input and output power balance of a DC/DC converter is controlled by the ON and OFF timing of the switching MOSFET. The ratio of the ON and OFF phases is called the switching duty cycle (DC). The DC can be calculated using a simplified formula or a more detailed equation. Both approaches for calculating the DC are described in **Chapter 2.3**.

STEP 4: Selection of the Boost Inductor - L_{BO}

An inductor is necessary to supply the output of a boost converter with the appropriate amount of power. To dimension the boost inductor L_{BO} you need to calculate the current flowing trough the inductor depending on the required input voltage condition. A worst-case condition, which results in a higher inductor value, is the minimum value of input supply voltage VIN and a lower switching frequency f_{SW}. The calculation of the proper boost inductor L_{BO} for the TLD5095/98 ICs also depends on the current loop stability and the value of the current sensing resistor R_{CS} that senses the current through the inductor. All the equations required for this purpose are furnished in **Chapter 2.4**.

STEP 5: Calculation and Selection of Output Capacitor - C_{OUT}

The output capacitor of a boost system is very important to maintain constant current flow through the load. The capacitance value at the given output voltage is crucial. The effect of a capacitor's DC bias is often underestimated. For selection of the proper C_{OUT} please refer to **Chapter 2.5**.

STEP 6: Calculation and Selection of Input Capacitor - C_{IN}

The value of the input capacitance C_{IN} of a boost converter is generally selected to limit the input voltage ripple ΔV_{IN} required by the specification. For proper dimensioning please refer to **Chapter 2.6**.

STEP 7: Select Other External Components such as MOSFET, R_{FB}, R_{OVL}, R_{OVH}, D_{BO}

The selection of the switching MOSFET, freewheeling diode D_{BO}, load current defining shunt resistor R_{FB} and the over-voltage protection resistors R_{OVL}, R_{OVH} plus gate buffer capacitance C_{IVCC} is described in **Chapter 2.7** to **Chapter 2.11**.

STEP 8: Determine the Compensation Network - R_{COMP}, C_{COMP1}, C_{COMP2}

The external compensation network provides the flexibility to ensure a stable application with respect to various boundary conditions. The calculation of the open loop gain and the corresponding phase margin PM and the influence of the compensation network are explained in **Chapter 3**.

STEP 9: Calculate Power Loss and System Efficiency

After dimensioning the external components and the selection of the actual parts used to build up a TLD5095/98 application, the system power loss and efficiency can be determined. The method for this is illustrated in **Chapter 4**.

STEP 10: Verify the Application with Simulations and Measurements

Before building prototype hardware, it is useful to perform system simulations (e.g. SPICE simulations). A thermal system evaluation, too, could be beneficial. Infineon provides several design-in tools to simplify the usage of the TLD5095/98 products. A summary of the available design-in tools is presented in **Chapter 5**.

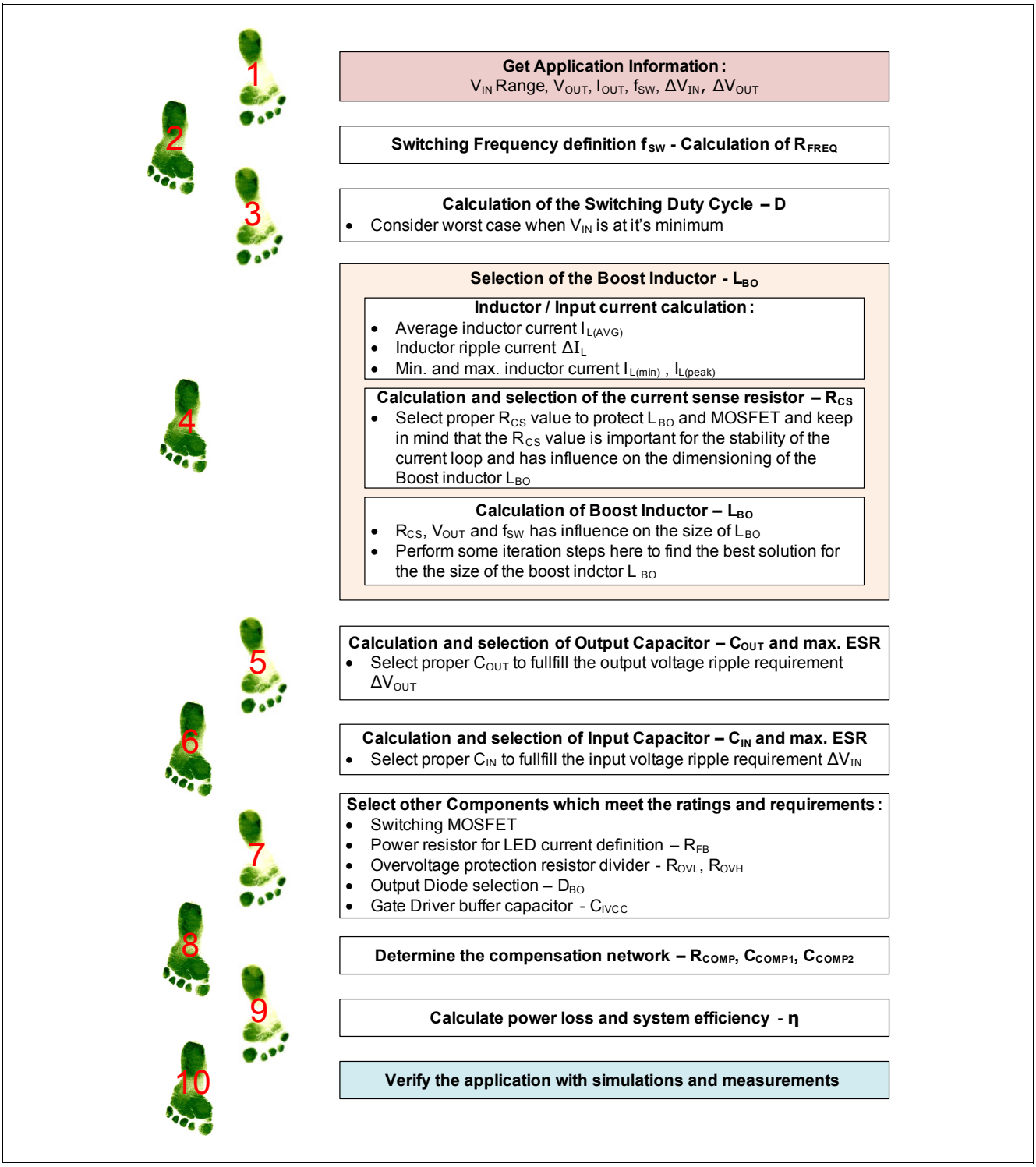


Figure 1 Proposed procedure for selecting external components

2 Calculation of external components for a TLD5095/98 application

The following chapter provides a detailed overview of the formulas that are used to achieve proper dimensioning of all external components used to build up a DC/DC boost application featuring the TLD5095/98. In addition, a sample calculation demonstrates the usage of these formulas. An Excel sheet including all formulas below can be provided on request. Refer to **Chapter 5** to get an overview of other support tools and info material.

Only constant current mode (CCM) is taken into account for further considerations.

2.1 Example: Automotive LED application

A typical automotive exterior light application these days is the Daytime Running Light function. Most of the OEM's introduce LED lights to establish brand recognition and achieve extraordinary headlamp design solutions. **Figure 2** below illustrates an eye-catching OEM example of a DRL application.

Figure 2 Daytime running light example - source: AUDI AG

2.1.1 Application boundary conditions:

*Note: The following example of an application boundary condition is independent of the picture illustrated in **Figure 2**.*

- Sum of LED forward voltage = output voltage V_{OUT} = 40 V.
- Supply input voltage V_{IN} is specified in the range 8 V < V_{IN} < 16 V. The typical value is usually 12 V.

Note: Many calculations must consider the worst case input voltage condition to achieve a design that works properly over the entire input voltage range. Therefore, many calculations consider 8 V (= lowest input voltage is the worst case for boost converters).

- LED current or output current I_{OUT} should be 400 mA.
- Switching frequency f_{SW} of the DC/DC converter is 400 kHz.
- Boost to GND application is used according to **Figure 3** below.

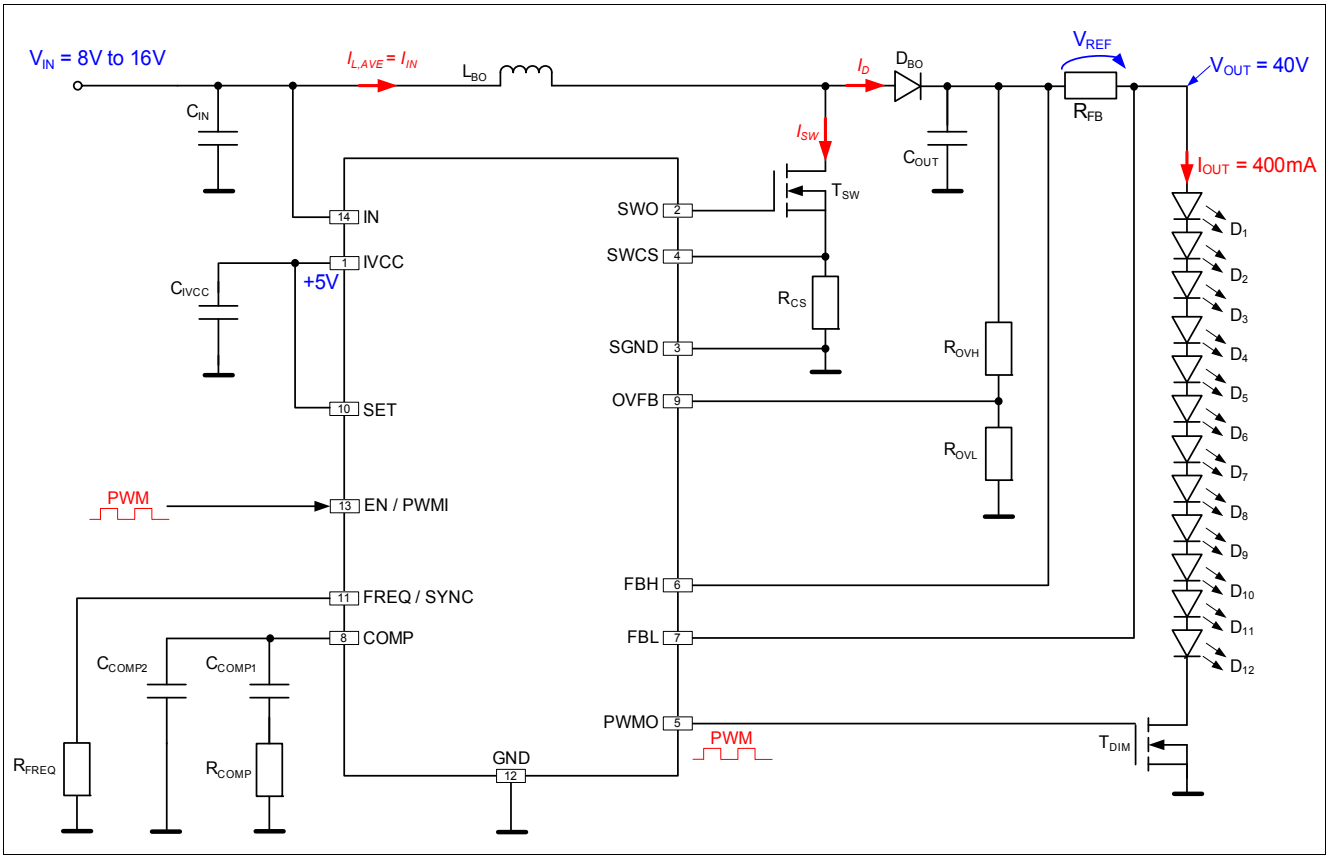


Figure 3 Example: B2G configuration

A summary of the application boundary condition, which should be the basis of the values used in our example for better understanding of the upcoming equations, is presented in **Figure 4** below.

INPUTS			
Symbol	**Value**	**Unit**	**Name**
V_{IN}	12,00	V	Input Voltage
V_{out}	40,00	V	Output Voltage
I_{out}	0,40	A	Output Current
f_{sw}	400,00	kHz	Switching Frequency
ΔV_{OUT}	100,00	mV	Max. allowable Ripple Voltage on V_{OUT}
ΔV_{IN}	100,00	mV	Max. allowable Ripple Voltage on V_{IN}
$\Delta I_{L\%}$	20,00%	%	Pk-Pk Inductor Ripple Current
V_{REF}	300,00	mV	Feedback reference voltage V_{REF}

Figure 4 Example: Typical input values

2.2 Switching frequency definition f_{SW} - calculation of R_{FREQ}

The regulator switching frequency f_{SW} of the TLD5095/98 can be adjusted via:

1) a simple resistor R_{FREQ} (for f_{SW} between 100 kHz and 500 kHz) or

2) an external clock signal generated by a µC port (V_{CLK} -> f_{CLK} between 250 kHz and 500 kHz).

The synchronization with an external clock signal can be beneficial if there are multiple DC/DC converters in a system. A defined phase shift strategy could improve EMC performance. **Figure 5** illustrates the two options for controlling the switching frequency.

*Note: The value of the boost inductor L_{BO} required is calculated differently for the two switching control methods. (Please refer to **Section 2.4.2** and **Section 2.4.3**)*

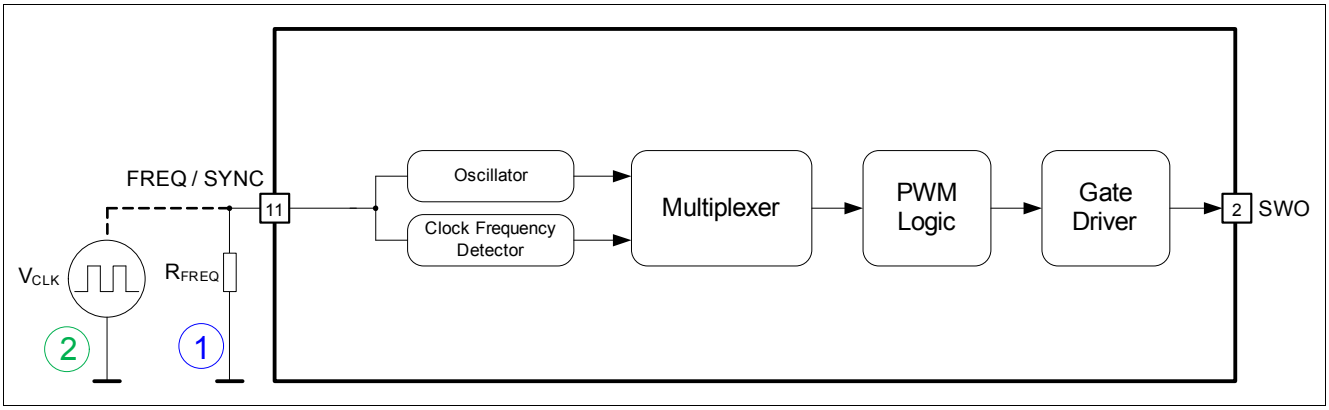


Figure 5 Two options for controlling the regulator switching frequency f_{SW}

The formula below expresses the mathematical relationship between the resistor R_{FREQ} and the switching frequency f_{SW} **Figure 6** provides a diagram for fast evaluation.

$$R_{FREQ} = \frac{1}{141 \cdot 10^{-12} F \cdot f_{SW}} - 3.5 \cdot 10^{3} \quad (1)$$

$$R_{FREQ} = \frac{1}{141 \cdot 10^{-12} F \cdot 400\,kHz} - 3.5 \cdot 10^{3} = 14.23\,k\Omega \quad (2)$$

Note: $141*10^{-12}F$: internal equivalent capacitance of the Oscillator

R_{FREQ}	f_{SW}
67.42 kΩ	100 kHz
43.78 kΩ	150 kHz
31.96 kΩ	200 kHz
24.87 kΩ	250 kHz
20.14 kΩ	300 kHz
16.76 kΩ	350 kHz
14.23 kΩ	400 kHz
12.26 kΩ	450 kHz
10.68 kΩ	500 kHz

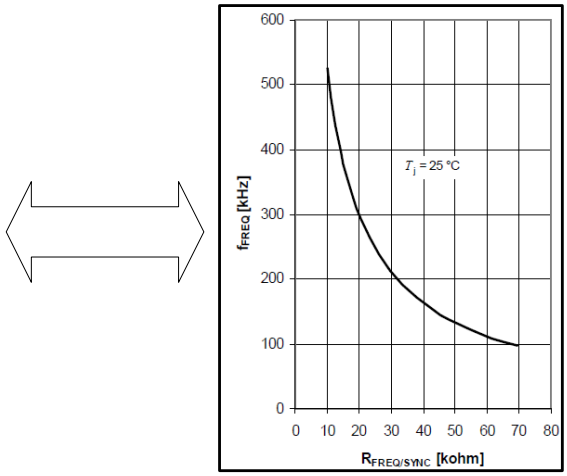


Figure 6 Switching frequency f_{SW} versus frequency selection resistor R_{FREQ} to GND

2.3 Calculation of the switching duty cycle - D

The first step is to determine the switching duty cycle, D, which is needed to generate a high output voltage V_{OUT} from a low input voltage V_{IN}. In principle, there are two approaches for calculating the duty cycle of the MOSFET boost switch.

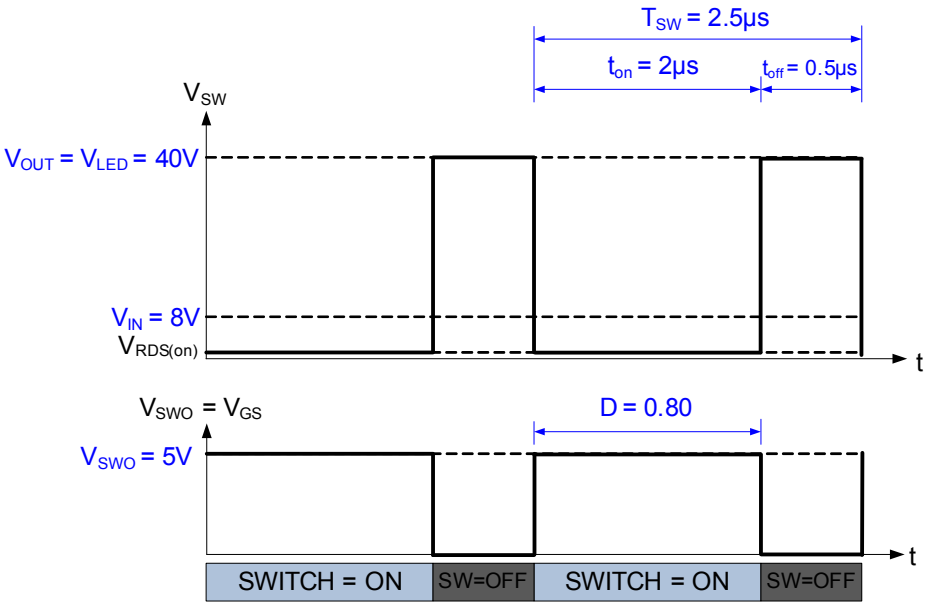


Figure 7 Switching MOSFET voltage V_{SW} and the switching duty cycle - D

1) Simplified equation:

This calculation approach merely focuses on the input and output voltage relation. In most cases, these results are sufficient and can be used for further calculations. (All the following considerations are based on this simplified equation.)

$$D \approx \frac{V_{OUT} - V_{IN}}{V_{OUT}} \tag{3}$$

The worst case evaluation considers the lowest input voltage $V_{IN(min)}$ and the highest output voltage $V_{OUT(max)}$ that can occur in a system. For further calculations, this worst case duty cycle is referred to as $D_{(worst\ case)}$. For some calculations, this parameter is required to ensure a proper dimensioning of the external passive components.

$$D_{(worstcase)} \approx \frac{40V - 8V}{40V} \approx 0.80 \tag{4}$$

The ON and OFF times of the switching MOSFET can be calculated on the basis of the duty cycle. The parameter T_{SW} is the switching period time and can be calculated from the given switching frequency:

$$T_{SW} = \frac{1}{f_{SW}} = \frac{1}{400kHz} = 2.5\mu s \tag{5}$$

$$t_{on} = D \cdot T_{sw} \tag{6}$$

$$t_{on} = 0.80 \cdot 2.5\mu s = 2\mu s \tag{7}$$

$$t_{off} = (1 - D) \cdot T_{sw} \tag{8}$$

$$t_{off} = (1 - 0.80) \cdot 2.5\mu s = 0.5\mu s \tag{9}$$

2) Detailed equation:

The **Equation (10)** below also considers the freewheeling diode forward voltage V_D and the voltage drop across the switching MOSFET in the ON-state $V_{RDS(ON)}$. During the initial evaluation stages of a DC/DC application, it is not known which switching MOSFET and freewheeling diode will be used. Therefore, it seems difficult to calculate a precise duty cycle at the initial stage. To complete the picture, some values have been chosen to demonstrate the difference between the two calculation approaches.

Assumptions:

- $R_{DS(ON)}$ of switching MOSFET = 26 mΩ; $V_{RDS(ON)} = R_{DS(ON)} * I_{RMS\_SW}$ = 30mΩ ∗ 1.79 A = **0.046 V**
- forward voltage drop of freewheeling Schottky diode V_D = **0.4 V**

$$D = \frac{V_{OUT} + V_D - V_{IN}}{V_{OUT} + V_D - V_{RDS(ON)}} \tag{10}$$

$$D = \frac{40V + 0.4V - 8V}{40V + 0.4V - 0.046V} = 0.803 \tag{11}$$

There is not much difference between the approaches 1 and 2. For worst case considerations it may be meaningful to evaluate the exact duty cycle.

2.4 Calculation of boost inductor L_{BO} and current loop resistor R_{CS}

Note: The following description to calculate the appropriate boost inductor L_{BO} is based on the current loop stability and the integrated slope compensation of the TLD5095/98, and differs from the standard booster equations.

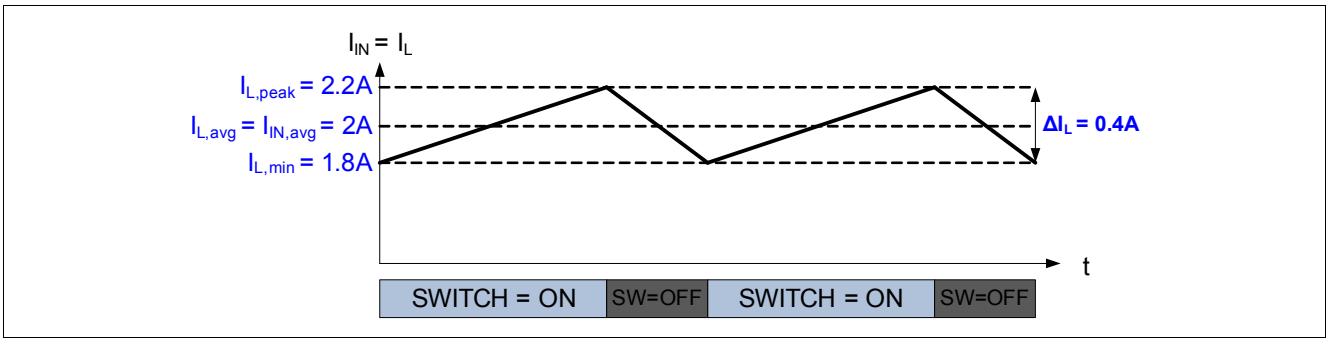


Figure 8 Inductor current

The average current $I_{L(AVG)}$ that flows trough the boost inductor L_{BO} is dependent on the output current I_{OUT} required and the worst case duty cycle $D_{(worst\ case)}$.

$$I_{L(AVG)} = \frac{I_{OUT}}{1 - D_{(worstcase)}} \tag{12}$$

$$I_{L(AVG)} = \frac{0.4A}{1 - 0.80} = 2A \tag{13}$$

Referring to the inductor current slope of a boost converter in CCM operation (shown in **Figure 5**) the minimum inductor current $I_{L(min)}$ and the peak inductor current $I_{L(Peak)}$ can be calculated from the current ripple ΔI_L specified.

$$\Delta I_L = I_{L(AVG)} \cdot \Delta I_{L\%} \tag{14}$$

$$\Delta I_L = 2A \cdot 0.20 = 0.4A \tag{15}$$

$$I_{L(peak)} = I_{L(AVG)} + \frac{\Delta I_L}{2} \tag{16}$$

$$I_{L(peak)} = 2A + \frac{0.4A}{2} = 2.2A \tag{17}$$

$$I_{L(\min)} = I_{L(AVG)} - \frac{\Delta I_L}{2} \tag{18}$$

$$I_{L(\min)} = 2A - \frac{0.4A}{2} = 1.80A \tag{19}$$

The inductor peak current $I_{L(Peak)}$ calculated for the worst case, **Equation (17)**, indicates the maximum current flowing through the inductor LBO, the MOSFET SW and the current loop sense resistor R_{CS}. (See the application drawing in **Figure 39** for details.)

An important factor for the calculation of the boost inductor L_{BO} in **Equation (22)** is the value of the sensing resistor R_{CS}.

2.4.1 Calculation of the current sensing resistor - R_{CS}

The R_{CS} resistor has two functions:

- 1) Over-current protection: R_{CS} is needed to limit the current through the external MOSFET switch SW and the inductor L_{BO}.
- 2) Building up a current control loop for the boost regulator: R_{CS} is needed to measure the current through the switch.

The switch peak over-current threshold (V_{SWCS}) in the datasheet is required to determine the proper value for R_{CS}: The relationship is described in **Equation (20)** below.

$$R_{CS} = \frac{V_{SWCS}}{I_{limit}} \tag{20}$$

The limiting current I_{limit} should be chosen according to the highest peak current $I_{L(peak)}$ that can occur in the system + a reasonable margin of safety. Furthermore, I_{limit} should be higher than the max. peak inductor current $I_{L(peak)}$ and should be lower than the permissible current rating of the MOSFET SW selected and the boost inductor L_{BO}. Based on the maximum peak current calculated in **Equation (17)**, we must consider 2.2 A. The assumption for I_{limit} = 3 A.

$$R_{CS} = \frac{0.15V}{3A} = 0.05\Omega \tag{21}$$

2.4.2 Boost inductor L_{BO}

The equivalent circuit of an inductor consists of 3 components:

- DCR: DC resistance of a coil. The DCR value is used to calculate the power loss in the inductor.
- L: total inductance of a coil.
- C_W: winding capacitance (winding capacitance will be ignored in further considerations)

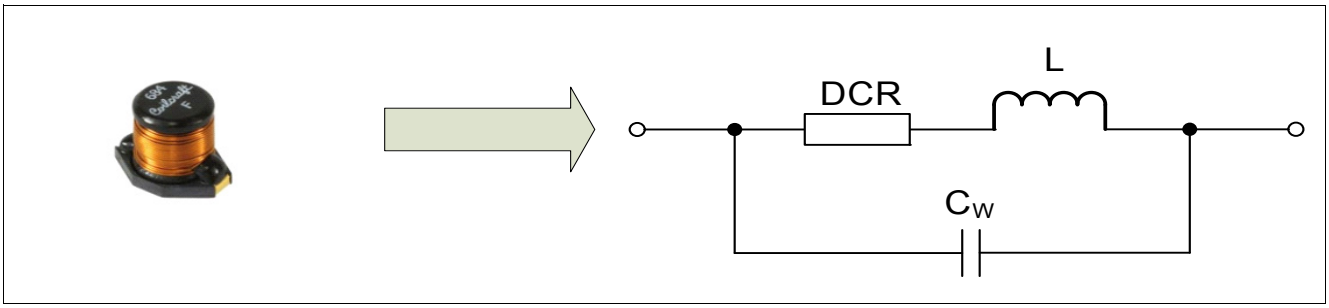


Figure 9 Example: Equivalent circuit of a real inductor

Knowing the proper R_{CS} resistance completes the device specific formula, which includes the integrated slope compensation consideration for control loop stability at duty cycles above 0.5. This formula considers V_{OUT}>>V_{IN}. The constant slope compensation is not dependent on the switching frequency f_{SW}.

$$L_{BO} \geq \frac{V_{OUT} \cdot R_{CS}}{106 \cdot 10^{-3} V \cdot f_{SW}} \quad (22)$$

$$L_{BO} \geq \frac{40V \cdot 0.05\Omega}{106 \cdot 10^{-3} V \cdot 400\,kHz} = 47.17\,\mu H \quad (23)$$

Component selected:

- Coilcraft MSS1278563MLD, L = 56 µH, DCR = 80.2 mW

2.4.3 Boost inductor L_{BO} if switching frequency f_{SW} is provided by the µC

If the synchronization feature is used, the following formular should be applied to determine the proper inductor value. The constant slope compensation is fixed for a specific switching frequency (f_{SW} = 250 kHz).

$$L_{SYNC} \geq \frac{V_{OUT} \cdot R_{CS}}{106 \cdot 10^{-3} V \cdot 250kHz} \quad (24)$$

$$L_{SYNC} \geq \frac{40V \cdot 0.05\Omega}{106 \cdot 10^{-3} V \cdot 250kHz} = 75.47\mu H \quad (25)$$

Note: $106*10^{-3}V$: equivalent slope compensation voltage

Tips for choosing the right inductor L_{BO}

- In fixed-frequency boost converters, the value of the inductor is based on the desired peak-to-peak ripple current ΔIL.
- Selection of the boost inductor is a trade-off between size and cost. Higher switching frequencies = lower inductance value = smaller component size = lower costs.
- Larger inductance means lower input ripple current.
- Ripple current between 20 % to 50 % of I_{LAVG} are reasonable values to make calculations for CCM
- Check the maximum DC peak current ratings and maximum operating frequencies for the inductor selected. (In general, always try to remain within the max. ratings.)

2.5 Calculation of the output capacitor - C_{OUT}

The simplified equivalent circuit of a capacitor is shown in **Figure 10** below. The resistive part of the capacitor is considered as equivalent to a series resistance ESR. The output capacitor is chosen such that it filters the switching ripple significantly. The parasitic resistance ESR, which is out of phase with its capacitance, causes additional voltage ripple. Ensure that capacitors are selected based on their maximum voltage, maximum ripple current and ESR ratings at the temperature and frequency of the application. The inductive portion L_C shall be ignored in further considerations.

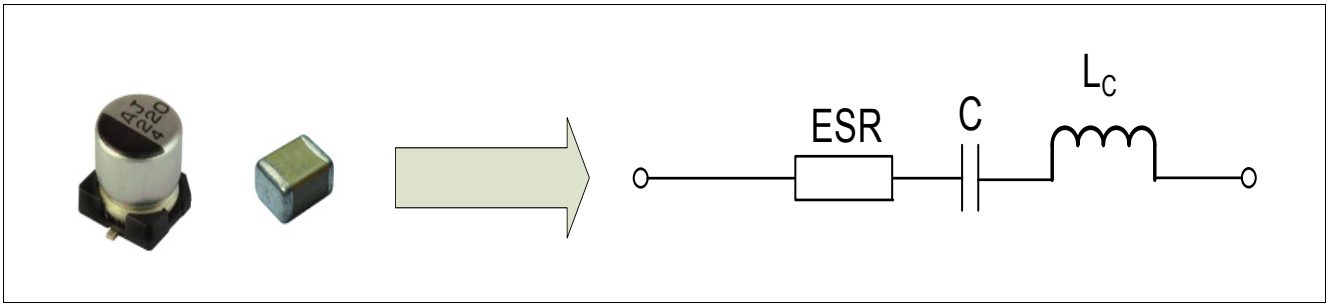


Figure 10 Simplified equivalent circuit of a real capacitor

The ESR value at the required switching frequency and the capacitance at the operating point (V_{OUT} = 40 V) can be obtained from the datasheets of capacitors. The capacitor elected has 2 µF @ V_{OUT} = 40 V although it is a device rated for 4.7 µF (**Figure 11**, diagram on the right hand side). Hence, the application requires 5 capacitors in parallel to achieve the required capacitance of >8µF.

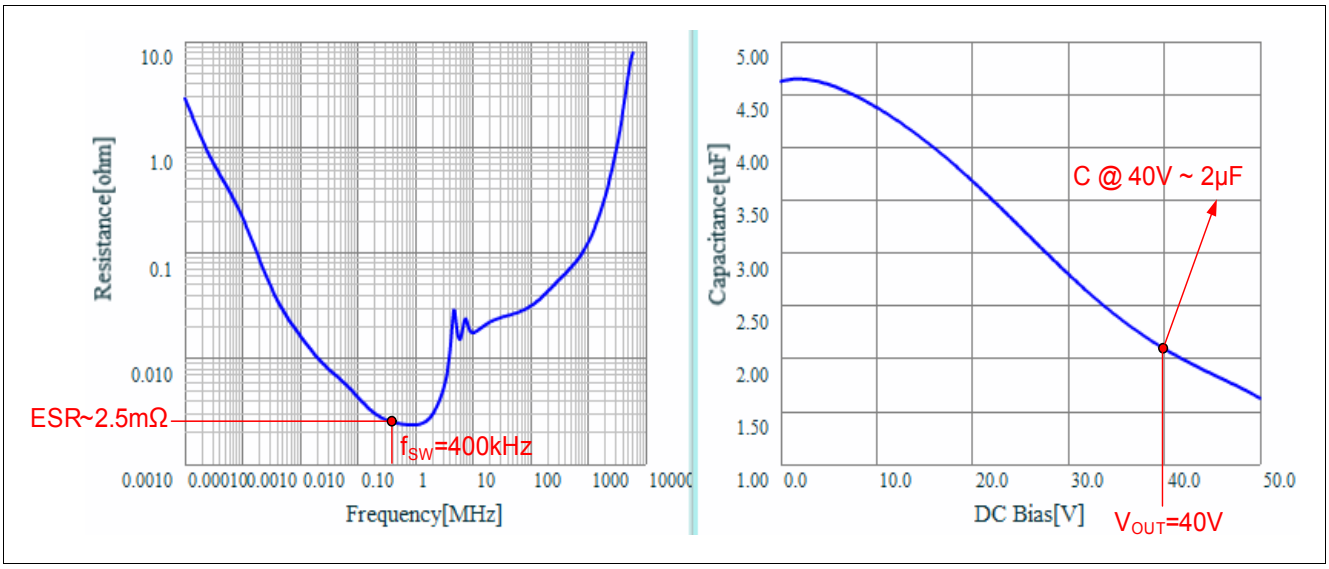


Figure 11 C_{OUT}: ESR and DC bias of a 4.7 µF/50 V/X7R ceramic capacitor (source Murata: GRM32EB31H475KA87) Automotive type: GCM32ER71H475KA55

When the switching MOSFET is ON the output capacitor C_{OUT} must supply the load. Therefore, the worst case duty cycle ($D_{(worstcase)}$) divided by the switching frequency (f_{SW}) is used in the formula to indicate the ON time (t_{ON} in **Equation (6)**). The ripple content due to the ESR of the capacitor is ignored in this formular.

$$C_{OUT} \geq \frac{I_{OUT} \cdot D_{(worstcase)}}{\Delta V_{OUT} \cdot f_{SW}} \tag{26}$$

$$C_{OUT} \geq \frac{0.4A \cdot 0.80}{100mV \cdot 400kHz} \geq 8\mu F \tag{27}$$

It is good to know the mean current which is flowing through the output capacitor for the calculation of the power consumption of the output capacitor.

$$I_{RMS\_COUT} = \sqrt{I_{OUT}^{2} \cdot \frac{D_{(worstcase)}}{1 - D_{(worstcase)}} + \frac{\Delta I_L^{2}}{12} \cdot \left(1 - D_{(worstcase)}\right)^2} \tag{28}$$

$$I_{RMS\_COUT} = \sqrt{0.4A^2 \cdot \frac{0.80}{1-0.80} + \frac{0.20^2}{12} \cdot (1-0.80)^2} = 0.800013A \tag{29}$$

A simplified formula can be used since the second term only has a small impact:

$$I_{RMS\_COUT} \approx I_{OUT} \cdot \sqrt{\frac{D_{(worstcase)}}{1 - D_{(worstcase)}}} \tag{30}$$

$$I_{RMS\_COUT} \approx 0.4A \cdot \sqrt{\frac{0.80}{1 - 0.80}} \approx 0.8A \tag{31}$$

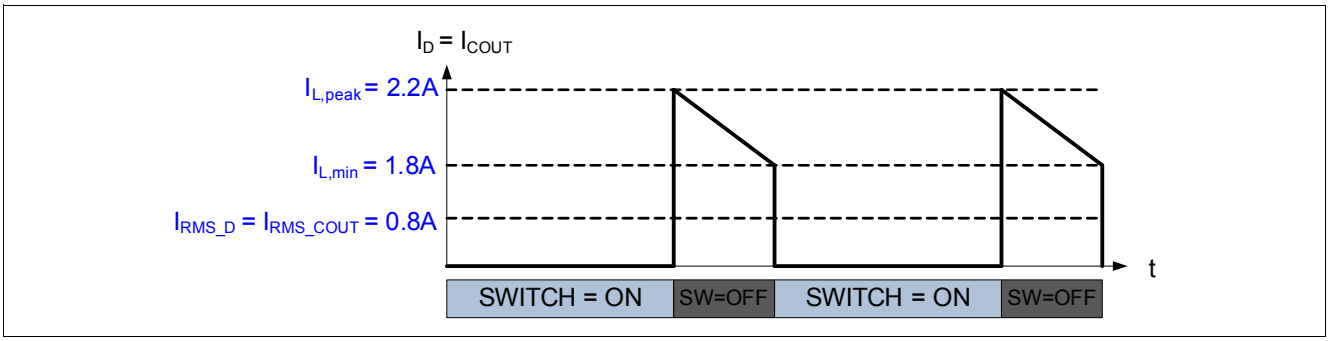


Figure 12 Diode current I_D flowing trough C_{OUT}

The maximum permissible voltage ripple on the output voltage should be known and specified by the application. In our example, the voltage output ripple should not exceed: ΔV_{OUT} = 100 mV.

Output voltage ripple and ESR value:

$$\Delta V_{OUT} = I_{L(peak)} \cdot ESR \tag{32}$$

The maximum permissible ESR value can be derived:

$$ESR \leq \frac{\Delta V_{OUT}}{I_{L(peak)}} \tag{33}$$

$$ESR \leq \frac{100mV}{2.2A} = 45.45m\Omega \tag{34}$$

Selection of the output capacitor:

- Voltage Rating > 40 V: **GCM32ER71H475KA55 = 50 V**
- I_{RMS} > 800 mA: **GCM32ER71H475KA55 > 1 A**
- ESR < 45.45 mOhm: **GCM32ER71H475KA55 = 5 times 2.5 mΩ in parallel = 2mΩ**

The output capacitor system design could consider:

1) An electrolytic capacitor. This solution is suitable if the capacitance value required is relatively high (e.g. > 22 µF) and higher DC voltage classes are called for. Despite the advantage of higher capacitance values available, the electrolytic capacitor has some disadvantages such as:

- Higher ESR values = more power losses (those with low ESR are more expensive and, in any case, far less than ESR values for ceramic capacitors)
- Poor thermal conduction path (e.g. SMD versions have a plastic interface to the PCB)
- Less robust and less reliable
- Limited temperature range (those with high temperature ranges are more expensive)

If an electrolytic capacitor is used in a system, it is a good practice to place a small (e.g. 100 nF) capacitor in parallel to bring down the ESR and achieve an additional filtering effect.

2) To overcome the issues with electrolytic capacitors, you can also use a bank of several ceramic capacitors connected in parallel. For the example under consideration, 5 times 4.7 µF/50 V capacitors can be placed in parallel, to fulfill the requirements. As shown in **Figure 11**, the capacitance value at 40 V is only 2 µF although the nominal rating is 4.7 µF. To be on the safe side, it is recommended to use 5*2 µT = 10 µF. The major advantage is the very low ESR value of 2 mΩ.

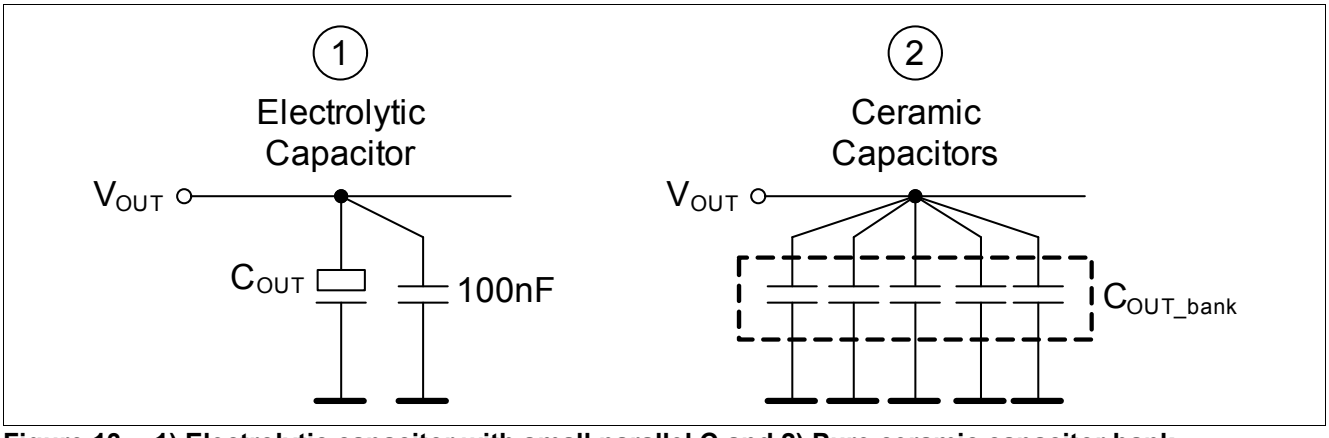


Figure 13 1) Electrolytic capacitor with small parallel C and 2) Pure ceramic capacitor bank

Tips:

- The output capacitance depends on the load and the converter configuration.
- In boost configurations, output capacitances are larger than in buck configurations to achieve the same load current ripple.
- Lower operating frequencies will require larger output capacitances.
- Output capacitors are selected based on their: capacitance; equivalent series resistance (ESR should be low); RMS or AC current rating and the DC bias voltage response.
- Note that a ceramic capacitor can have a very low capacitance value at the working voltage level! Hence, a reasonable margin of safety should be considered.
- X7R ceramic capacitances should be used: For automotive high-temperature applications, X8R ceramic capacitors are available.
- To improve the EMC, cost and thermal response, a parallel setup of ceramic capacitors is recommended. (Disadvantage: this is only possible in a reasonable µF range).

2.6 Calculation of the input capacitance C_{IN}

The value of the input capacitance C_{IN} of a boost converter is generally selected to limit the input voltage ripple ΔV_{IN} specified by the application. For continuous inductor current mode operation, the current flowing through C_{IN} is primarily determined by the inductor ripple current ΔI_L. The charge and discharge current of the capacitors is balanced, and thus, the root mean square (RMS) current flowing through the capacitor is zero.

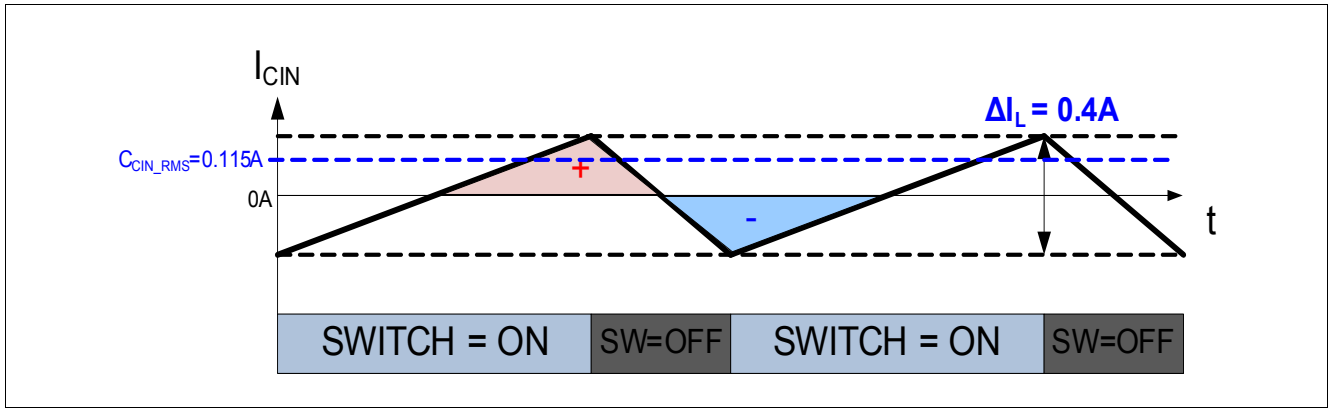


Figure 14 Current flowing through input capacitor C_{IN}

Note: For the worst case calculation, V_{IN} = 8 V has been considered. Hence, ΔL is at its maximum value.

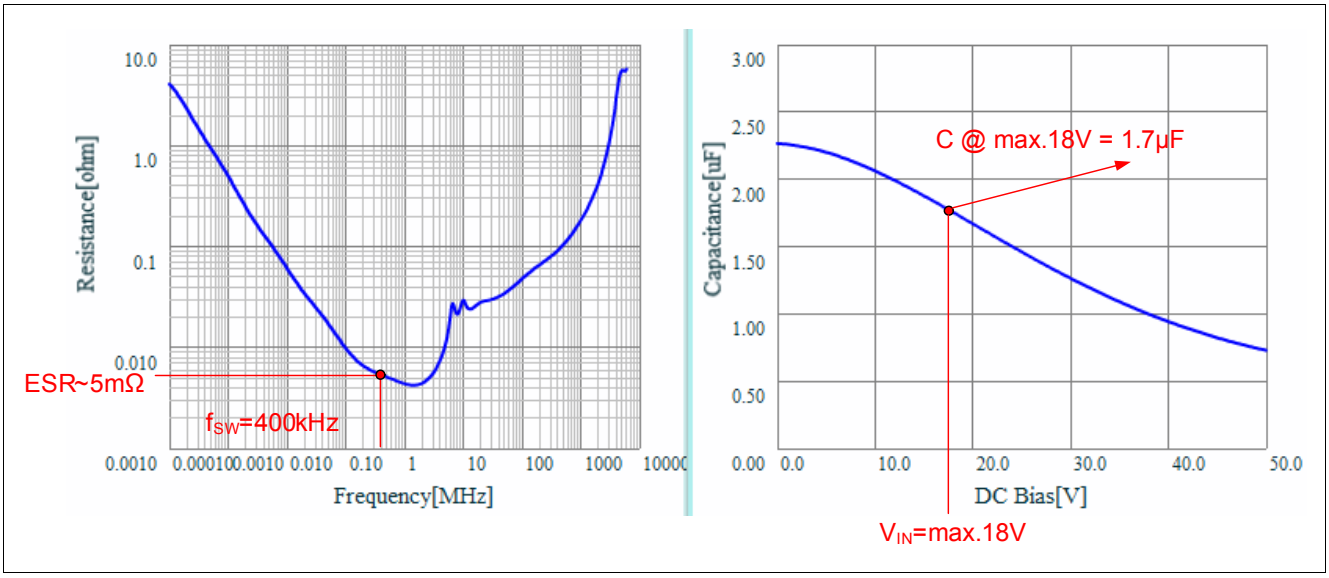


Figure 15 C_{IN}: ESR and DC bias of a 2.2 µF/50 V/X7R ceramic capacitor (source Murata: GRM31CR71H225KA88) Automotive type: GCM31CR71H225KA55

The input capacitor C_{IN} can be calculated as:

$$C_{IN} \geq \frac{\Delta I_L \cdot T_{SW}}{8 \cdot \Delta V_{IN}} \tag{35}$$

$$C_{IN} \geq \frac{0.4A \cdot 2.5\mu s}{8 \cdot 100mV} = 1.25\mu F \tag{36}$$

RMS current through C_{IN}:

$$I_{RMS\_CIN} = \frac{\Delta I_L}{\sqrt{12}} \tag{37}$$

$$I_{RMS\_CIN} = \frac{0.4A}{\sqrt{12}} = 0.115A \tag{38}$$

Input voltage ripple and ESR value:

$$\Delta V_{IN} = \Delta I_L \cdot ESR \tag{39}$$

The maximum permissible ESR value can be derived:

$$ESR \leq \frac{\Delta V_{IN}}{\Delta I_L} = \frac{100\,mV}{0.4\,A} = 25\,m\Omega \tag{40}$$

Selection of input capacitor C_{IN}:

- Voltage rating > 18 V: **GCM31CR71H225KA55 = 50 V**
- I_{RMS} > 115 mA: **GCM31CR71H225KA55 > 1 A**
- ESR < 25 mOhm: **GCM31CR71H225KA55 = 5 mΩ**

Tips:

- SEPIC and boost converters require a lower input capacitance than buck converters
- Refer to remarks in the output capacitance section

2.7 Switching MOSFET considerations

The major parasitic components are show in the MOSFET equivalent circuit on the right hand side in **Figure 16**. Furthermore, the corresponding MOSFET gate charging steps are shown on the left hand side.

Note: Parasitic MOSFET and freewheeling diode effects are not considered in this summary!

Explanation of the different gate charging steps:

- Before time t_0 the gate source voltage V_{GS} is zero and no current flows in the MOSFET.
- At time t_0 the gate-source voltage V_{GS} starts to increase.
- At time t_1, the gate-source voltage V_{GS} is equal to the threshold voltage $V_{GS(th)}$ and the current I_D begins to flow in the MOSFET, and until time t_2, all the current I_D flows in the MOSFET. (
- The input capacitance C_{gs} continues to charge during the time interval t_1 - t_2.
- After time t_2 the drain voltage V_{DS} begins to decrease while the drain current I_D is constant.
- The drain voltage decreases during the interval t_2 - t_3. At t_3 the drain voltage V_{DS} reaches the value R_{DSon} * I_D (where R_{DSon} is the power MOSFET ON resistance and the sum of R_d + R_s).
- Towards t_3 the gate source voltage V_{GS} can be increased furthermore to drive the ON resistance at an optimum value.

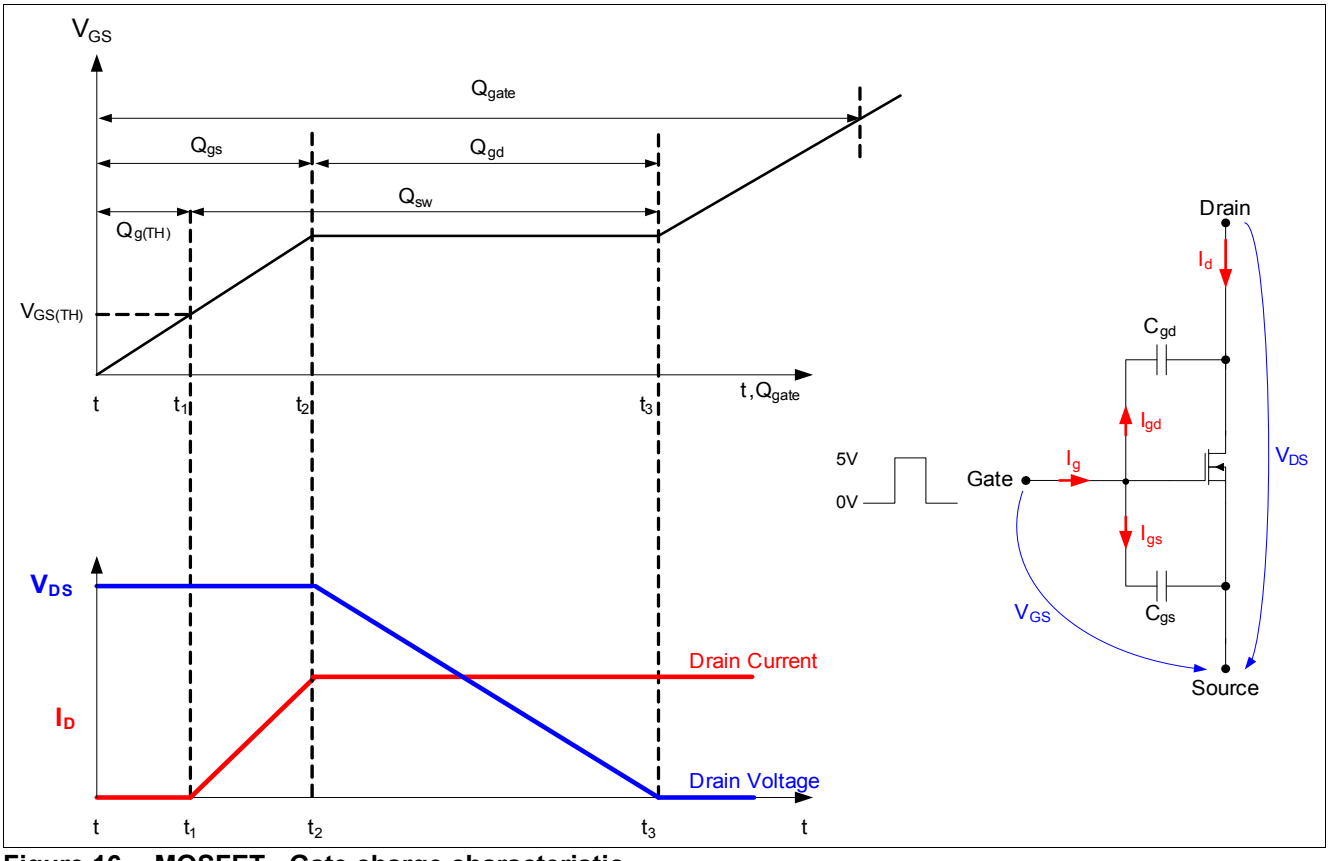


Figure 16 MOSFET - Gate charge characteristic

Switch ON timing calculation for a MOSFET:

$$t_{ON} = \frac{Q_{gate}}{I_{SWO,SRC}} \tag{41}$$

$$t_{ON} = \frac{6.5nC}{380mA} = 17.22ns \tag{42}$$

Switch OFF timing calculation for a MOSFET:

$$t_{OFF} = \frac{Q_{gate}}{I_{SWO,SNK}} \tag{43}$$

$$t_{OFF} = \frac{6.5nC}{550mA} = 11.82ns \tag{44}$$

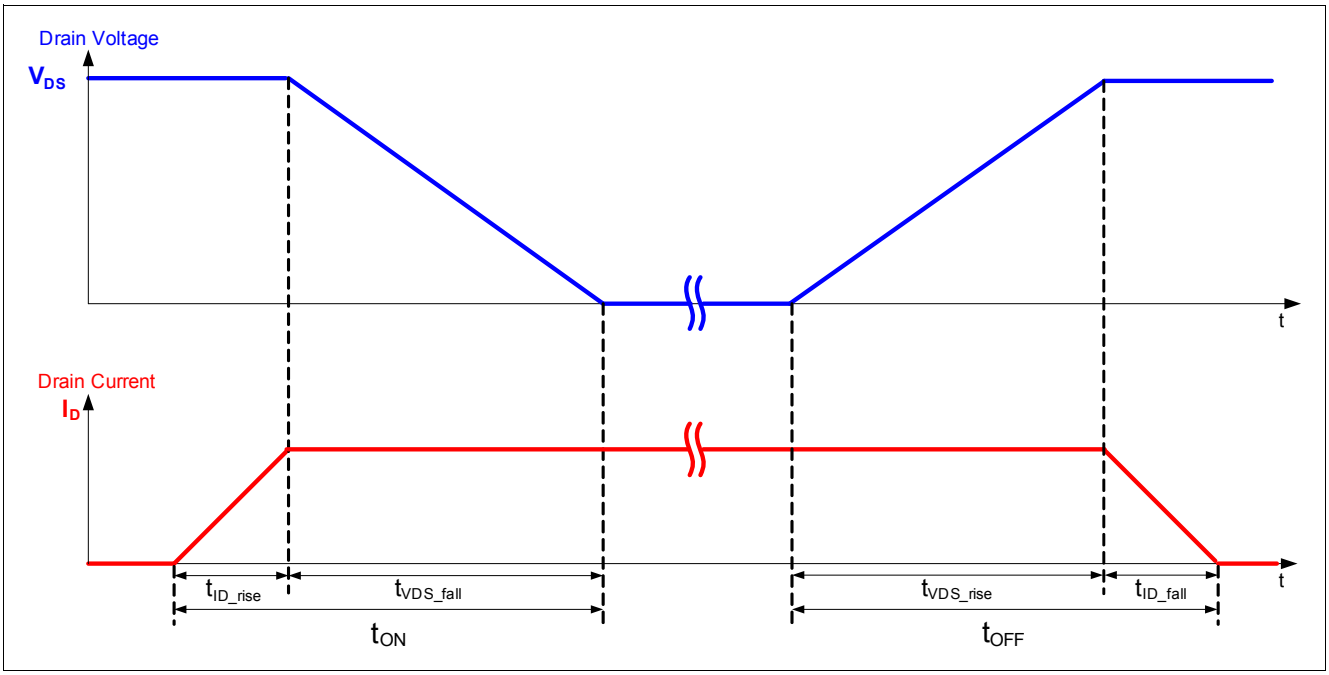


Figure 17 MOSFET - Switching time definition

Tips for selecting the power MOSFET:

For the application example under consideration, the Infineon OptiMOS®-T2 power transistor IPD25N06S4L-30 has been selected. Automotive applications require the use of AEC qualified robust MOSFETs with high operating temperature rating ($T_{j(max)}$ = 175°C). The crucial MOSFET parameters are shown in **Figure 18** below.

- n-channel MOSFETs are used for boost configurations (advantage of simple gate drive), a 5 V gate voltage compatible device should be selected (example: $V_{GS(th)}$ of 1.7 V).
- The MOSFET should have an appropriate $R_{DS(on)}$ to handle the input current flow even during worst case conditions and to reduce the conduction losses P_C.
- The MOSFET breakdown voltage $V_{(BR)DSS}$ should be greater than the maximum output voltage (example: V_{OUT} = 40 V < V_{DS} = 60 V).
- The MOSFET should have low value of gate input capacitances and gate charges since this will minimize the MOSFET's switching losses P_{SW} and power loss inside the TLD5095/98 P_{IC} (example: Q_G = 6.5 nC).
- Lead-free automotive qualified MOSFETs from Infineon are recommended: Please browse the portfolio on Infineon's website: **www.infineon.com/automotivemosfet**

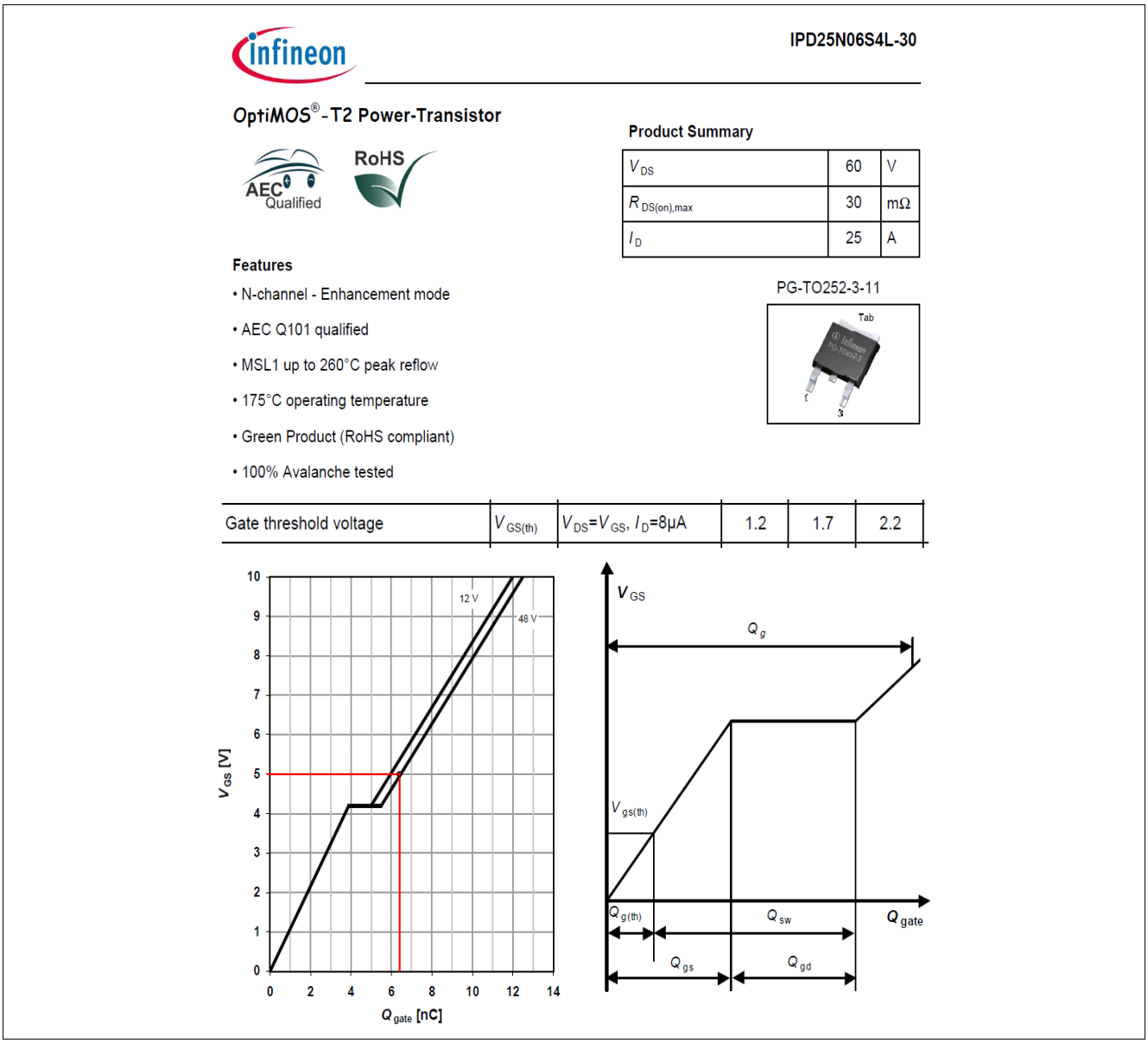


Figure 18 MOSFET datasheet abstract - IPD25N06S4L-30

2.8 Calculation of power resistor for LED current definition - R_{FB}

The typical reference voltage V_{REF} is 300 mV (specified parameter in product datasheet).

$$R_{FB} = \frac{V_{REF}}{I_{OUT}} \tag{45}$$

$$R_{FB} = \frac{0.3V}{0.4A} = 0.75\Omega \tag{46}$$

Tips:

- Isabellenhuette power shunt resistors of the SMS series having 1 % tolerance can be recommended

2.9 Calculation of over-voltage protection resistor divider - R_{OVL}, R_{OVH}

The maximum permissible voltage at the output ($V_{OUT(max)}$) should be slightly higher than the desired operating voltage V_{OUT}. To simplify the calculation, the lower value of the over-voltage resistor R_{OVL} is fixed at 1 kΩ. The internal over-voltage feedback threshold $V_{OVFB,TH}$ is specified in the product datasheet. The typical value is: $V_{OVFB,TH}$ = 1.25 V. The current flowing through the over-voltage protection resistor divider is:

$$I_{OV} = \frac{V_{OVFB,TH}}{R_{OVL}} \tag{47}$$

$$I_{OV} = \frac{1.25V}{1k\Omega} = 1.25mA \tag{48}$$

Now, you can calculate the upper over-voltage protection resistance. The rough assumption is to apply a little voltage overhead of 3 V for this estimation $V_{OUT(max)}$ = 43 V.

$$R_{OVH} = \frac{V_{OUT,\max}}{I_{OV}} \tag{49}$$

$$R_{OVH} = \frac{43V}{1.25mA} = 34.4k\Omega \tag{50}$$

The over-voltage resistor divider protects the application at:

$$V_{OUT\_OV} = 1.25V + 43V = 44.25V \tag{51}$$

The internal parameter $V_{OVFB,TH}$ has a spread of +/-3.2%. The external resistor divider should have a tolerance of 1 % (E96 series). This leads to a variation in the protected voltage V_{OUT_OV} of +/-4.2%. **Figure 19** below shows the variation of the protected output voltage. It is important that $V_{OUT} < V_{OUT\_OVmin}$ to ensure proper application according to the maximum output voltage desired.

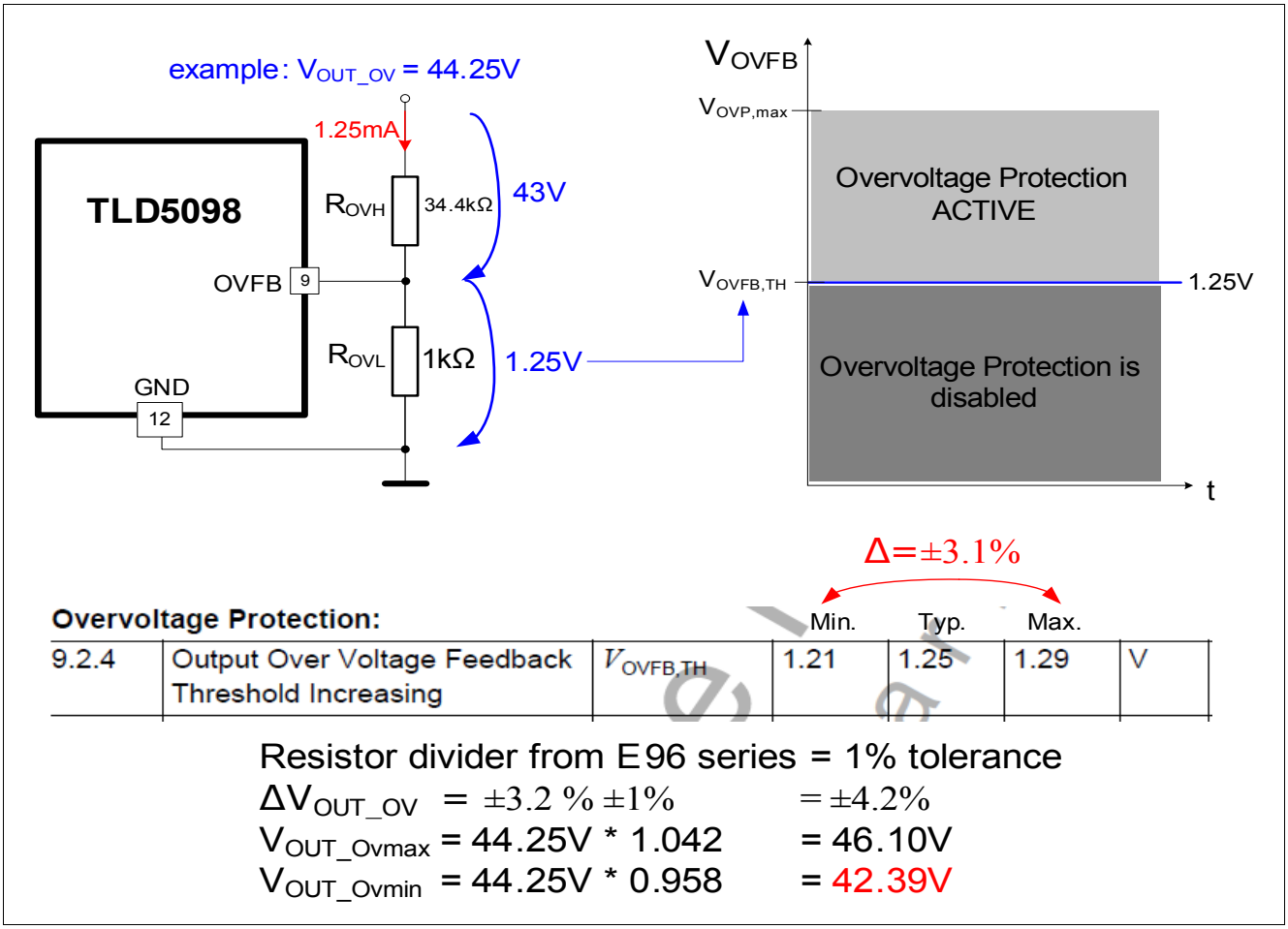


Figure 19 Description of over-voltage protection

Tips:

- E96 series (1%) resistors recommended

2.10 Output diode selection - D_{BO}

Diode selected for the example:

Schottky diode: 1 A / 50 V

Tips:

- The diode must handle the maximum DC output current = I_{OUT}
- The minimum reverse voltage should be higher than the max. V_{OUT} voltage
- Low leakage current at higher temperatures could be important
- Low forward voltage drop (use Schottky diodes)
- Diode should react fast (= fast switching)
- Package and thermal resistance considerations

2.11 Gate driver buffer capacitance selection - C_{IVCC}

The calculation of the gate buffer capacitance C_{IVCC} is based on the standard capacitance equation:

$$I = C \cdot \frac{dV}{dt} \tag{52}$$

The current in this formula is specified in the TLD5095/98 datasheet and represented by the gate driver peak sourcing current $I_{SWO,SRC}$ = 380 mA.

The value of dV is the voltage ripple on the regulator output voltage. Let's assume dV = 20 mV.

The value of dt is the switching ON time of the MOSFET, which is calculated in **"Switching MOSFET considerations" on page 22**. t_{ON} = 17.22 ns

The buffer capacitance required can be calculated:

$$C_{IVCC} = \frac{I_{SWO,SRC} \cdot t_{ON}}{dV} = \frac{380\,mA \cdot 17.22\,ns}{20\,mV} = 327\,nF \tag{53}$$

Selection of gate driver buffer capacitance C_{IVCC}:

C_{IVCC} = 1µF/6V

Tips:

- C_{IVCC} should have a low ESR
- X7R ceramic capacitors should be used: For automotive high-temperature applications, X8R ceramic capacitors are available.
- The parasitic inductance of the capacitor should be as low as possible. Otherwise, the parasitic inductor could lead to decreasing the gate switch ON time and result in higher switching power losses. The slope control of the MOSFET should be done with a defined external resistor (e.g. 10 Ohm), if necessary. A parasitic inductance also creates more ringing on the voltage signal and thus influences the delta voltage on the regulator output.

3 Stability considerations

The TLD5095/98 products feature an external compensation network (R_{COMP}, C_{COMP1}, C_{COMP2}), which can be adapted to a variety of application boundary conditions and ensure stable switching behavior. All the details for the dimensioning are explained in the following chapter.

3.1 LED resistance considerations

One crucial parameter for the stability calculation is the output impedance. A resistor value for the LED load must be defined. This is explained in the figure below.

$$R_{LED} = \frac{\Delta V_F}{\Delta I_F} = \frac{0.4V}{600mA} = 0.67\Omega \tag{54}$$

We assume LED forward drop voltage of 3.1 V to reach with 12 LEDs the VOUT = 12 * 3.1 = 40.72 V which is close to our example VOUT = 40 V.

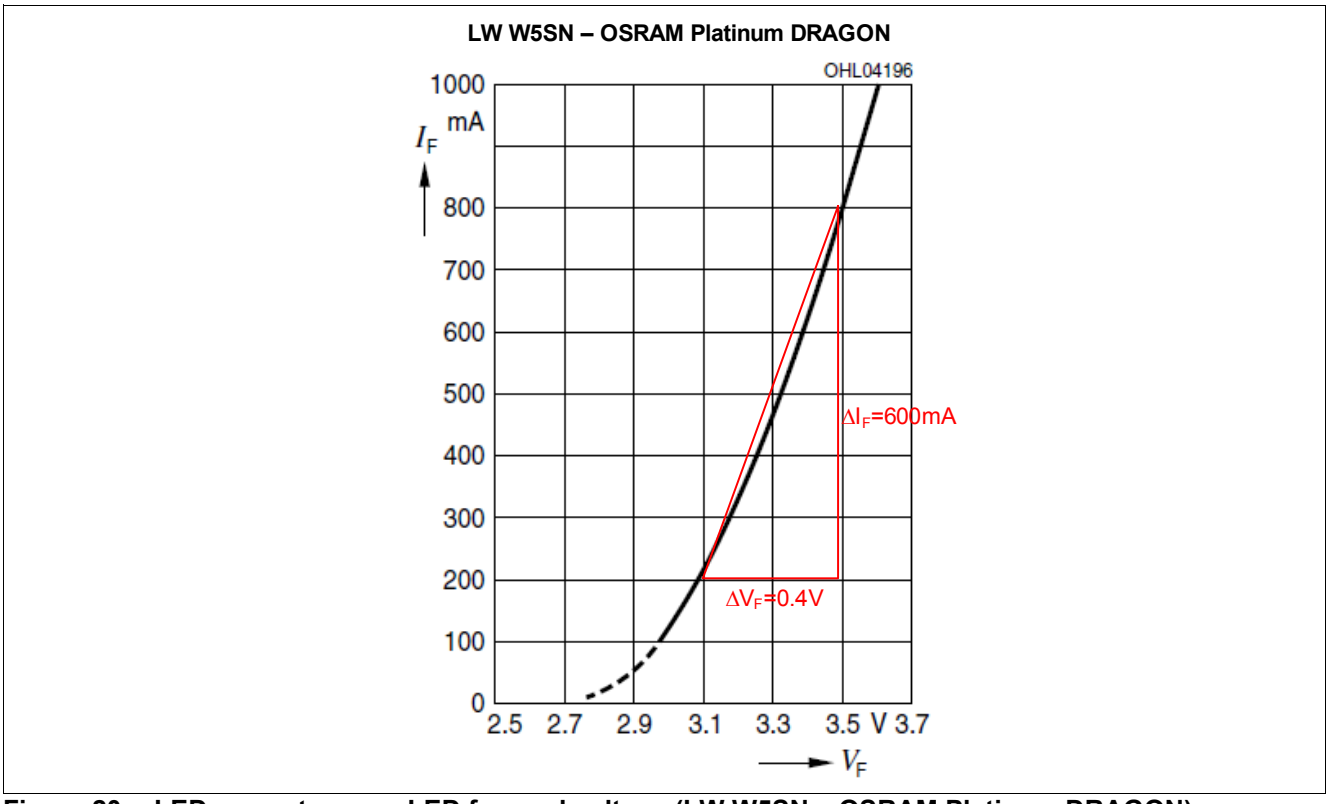


Figure 20 LED current versus LED forward voltage (LW W5SN – OSRAM Platinum DRAGON)

3.2 LED forward voltage considerations

Figure 21 below gives an indication of the LED forward voltage variation of a high-brightness LED. In general, the LED forward voltage V_F is dependent on the junction temperature T_j and the load current I_F.

At low temperatures, the LED forward voltage has its maximum value (e.g. 4.3 V). In many application specifications, where LEDs are connected in series, customers request the worst case forward voltage at low temperatures. This leads to relatively high output voltages and more expensive external components must be used as a consequence.

Theoretically, this may be correct but it should be always cross-checked if it is really necessary to map worst case on worst case conditions. In a real application, the LEDs will heat up very fast and the Tj = -40°C is not a continuous operating condition.

In our example, we select a continuous V_F of 3.368V for one single LED (typ. value @ Room Temperature). The sample application consists of 12 LEDs in series, which results in a V_{OUT} = 40.42V, which is very close to the output voltage initially assumed by us (V_{OUT} = 40 V).

Note: To be precise the contribution of V_{REF} (0.3V) must be considered as well, to get the proper output voltage:
$V_{OUT} = V_{LED} + V_{REF} = 40.42V + 0.3V = 40.72V$

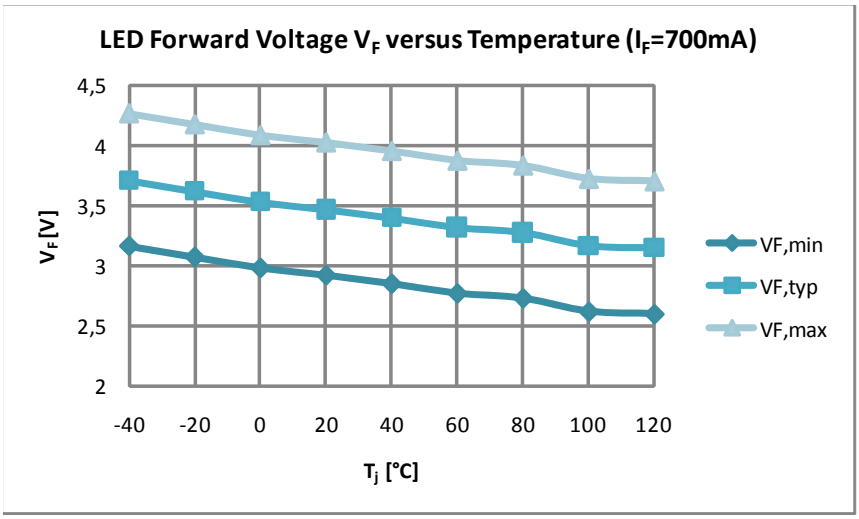


Figure 21 LED forward voltage V_F over temperature T_j (LW W5SN – OSRAM Platinum DRAGON)

3.3 Stability calculation

Figure 22 below shows the parameter input of a dedicated Excel calculation file. Especially for the stability calculation, it is more efficient to work with the tools provided to achieve faster results. Nevertheless, one sample calculation is shown to give a feel of the mathematical calculations used by the Excel tool. More information on the Excel tool is furnished in **"Excel tool for fast evaluation of external components, efficiency and stability" on page 42**.

One way of using the compensation sheet could be:

- Fill in the yellow parameters such as "application input values", "LED model characteristic values", "output RC network values" according to the values determined by the application dimensioning process.
- Try to fill in some initial estimated values for the "compensation network values". Use the values recommended in the TLD5095/98 product datasheet and view the stability results.
- If the phase margin parameter is below 60°, try to reduce the resistor value RCOMP and increase the value for C_{COMP1} and view the stability results once again.
- Repeat this procedure until you have the desired phase margin of > 60° and cross-check the result for the entire input voltage range.

Note: Sometimes it may be necessary to redefine the input values such as L_{BO}, R_{SWCS}, R_{ESR} to achieve optimized stability.

Parameter	Symbol	Value	Unit
Application Input Values			
Input Voltage DC/DC	VIN	**12**	V
Boost Inductor	LBO	**56,0**	µH
SET Voltage	VSET	**5**	V
Feedback Resistor	RFB	**0,750**	Ohm
Over Current Resistor	Rswcs	**0,05**	Ohm
Switching frequency	fsw	**400000**	Hz
LED Model Characteristic Values			
number of LED	n_LED	**12**	
LED threshold voltage	Vth_LED	**3,10**	V
single LED Resistor	R_LED	**0,67**	Ohm
Output RC network Values			
Capacitor	Cout	**10,00**	µF
Output Cap. Series Resistor	Resr	**0,01**	Ohm
Compensation network Values			
Resistor	Rcomp	**1000**	Ohm
Capacitor	Ccomp1	**47,00**	nF
Capacitor	Ccomp2	**0,00**	nF
Output Characteristic			
Feedback Reference Voltage	Vref	**0,30**	V
LED Current	ILED	**0,400**	A
LED Voltage	VLED	**40,42**	V
Output Voltage	Vout	**40,72**	V
Duty Cycle	D	**0,705**	
LED equivalent Resistor	RL	**8,04**	Ohm
Load Resistor	Rload	**8,79**	Ohm
DC Gain Values for small signal model			
Gain between VOUT and VFB	beta_DC	**0,09**	
Error Amplifier Gain	AEA_DC	**1500,00**	
Current Mode Gain	ACM_DC	**9,54**	
Stability results			
Open Loop DC Gain	DC_Gain	**61,73**	dB
Cut Frequency	fc	**1400**	Hz
Phase Margin	PM	**73,44**	deg

Figure 22 Inputs and numeric results of the Excel compensation sheet

3.4 Closed loop considerations

The TLD5095/98 control logic consists of two control loops. A current control loop, defined by the shunt resistor R_{CS}, and the voltage control loop, defined by the load current shunt resistor R_{FB}. Internal slope compensation ensures the loop stability at duty cycles above 50%. The external compensation network R_{COMP} and C_{COMP1} connected in series to ground, plus a parallel capacitor C_{COMP2} is needed to achieve a stable application for the application boundary condition specified.

The main contributors for the closed loop stability are displayed in **Figure 23** below. These are primarily the boost inductor L_{BO}, the output capacitor C_{OUT} and its ESR value, the feedback resistor R_{FB}, and the output network R_{LED} and V_{LED} have an significant impact on the stability. The freewheeling diode parameters V_d and R_d may be ignored.

*Note: The A_{CM} **Equation (56)** describes more than just the current loop amplifier. Current loop, slope compensation, logic and the booster network (consisting of: C_{OUT} and R_{LED}, L_{BO}) itself, are summarized as highlighted in the dotted area in **Figure 23**.*

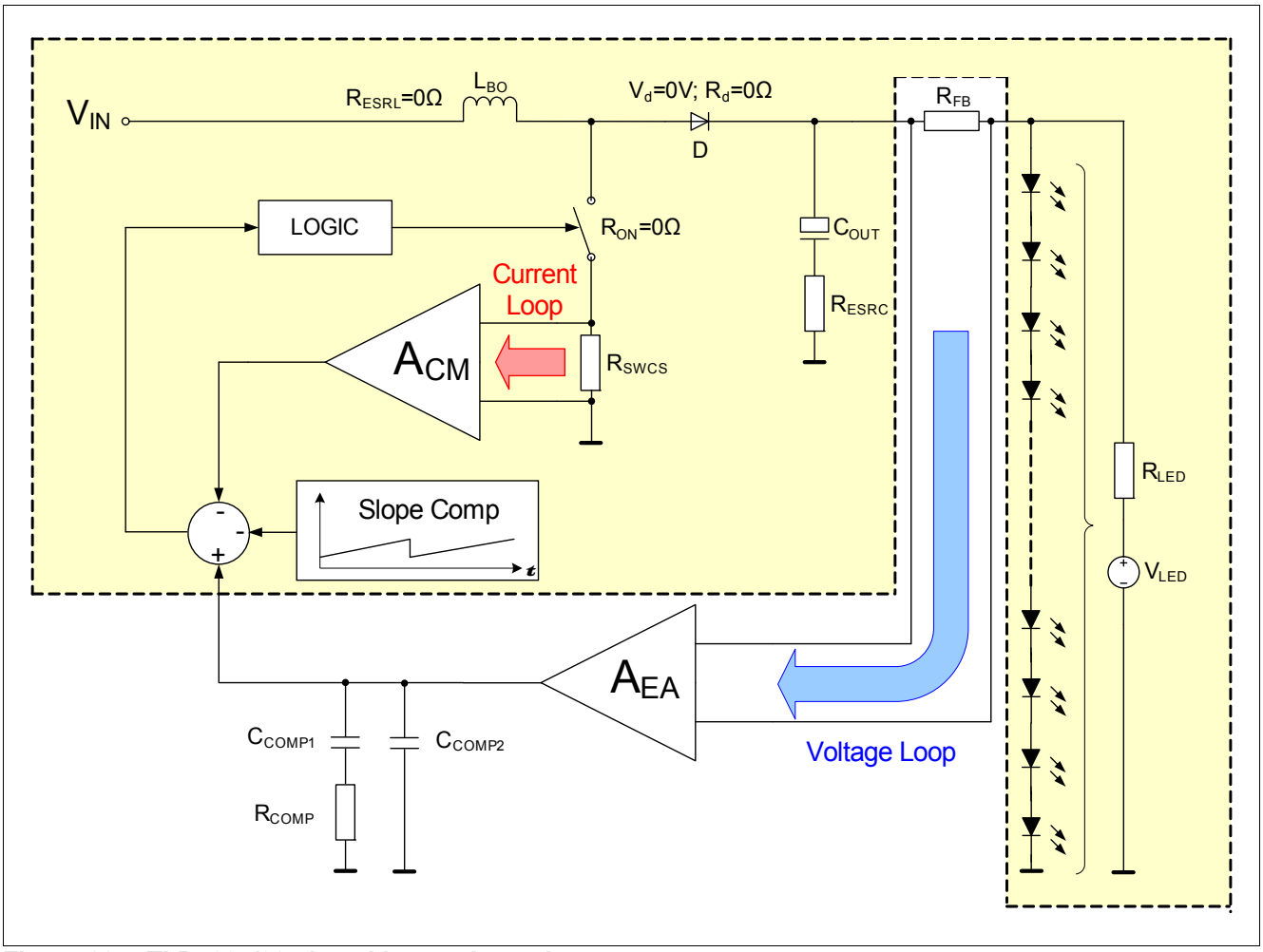


Figure 23 TLD5095/98 closed loop schematic

3.4.1 Definition of the open loop gain

The poles of the open loop gain need to be obtained for the stability of a control system. The pole and zero map is often used to assess the stability of a control system. In general, it can be said that a system is stable if all the poles are located on the left hand side of the imaginary axis. Refer to **Figure 24** to see more details.

Note: Zeros are not influencing the stability of a system!

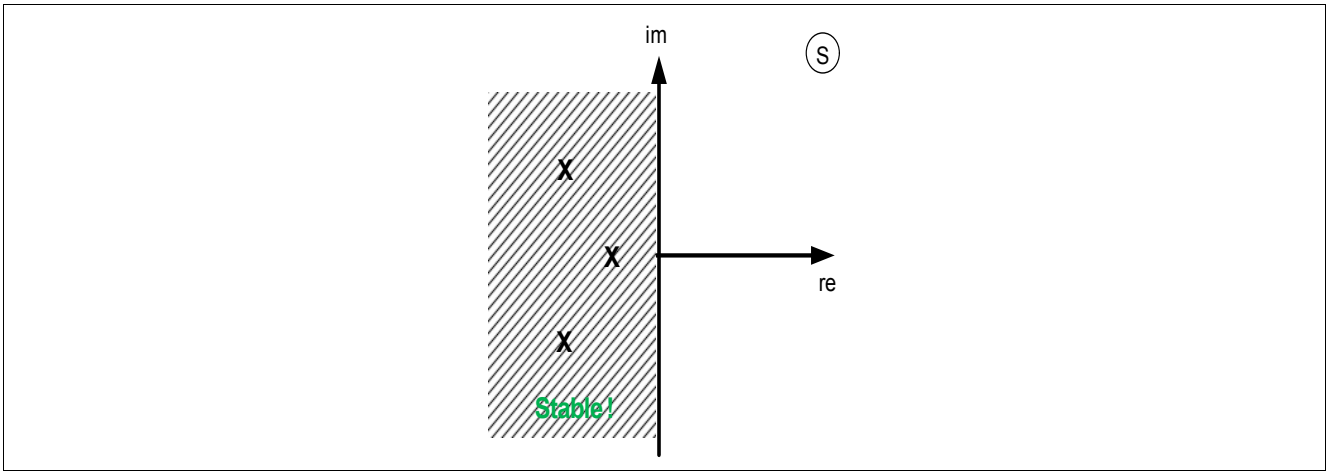


Figure 24 General overview of a pole and zero map

$$T \cong A_{CM} \cdot A_{EA} \cdot \beta \tag{55}$$

T = Open loop gain

A_{CM} = Amplification of current measurement amplifier (Current loop)

A_{EA} = Amplification of error amplifier (Voltage loop)

β = Feedback network

The feedback network describes the relation between the feedback signal and the output signal.

$$A_{CM} \cong \frac{0.2 \cdot D' \cdot R_{load}}{\left(1 + \frac{V_{OUT} - n \cdot V_{th\_LED}}{V_{OUT}}\right) \cdot R_{swcs}} \cdot \frac{(1 - \tau_{z1} \cdot s) \cdot (1 + \tau_{z2} \cdot s)}{(1 + \tau_{p1} \cdot s) \cdot \left(1 + \frac{s}{\omega_n \cdot Q} + \frac{s^2}{\omega_n^2}\right)} \tag{56}$$

$$A_{EA} \cong 0.0006 \times R_{EA} \times \frac{(1 + \tau_{z3} \cdot s)}{(1 + \tau_{p2} \cdot s) \cdot (1 + \tau_{p3} \cdot s)} \tag{57}$$

0.0006 = gmEA "transconductance" of the error amplifier

$$\beta \cong \frac{R_{FB}}{R_{load}} \tag{58}$$

3.4.2 Definition of zeros and poles

The following formulas require some parameters that are defined here:

$$D = 1 - D' \tag{59}$$

$$D' = \frac{V_{in}}{V_{out}} \tag{60}$$

$$D' = \frac{V_{in}}{V_{out}} = \frac{12V}{40.72V} = 0.295 \tag{61}$$

$$R_{load} \cong R_{FB} + n \cdot R_{LED} \tag{62}$$

$$R_{load} \cong R_{FB} + n \cdot R_{LED} = 0.75\Omega + 12 \cdot 0.67\Omega = 8.79\Omega \tag{63}$$

D’ = inverted switching duty cycle

n = number of LEDs

R_{LED} = forward LED resistor

The system displayed in **Figure 3** includes three zeros which are defined as:

$$\tau_{z1} \cong \frac{L_{BO}}{R_{load} \cdot D'^2} \cdot \left(\frac{V_{OUT} - n \cdot V_{th\_LED}}{V_{OUT}} \right) = \frac{56\mu H}{8.79\Omega \cdot 0.295^2} \cdot \left(\frac{40.72V - 12 \cdot 3.1V}{40.72V} \right) = 6.33 \cdot 10^{-7} \frac{s}{rad} \tag{64}$$

$$\tau_{z2} \cong C_{out} \cdot R_{ESR\_Cout} = 10\mu F \cdot 0.01\Omega = 1 \cdot 10^{-7} \frac{s}{rad} \tag{65}$$

$$\tau_{z3} \cong C_{comp1} \cdot R_{comp} = 47nF \cdot 1k\Omega = 4.7 \cdot 10^{-5} \frac{s}{rad} \tag{66}$$

Corresponding to the three zeros, the system includes three poles as well:

$$\tau_{p1} \cong \frac{C_{out} \cdot (R_{load} + 2 \cdot R_{ESR\_Cout})}{\left(1 + \frac{V_{OUT} - n \cdot V_{th\_LED}}{V_{OUT}}\right)} = \frac{10\,\mu F \cdot (8.79\,\Omega + 2 \cdot 0.01\,\Omega)}{\left(1 + \frac{40.72\,V - 12 \cdot 3.1\,V}{40.72\,V}\right)} = 8.11 \cdot 10^{-5}\,\frac{s}{rad} \quad (67)$$

R_{EA} = internal resistor of error amplifier

$R_{EA} \cong$ 2.5 MΩ (for TLD5098)

$R_{EA} \cong$ 47 MΩ (for TLD5095)

$R_{EA} >> R_{COMP}$

Note: $C_{COMP1} >> C_{COMP2}$

$$\tau_{p2} \cong \left(C_{comp1} + C_{comp2}\right) \cdot R_{EA} = \left(47nF + 0nF\right) \cdot 2.5M\Omega = 1.18 \cdot 10^{-1}\,\frac{s}{rad} \quad (68)$$

$$\tau_{p3} \cong C_{comp2} \cdot R_{comp} = 0nF \cdot 1k\Omega = 0\,\frac{s}{rad} \quad (69)$$

3.4.3 Definition of the slope compensation parameters and quality factor Q

The slope compensation parameters (ω_n, Q, m_c, S_e, S_n) for the current loop model is based on R.B. Ridley.

[1] **Reference:** Ridley, R.B.; "A New Continuos Time Model for Current Mode Control"; IEEE Transaction on Power Electronics; Vol. 6; Issue 2; pp. 271-280; 1991.

Note: For the stability of the system it is necessary that the quality factor Q is positive!

$$S_e = \frac{50 \cdot 10^{-6} A}{T_{SW}} = \frac{50 \cdot 10^{-6} A}{2.5 \mu s} = 20 \frac{A}{s} \quad (70)$$

T_{SW} = switching period

S_e = internal slope compensation

$$S_n = 0.001 \cdot \frac{V_{IN}}{L_{BO}} \cdot R_{swcs} = 0.001 \cdot \frac{12V}{56 \mu H} \cdot 50 m\Omega = 10.71 \frac{A}{s} \quad (71)$$

S_n = Slope of the ON period of the switch

$$m_c = 1 + \frac{S_e}{S_n} = 1 + \frac{20 \frac{A}{s}}{10.71 \frac{A}{s}} = 2.87 \quad (72)$$

$$Q \cong \frac{1}{\pi \cdot (m_c \cdot D' - 0.5)} = \frac{1}{\pi \cdot (2.87 \cdot 0.295 - 0.5)} = 0.92 \quad (73)$$

Q = Quality factor of the overshoot

3.4.4 Open loop gain calculations

$$A_{CM}(0) \cong \frac{0.2 \cdot D' \cdot R_{load}}{\left(1 + \frac{V_{OUT} - n \cdot V_{th\_LED}}{V_{OUT}}\right) \cdot R_{swcs}} = \frac{0.2 \cdot 0.295 \cdot 8.79\Omega}{\left(1 + \frac{40.72V - 12 \cdot 3.1V}{40.72V}\right) \cdot 0.05\Omega} = 9.54 \quad (74)$$

$$A_{EA}(0) \cong 0.0006 \cdot R_{EA} = 0.0006 \cdot 2.5 M\Omega = 1500 \quad (75)$$

$$\beta \cong \frac{R_{FB}}{R_{load}} = \frac{0.75\Omega}{8.79\Omega} = 0.0853 \quad (76)$$

$$T(0) \cong A_{CM} \cdot A_{EA} \cdot \beta = 9.54 \cdot 1500 \cdot 0.0853 = 1220.64 \quad (77)$$

$$T(0) \,|\, dB = 20 \cdot \log(1220.64) = 61.73 dB \quad (78)$$

3.5 Calculation of the phase margin:

Good practice for a proper phase margin value is > 60°. If the phase margin is lower, the system has a faster response time and oscillations can occur (the f cross-over is also higher in that case). A more gentle switching response can be achieved by increasing the phase margin.

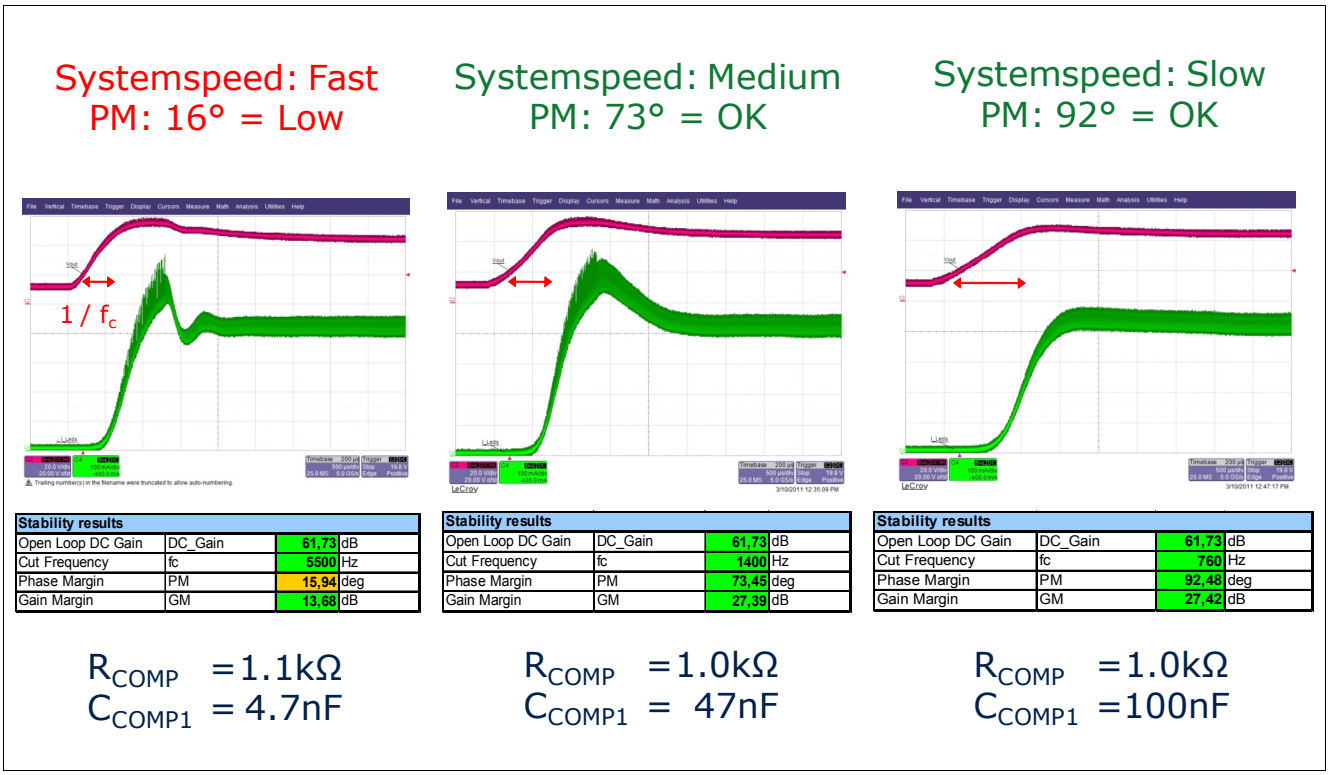


Figure 25 Response of fast and slow systems

This can be achieved by changing the compensation network values. A dedicated Excel file for the stability estimation is of great help to figure out the proper compensation network values R_{COMP}, C_{COMP1}, C_{COMP2}. The Excel sheet itself features a built-in function which indicates a green label for the phase margin if it is in the proper range for a stable application. In addition, a Bode plot is provided to see the phase and gain slopes directly as illustrated in **Figure 26** below. The crossover frequency f_{cross_over} is defined as the value when the gain slope intersects the 0 dB line. The phase margin PM of the system is obtained at the f_{cross_over} point.

$$f_{cross\_over} \cong \frac{T(0)}{2 \cdot \pi \cdot C_{comp1} \cdot R_{EA}} = \frac{1220.64}{2 \cdot \pi \cdot 47nF \cdot 2.5M\Omega} \cong 1653\,Hz \quad (79)$$

$$\omega_{c\_o} = 2 \cdot \pi \cdot f_{cross\_over} = 2 \cdot \pi \cdot 1653\,Hz = 10386\,\frac{rad}{s} \quad (80)$$

$$\phi_m = 180 - \tan^{-1}(\omega_{c0} \cdot \tau_{p1}) - \tan^{-1}(\omega_{c0} \cdot \tau_{p2}) - \tan^{-1}(\omega_{c0} \cdot \tau_{p3}) - \tan^{-1}(\omega_{c0} \cdot \tau_{z1}) + \tan^{-1}(\omega_{c0} \cdot \tau_{z2}) + \tan^{-1}(\omega_{c0} \cdot \tau_{z3}) \quad (81)$$

$$\phi_m = 180° - 40.1° - 89.95° - 0° - 3.76° + 0.06° + 26° = 72.25° \quad (82)$$

Note: The deviations between the calculated values and the results in the Excel sheet are attributable to differences on account of rounding up*!*

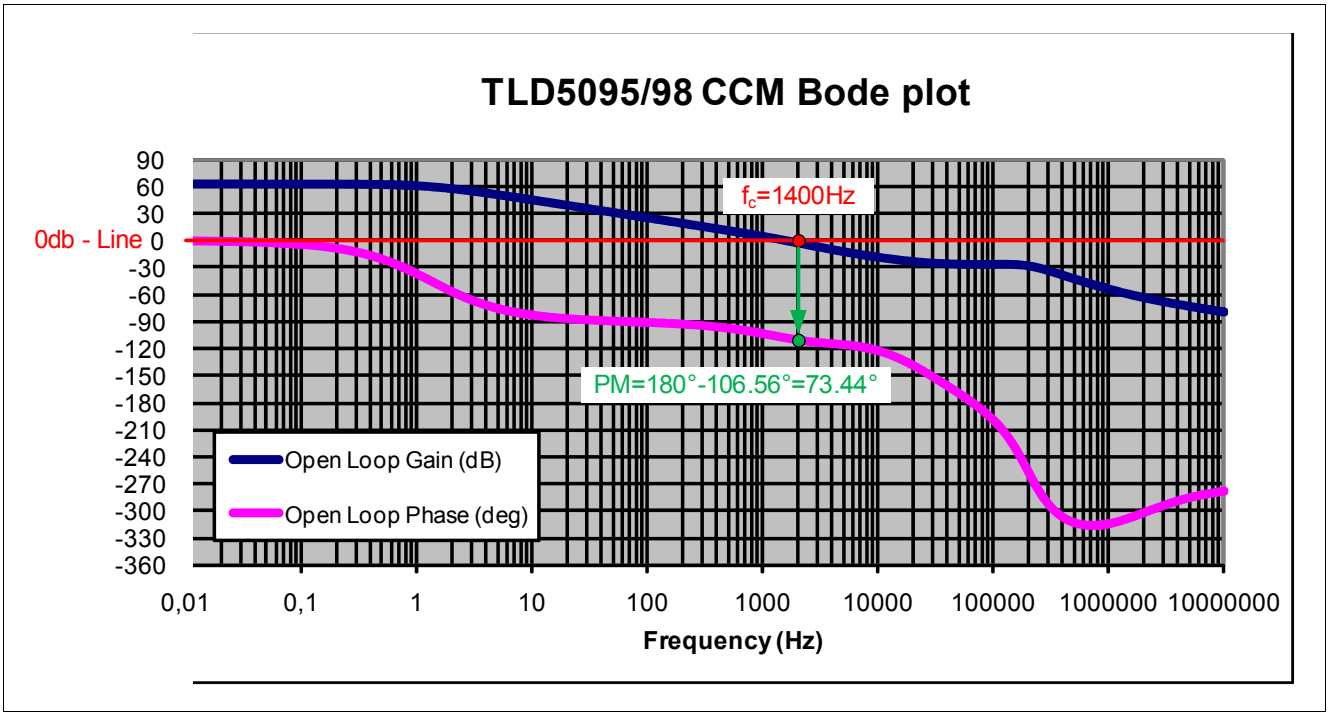
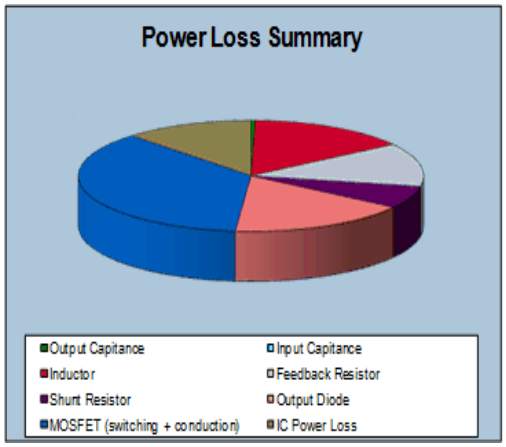


Figure 26 Bode plot

4 Power loss and system efficiency

After dimensioning and careful selection of the external components the overall power loss and system efficiency can be calculated. This chapter describes in detail how the power dissipation for each component can be obtained. The typical application input voltage V_{IN} = 12 V is considered for the calculations.



Power Loss Summary

Name	Value	Unit	Desciption
P_{COUT}	3,73	mW	Output Capitance
P_{CIN}	0,01	mW	Input Capitance
P_{L}	142,58	mW	Inductor
P_{RFB}	120,00	mW	Feedback Resistor
P_{RCS}	62,22	mW	Shunt Resistor
P_{Diode}	160,00	mW	Output Diode
P_{MOSFET}	345,85	mW	MOSFET (switching + conduction)
P_{IC}	115,20	mW	IC Power Loss
P_{out}	**16,00**	**W**	**Output Power**
Total	***949,595***	***mW***	***Sum of Losses***
η	***94,40%***	***%***	***Efficency of the system***

Figure 27 Power loss summary

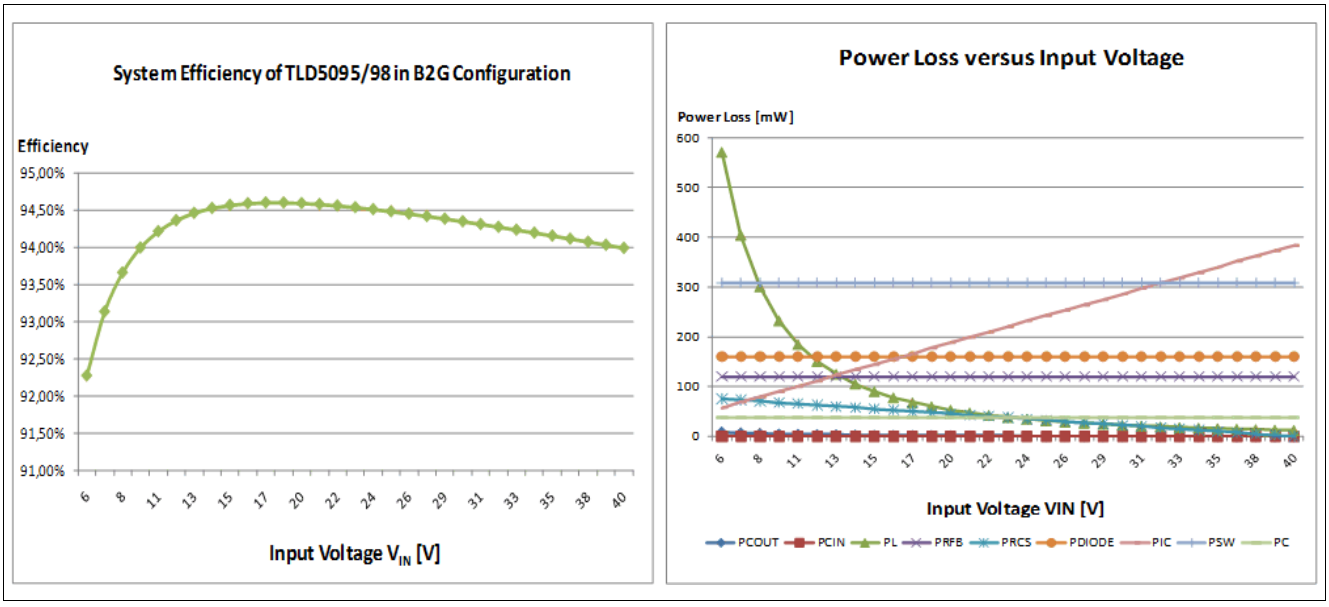


Figure 28 System efficiency and single power loss contribution slopes

4.1 TLD5095/98 IC Power Losses - P_{IC}

There are various power dissipating blocks integrated in the DC/DC controller IC.

1) Losses of the integrated voltage regulator - P_{LDO}:

It is necessary to calculate the average value of current required by the internal LDO.

$$I_{VCC\_RMS} = Q_g \cdot f_{SW} \tag{83}$$

$$I_{VCC\_RMS} = 6.5nC \cdot 400kHz = 2.6mA \tag{84}$$

$$P_{LDO} = (V_{IN} - V_{IVCC}) \cdot I_{VCC\_RMS} \tag{85}$$

$$P_{LDO} = (12V - 5V) \cdot 2.6mA = 18.2mW \tag{86}$$

2) Gate charge losses: P_{gate_charge}:

$$P_{gate\_charge} = V_{IVCC} \cdot I_{VCC\_RMS} \tag{87}$$

$$P_{gate\_charge} = 5V \cdot 2.6mA = 13mW \tag{88}$$

3) Quiescent current consumption losses - P_Q:

$$P_Q = V_{IN} \cdot I_{q\_on} \tag{89}$$

$$P_Q = 12V \cdot 7mA = 0.084W \tag{90}$$

Total IC losses:

$$P_{IC} = P_{LDO} + P_{gate\_charge} + P_Q = 115.2mW \tag{91}$$

4.2 Power MOSFET - P_{MOSFET}

The power MOSFET losses are split up between:

1) Conduction losses P_C:

$$P_C = D \cdot I_{IN}^{\ 2} \cdot R_{DS(on)} \tag{92}$$

$$P_C = 0.70 \cdot 1.33A^2 \cdot 30m\Omega = 37.33mW \tag{93}$$

2) Switching losses P_{SW}:

$$P_{SW} = 0.5 \cdot V_{OUT} \cdot I_{IN} \cdot (t_{ON} + t_{OFF}) \cdot f_{SW} \tag{94}$$

$$P_{SW} = 0.5 \cdot 40V \cdot 1.33A \cdot (39.5ns + 27.3ns) \cdot 400kHz = 308.52mW \tag{95}$$

The total MOSFET losses are:

$$P_{MOSFET} = P_C + P_{SW} = 37.33mW + 308.52mW = 345.85mW \tag{96}$$

4.3 LED current feedback resistor power loss - P_{RFB}

$$P_{RFB} = I_{OUT}^{\ 2} \cdot R_{FB} \tag{97}$$

$$P_{RFB} = 0.4A^2 \cdot 0.75\Omega = 0.12W \tag{98}$$

4.4 Switch current sensing resistor power loss - P_{RCS}

$$P_{RCS} = D \cdot I_{IN}^{\ 2} \cdot R_{CS} \tag{99}$$

$$P_{RCS} = 0.70 \cdot 1.33A^2 \cdot 0.05\Omega = 0.062W \tag{100}$$

4.5 Inductor power loss - P_{LBO}

$$P_{LBO} = I_{L,AVG}^{\ 2} \cdot DCR \tag{101}$$

$$P_{LBO} = 1.33A^2 \cdot 0.0802\Omega = 142.58mW \tag{102}$$

4.6 Input capacitor power loss - P_{CIN}

$$P_{CIN} = I_{RMS}^{\ 2} \cdot ESR \tag{103}$$

$$P_{CIN} = 0.115\ A^2 \cdot 0.005\ \Omega = 10\ \mu W \tag{104}$$

4.7 Output capacitor power loss - P_{COUT}

$$P_{COUT} = I_{RMS\_COUT}^{\ 2} \cdot ESR \tag{105}$$

$$P_{COUT} = 0.61 A^2 \cdot 0.01 \Omega = 3.73 mW \tag{106}$$

4.8 Freewheeling diode power loss - P_{DBO}

$$P_{diode} = I_{OUT} \cdot V_{FW} \tag{107}$$

$$P_{diode} = 0.4A \cdot 0.4V = 160mW \tag{108}$$

5 Design-in tools

Dimensioning and design efforts could become a very time-consuming task, particularly for switched mode power supply applications. To reduce the development cycle, design-in tools are well appreciated by customers, and Infineon provides several tools and guidelines to ensure streamlined design-in activity for the TLD5095/98 DC/DC controller ICs.

5.1 Excel tool for fast evaluation of external components, efficiency and stability

All the equations that have been summarized and described in this application note have been incorporated in a dedicated Excel sheet. This Excel tool supports the dimensioning, stability, and power loss and efficiency considerations very clearly. Last but not least, it is possible to export all results into a PDF document, which can be used as a design summary for permanent application documentation. The application note in combination with the Excel tool should provide a focused and fast approach for the proper design of a TLD5095/98 application.

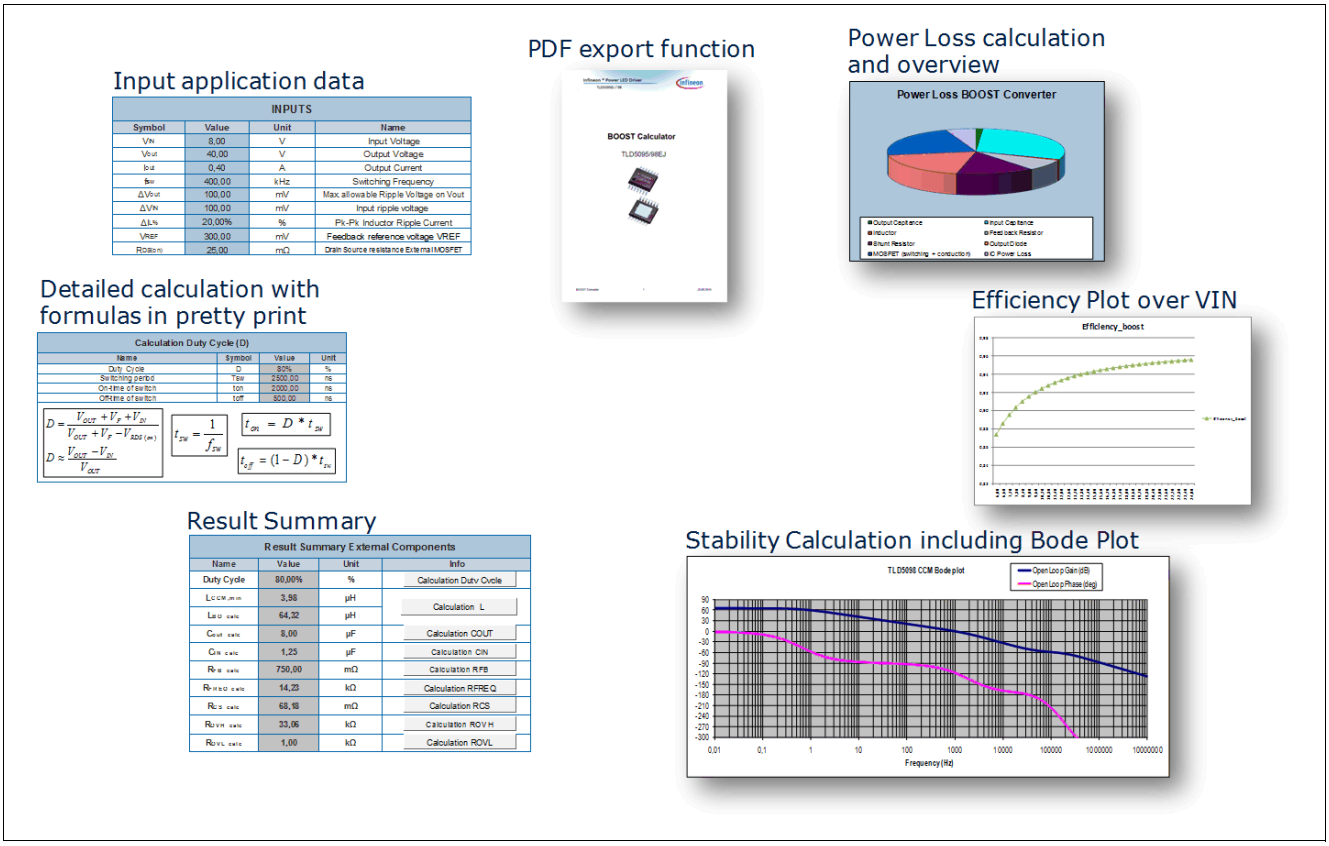


Figure 29 Excel sheet calculator for application dimensioning and stability

5.2 Electrical and thermal simulation

A PSPICE model could be very beneficial to get an initial impression of the system response. After the dimensioning process, a quick crosscheck of the application response could save costs by reducing hardware development cycles. Stability and switching response can be investigated easily with the help of the PSPICE models of the TLD5095/98 ICs provided. A complete test bench including discrete components, the DC/DC converter and the MOSFET can be provided on request. It is also worth mentioning that the comprehensive Infineon MOSFET portfolio also features dedicated PSPICE models that could be included in such a test bench.

Infineon website: **www.infineon.com/automotivemosfet**

In addition to electrical simulation, it becomes increasingly important to estimate the thermal performance of a system. It is recommended to run thermal simulations (e.g. Flotherm) or other appropriate tools to study the thermal response of a rough layout. The maximum ratings of the components used must not be exceeded!

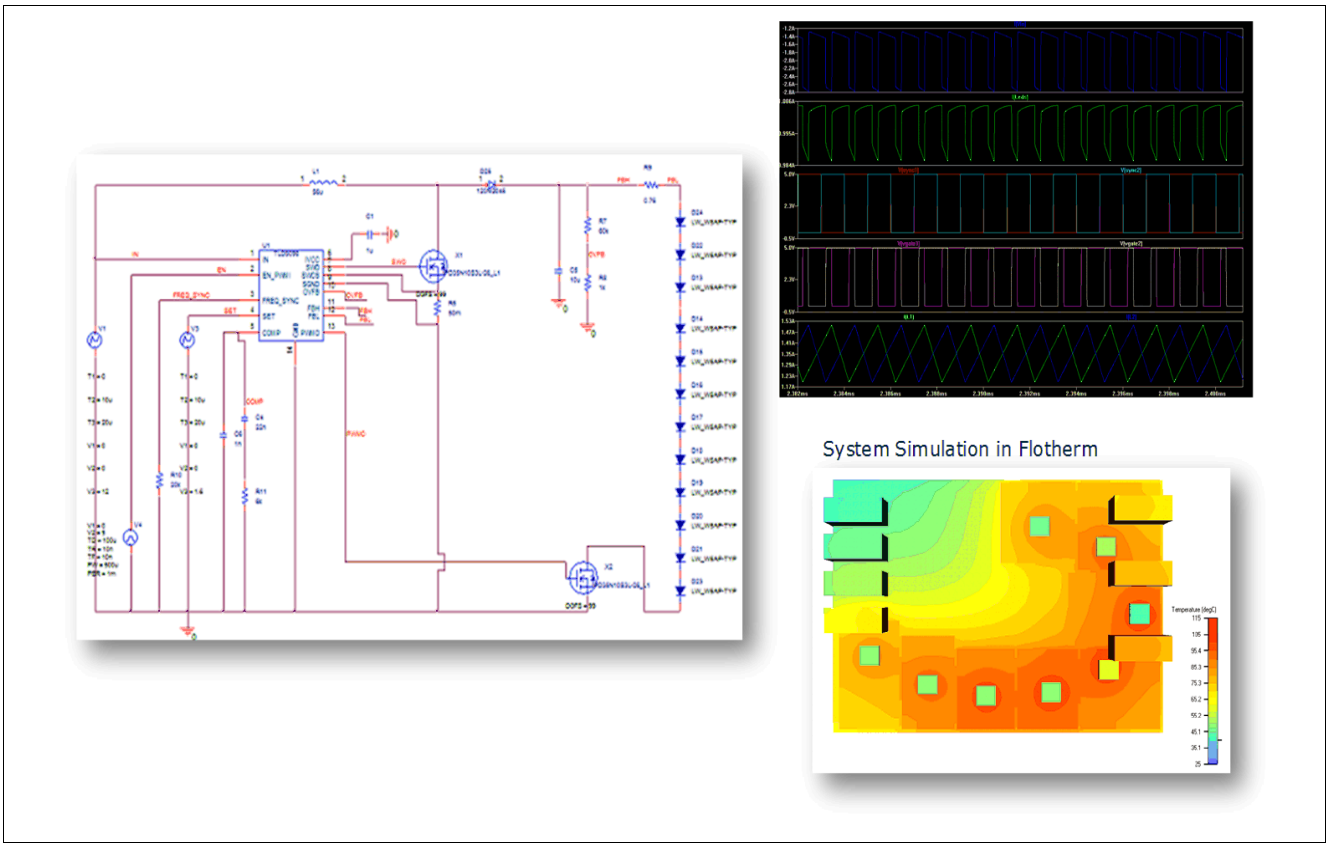


Figure 30 Simulation tools and support

5.3 Demo boards for fast evaluation in the lab & onboard LED chain

Another step in the evaluation of the TLD5095/98 products could be to conduct real measurements on a plug & play hardware such as the evaluation kit. The DC/DC layout has been reused from our EMC test PCB. All pins of the ICs can be easily connected with the help of banana cables to the measuring instruments, load and power supply equipment.

The evaluation kit features onboard LEDs (max. 8 LEDs in series, reconfigurable to only 1 LED in series for buck boost configurations). In addition, there is the feature of driving real loads via dedicated ports (4 mm banana sockets). You can switch between onboard LEDs and the external load using a simple switch on the demo board.

As illustrated in **Figure 31** below, the Evaluation Kit can be ordered for two different configurations.

1. One demo board features the standard boost to GND application and a SEPIC configuration can be realized with simple adaptation of the external circuitry. In addition, both, the B2G and the SEPIC can be driven in a constant voltage mode.
2. The second demo board features a boost to battery configuration, which is needed to achieve a BUCK-BOOST response and connect a single LED or several LEDs in a string. Constant voltage mode regulation is also possible for this configuration after simple modification of the external components on the demo board.

The TLD5095/98 demo boards enable quick evaluation of the products under real application conditions at the work bench level and can be ordered from our local sales team.

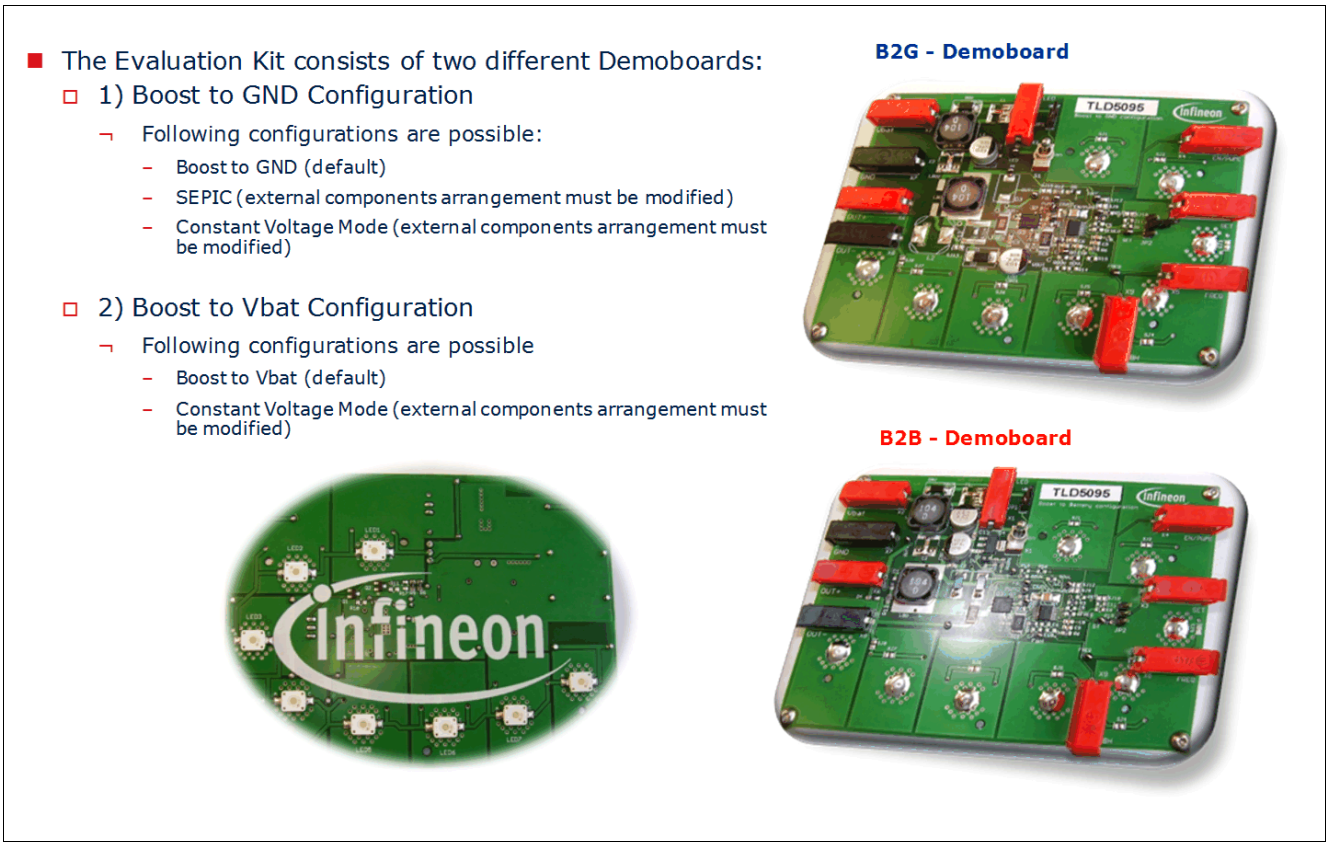


Figure 31 Plug & play demo boards for getting started in the laboratory

5.4 Sample layouts for small application boards

In addition to the evaluation kit for fast evaluation of the products, dedicated EMC and size-optimized application PCBs are available. These application boards are dedicated to one specific configuration such as the standard boost to GND or SEPIC configurations. The size of the application boards is 4.5 cm x 4 cm and the connections to the power supply and external load can be established with cables.

To simulate real load conditions, Infineon has also developed a general purpose LED board. The LED load board features up to 20 LEDs in series or can be configured in parallel connection as well to simulate multi-channel light sources.

The application boards in combination with real loads or the Infineon load board enable fast and realistic application prototyping and could be very beneficial for constructing initial system demonstrators. The layout of these boards is optimized for EMC and can be reused for customer applications.

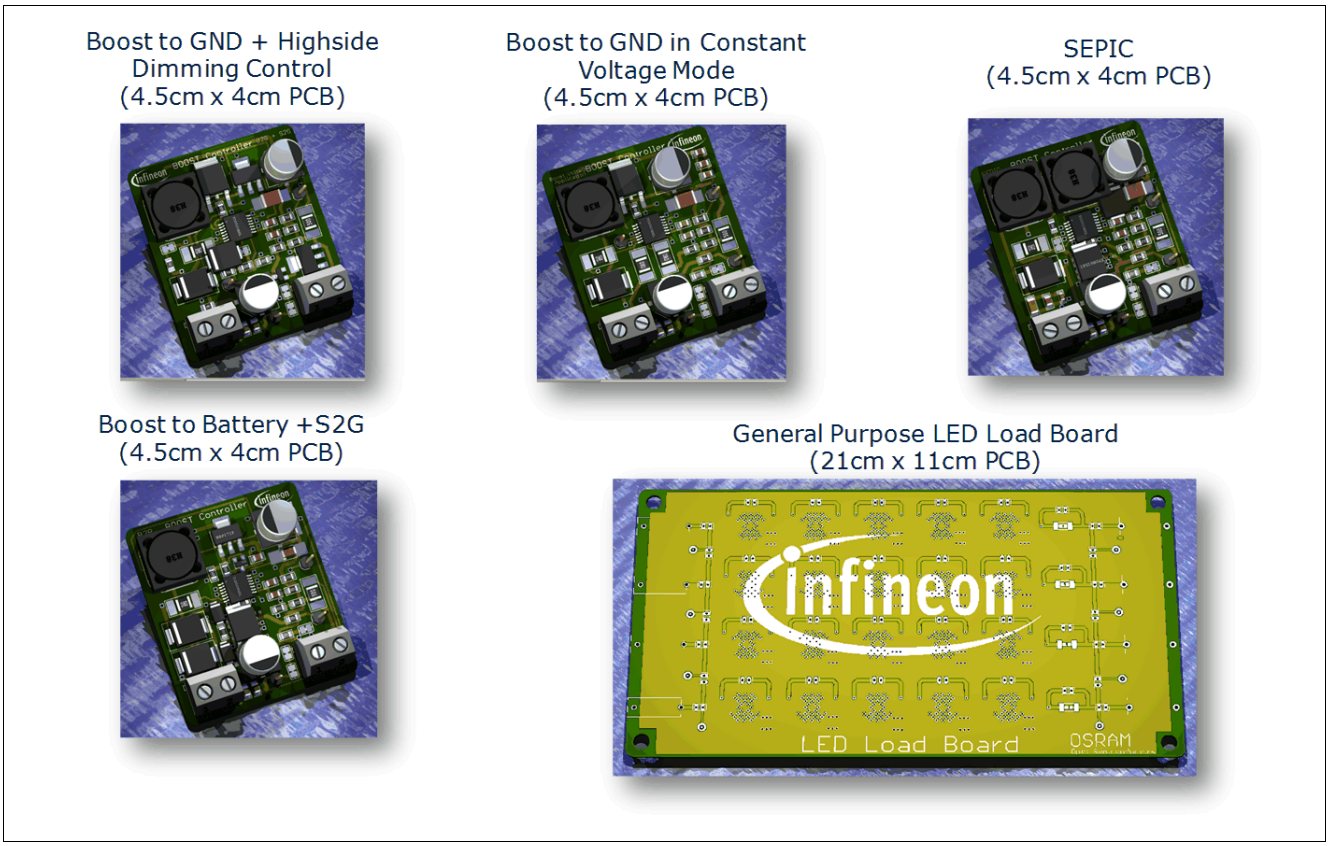


Figure 32 Small versatile application boards and EMC optimized layouts

5.5 EMC test reports and results summary

The EMC behavior of switched mode power supplies is considered as one of the most crucial topics during the design-in activities. All OEMs specify different limits which must be complied with by the application. The Infineon EMC investigation clearly takes care of the OEM and customer specifications and provides comprehensive reports.

The EMC reports consist of conducted and radiated emissions, immunity response, and ISO pulses.

In some cases, dedicated filter and countermeasures are described to improve the EMC behavior further as well as to provide guidelines to the reader for a proper EMC design.

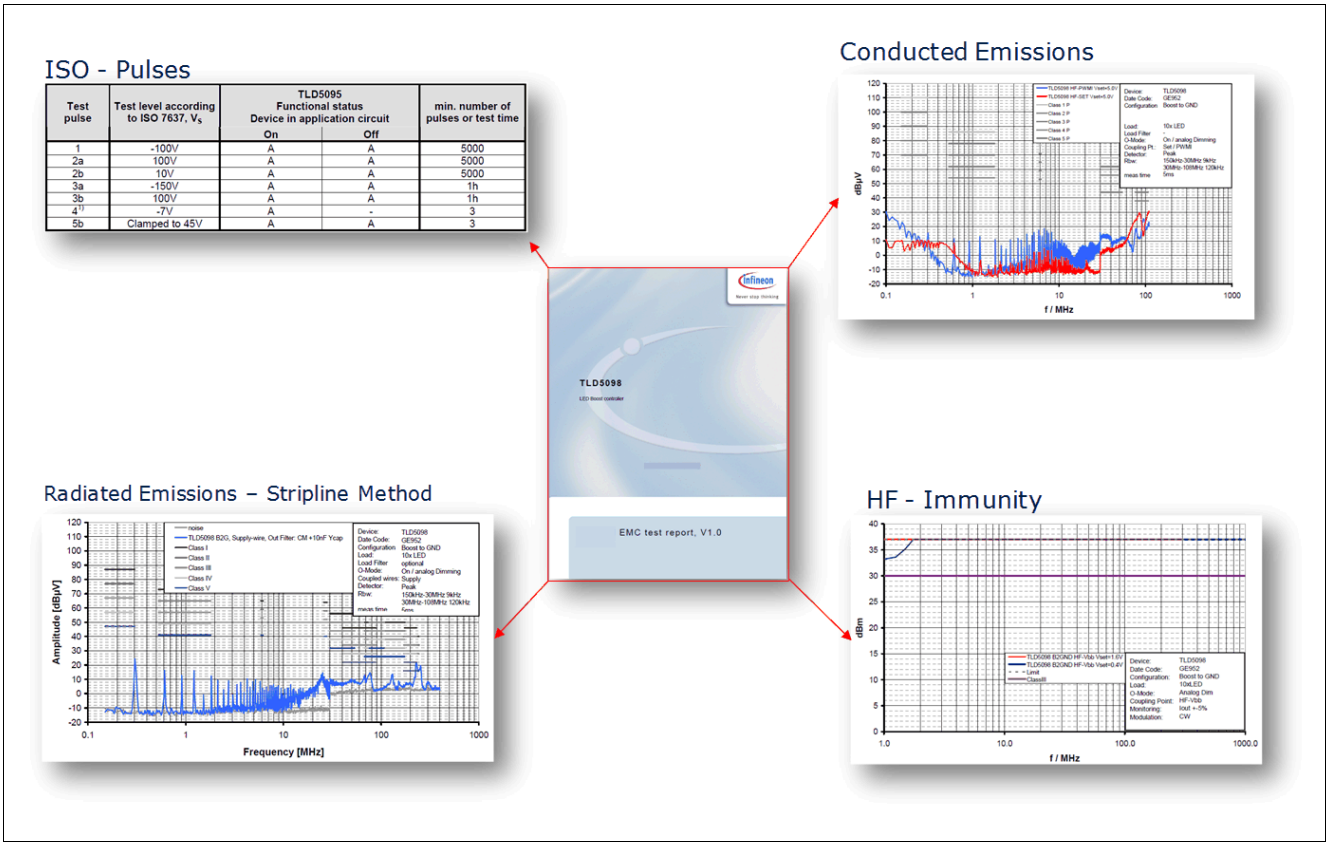


Figure 33 EMC test reports and results summary

- For further information, please contact **http://www.infineon.com/**

6 Revision history

Revision History: V1.3, 2011-08-08	
Previous version(s): 1.0, 1.1, 1.2	
Page	**Subjects (major changes since last revision)**
all	Editorial Changes

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