SIEMENS

# System Engineering Automotive

# Application Note

☑ : Additional file
TLE62x0GP.exe available

## Interfacing the Siemens Multiple Low-Side Switch Family TLE 62x0 GP to Siemens C500 and C16x Microcontrollers

This ApNote describes how to establish communication between Siemens 8 and 16 bit microcontrollers and the intelligent power IC family TLE 62x0 GP via the Serial Peripheral Interface (SPI).

Author: Hermann Kern / HL AI AE SE

File name: TLE62x0GP_01.pdf

**Contents** **Page**



| **ApNote - Revision History** | | |
|---|---|---|
| Actual Revision: 1.99 | Previous Revision: none (Original Version) | |
| Page of actual Rev. | Page of prev.Rel. | Subjects (changes since last release) |
| | | |

## 1 Introduction of the TLE 62x0 GP family

Siemens Semiconductors provides a family of smart multiple Low-Side Switches. The TLE 62x0 GP family addresses the demand for high system integration combined with enhanced diagnosis functionality. Members of this family are the quad (TLE 6220 GP) the octal (TLE 6230 GP) and the hex Low-Side Switch (TLE 6240 GP).
All derivatives of this family provide a Serial Peripheral Interface (SPI) which supports full duplex data transfer at baudrates up to 5 MBaud. Each output stage can be individually controlled and monitored via the SPI link. The status information of each channel (normal function, overload, short to ground and open load) can be obtained via the SPI lines. All these devices have a common communication protocol. Depending on the number of cannels the devices provide different SPI data length (8 or 16 bit see table below).
Additionally, dedicated channels can be directly controlled in parallel for PWM applications. Therefore, the TLE 62x0 GP is particulary suitable for engine management and powertrain applications as well as for body applications. For more information please refer to the data sheets of the TLE 62x0 GP. Table 1 below summarizes the features of TLE 62x0 GP family.

**Table 1 :**
**Multiple Low-Side Switch Family TLE 62x0 GP**

| | **TLE 6220 GP** | **TLE 6230 GP** | **TLE 6230 GP** |
|---|---|---|---|
| Channels | 4 | 8 | 16 |
| $R_{DSon}$ @ 25°C | 400 mOhm | 1 Ohm | 8 x 400 mOhm<br>8 x 1 Ohm |
| $I_{D(NOM)}$ | 3 A | 1 A | 8 x 0,5 A<br>8 x 0,3 A |
| SPI Datalength | 8 bit | 16 bit | 16 bit |
| SPI Baudrate | 5 MBaud | 5 MBaud | 5 MBaud |
| Package | P-DSO 20 | P-DSO 36 | P-DSO 36 |

Figure 1 shows a typical application. This example and all further given software routines are based on the TLE 6230 GP octal multiple Low-Side Switch.
In general, a microcontroller will be used to supervise these multiple Low-Side Switches. Control and diagnosis information are exchanged via the SPI bus. The $\overline{\text{Fault}}$ output of the power device shows low level, if there is an error condition at one of the output stages. Therefore the controller can use this signal as trigger for the diagnosis request. With this proceeding periodical diagnosis requests can be avoided without reducing system security.
Four of the eight output stages can be controlled in parallel and are connected to outputs with PWM capability of the microcontroller without the need of additional external dirver circuits.

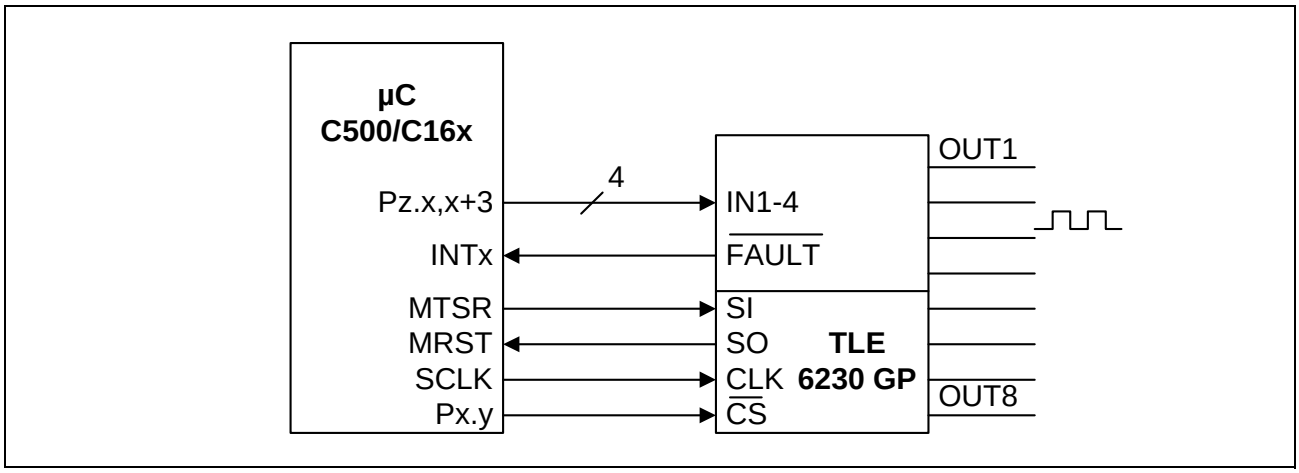


**Figure 1 :**
**Application Example**

The intelligent Octal Low-Side Switch TLE 6230 GP accepts 16 bit command words which control the eight output stages and it returns 16 bit diagnosis words which represent the actual status of the device.
Due to the integrated Serial Peripheral Interface more and more intelligence can be transferred to the power device. Therefore, complex instructions and diagnosis information can be exchanged via the SPI bus interface. Please refer to figure 2.

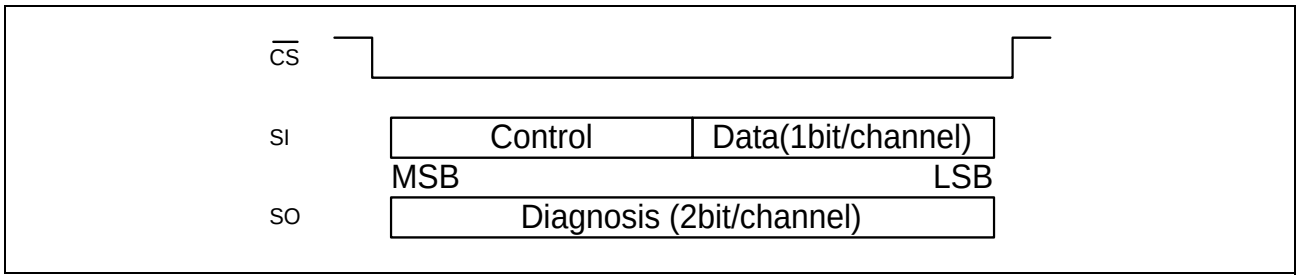


**Figure 2 :**
**SPI Protocol of the TLE 6230 GP**

.

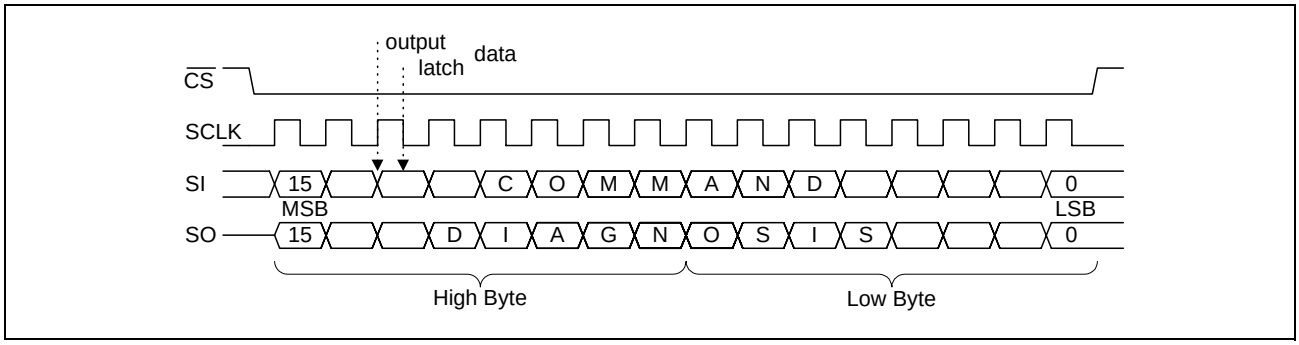


**Figure 3 :**
**SPI Timing Diagram**

Most derivatives of the Siemens C16x 16 bit microcontroller family and dedicated members of the Siemens C500 8 bit family are equipped with a SPI compatible SSC peripheral. The SSC (Synchronous Serial Channel) allows flexible high-speed communication with other microcontrollers, external memory devices, external peripherals or actuators like the TLE 62x0 GP family.
This application note describes how to control the TLE 6230 GP with 8 and 16 bit microcontrollers using the SSC peripheral. Furthermore a software emulation of the SPI interface for 8 bit microcontrollers will be introduced.
All given software examples are based on the octal Low-Side Switch TLE 6230 GP. With the basic understanding of the TLE 6230 GP, the introduced principles and the given software examples, it should be easy to establish communication between the quad or octal Low-Side Switch and 8 or 16 bit microcontroller.

## 2 How to control a TLE 6230 GP with a C500 microcontroller

The Siemens C500 8 bit microcontroller family offers a variety of different derivatives. The Serial Peripheral Interface of the TLE 6230 can be served either by the on-chip SSC peripheral, or if not available by a software emulation of the SPI. Both proceedings will be discussed in the following chapters.

As mentioned above the power device accepts 16 bit command words and returns 16 bit diagnosis information (Figure 2). Therefore, the 8 bit data format of the C500 microcontroller has to be adapted to the requirements of the power IC . This means, that the 16 bit data frames have to be treated as two eight bit portions.
During the SPI data transfer the power IC outputs data on the rising edge and latches data on the falling edge of the serial clock line. The transmission starts with the Most Significant Bit (MSB).
While the $\overline{CS}$ line is activated, the 8 bit microcontroller has to execute two consecutive 8 bit data transfers. The data transmission starts with the high byte of the 16 bit word and the low byte follows immediately afterwards. After the transmission of the high byte, the received data can be saved and the transmit buffer can be rewritten. The only condition that must be fulfilled during this consecutive byte transfer is that the $\overline{CS}$ line remains in low state which indicates that the transmission will go on.

The general timing of a complete 16 bit data transmission is shown in detail in figure 3 .

### 2.1 Using the on-chip Synchronous Serial Channel

The following members of the Siemens C500 8 bit mircrocontroller family are equipped with an on-chip SPI compatible interface: C513, C513A, C515C and C541. The C515C derivative is dedicated designed for automotive and industrial applications. All given software examples relating the SSC are based on this device.

The Serial Synchronous Channel (SSC) of the C515C has to be initialized according to the demands of the TLE 6230 which are listed below.

- MSB First
- Master Mode
- Idle Clock Low
- Latch Data on Falling Edge
- Output Data on Rising Edge
- Baudrate (the C515C achieves baudrates of up to 2.5 MBaud @ fosc = 10 MHz)

The corresponding initialization routine can be found in the attached software examples.

The consecutive data transfer of high and low byte of the 16 bit command/diagnosis word can be realized with a software routine like the one below.

```
data union
{
 unsigned int i;
 unsigned char c[2];
}spi_buffer;

#define spi_buffer_high  spi_buffer.c[0]
#define spi_buffer_low   spi_buffer.c[1]

void 16bit_transfer (void)
   {
    CS = 0;                  // activate chip select
    SCF &= 0xfe;             // clear transfer completed bit
    STB = spi_buffer_high;   // transmit high byte
    while(! (SCF & 0x01));   // wait until transfer completed
    spi_buffer_high = SRB;   // get high byte
    SCF &= 0xfe;             // clear transfer completed bit
    STB = spi_buffer_low;    // send/receive low byte
    while(! (SCF & 0x01));   // wait until transfer completed
    spi_buffer_low =SRB;     // get low byte
    CS = 1;                  // deactivate chip deselect
   }
```

**Figure 4 :**
**16 bit data transfer via 8 bit SSC interface**

The timing diagram of this routine is shown in Figure 5.

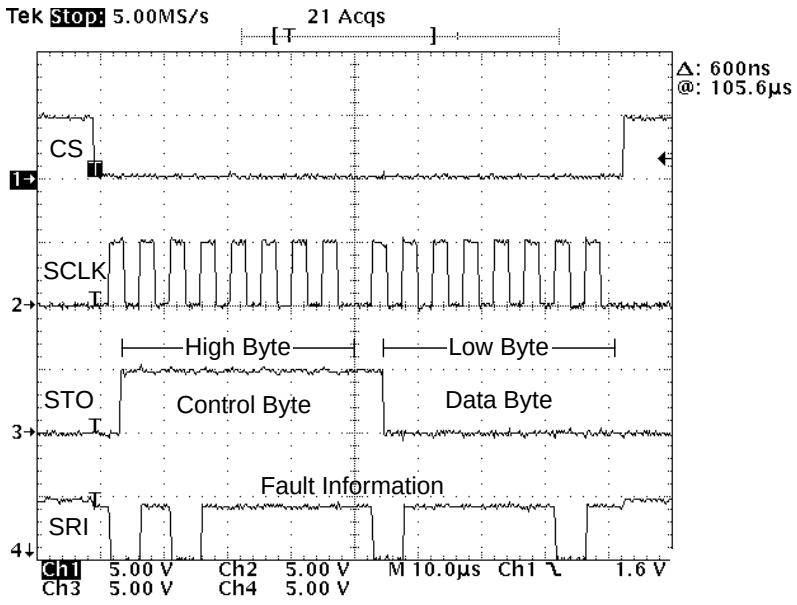


**Figure 5 :**
**Consecutive Byte Transfer with the SSC of the C515C**

## 2.2 Software Emulation of the Serial Peripheral Interface

In general the SPI compatible Synchronous Serial Channel will be used for communication between microcontroller and intelligent power IC. But there is still another way to establish communication between a Siemens C500 8 bit microcontroller and the intelligent Siemens power IC TLE 6230. If the SSC is used for other tasks or simply if the microcontroller is not equipped with the SSC peripheral a software emulation of the SPI can be used.
In this case, clock generation, serial shift with an emulated shift register and sampling of the applied data must be realized by software.
The separation of single bits can be achieved by rotating the relevant bit into the Carry Bit, which is bit accessable. With this principle single bits can be transferred to a dedicated output pin (SO). With the same principle the data applied on an input pin (SI) can be copied into the Carry Bit and will be transferred with the next left rotation to position 0 of the Accu. After the transmission of 8 bit the Accu contains the received byte. The basic principle is illustrated in figure 6.

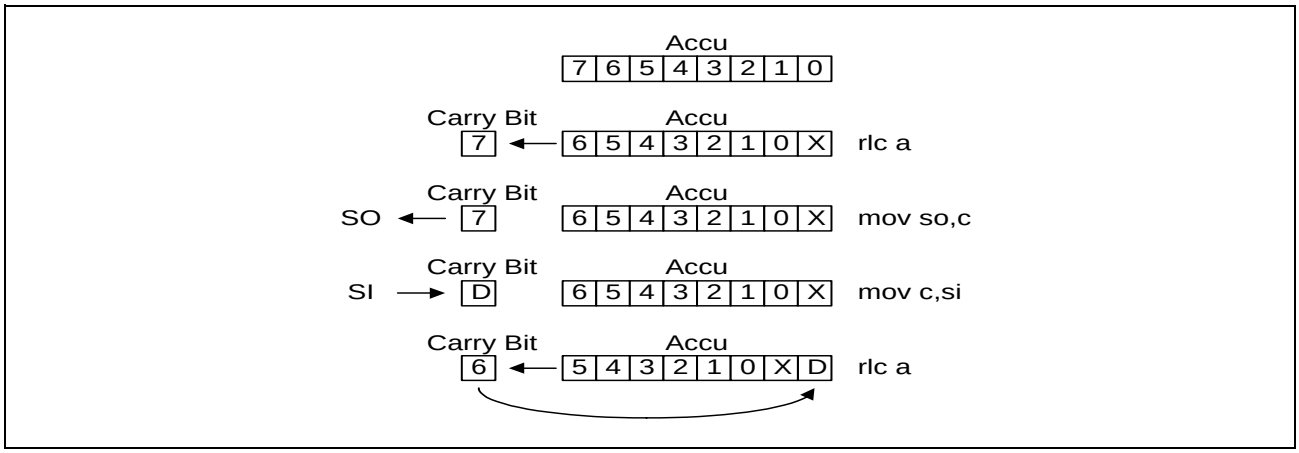


**Figure 6 :**
**Principle of software emulation of the SPI**

The assembler listing of the software emulation of the Serial Peripheral Interface is shown in Figure 7 and the timing diagram of this procedure can be found in figure 8. In this example the driver software is written in assembler in order to achieve high SPI transfer rates

```
1:      clr  SCLK              ; set idle clock to low
2:      clr  CS                ; activate chip select
3:      mov  A, spi_buffer     ; load high byte
4:      mov  bit_counter,#8h   ; set bit count
 loop1:
5:      setb SCLK              ; rising clock edge: output data
6:      rlc  A                 ; shift the bit to be transferred into the carry bit
7:      mov  SO, C             ; copy this bit to output pin
8:      clr  SCLK              ; falling clock edge: latch data
9:      mov  C, SI             ; read input pin
10:     djnz bit_counter,loop1;
11:     rlc  A                 ; shift last bit from carry to reg A
12:     mov  output16, A       ; save received data
13:     mov  A, spi_buffer+01H; load low byte
14:     mov  bit_counter,#8h   ; set bit count
 loop2:
15:     setb SCLK              ; see above
16:     rlc  A
17:     mov  SO, C
18:     clr  SCLK
19:     mov  C, SI
20:     djnz bit_counter,loop2
21:     rlc  A
22:     mov  spi_buffer+01H, A; save received data
23:     setb CS                ; deactivate chip select
24:     ret
```

**Figure 7 :**
**Software Emulation of the Serial Peripheral Interface**

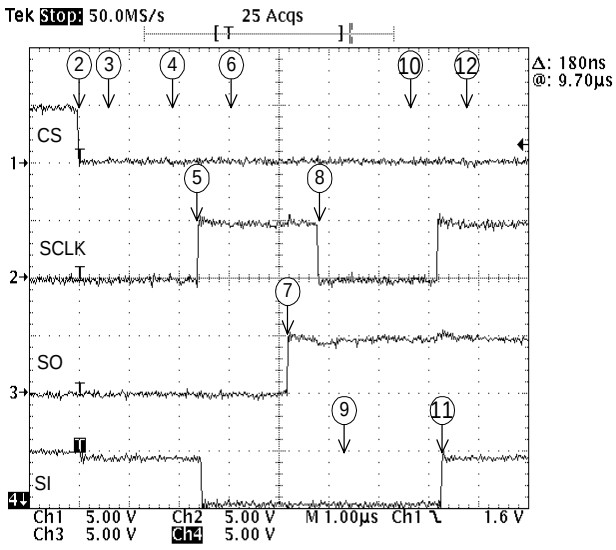


**Figure 8 :**
**Timing diagram of the software emulation (numbers in circles relate to code lines in figure 7)**

### 2.3 Performance considerations

The performance comparison between the both introduced principles is done with a C515C running at a crystal frequency of 10 MHz.

- on chip SSC achieves a max. baudrate of 2,5 MBaud
- software SPI emulation achieves a max. baudrate of 200 KBaud

In both cases two bytes have to be transfered consecutively. The SSC peripheral allows high transmission rates with a minimum of CPU load.
In contrast to that, a software emulation of the SPI Interface can never be as fast as a dedicated peripheral and will require much more CPU attention. The 16 bit data transfer is done within 80 µs and full CPU load. But the software emulation can be interrupted by a higher prior task at any time. In this case it must be ensured that the pins assigned to the SPI bus interface keep their state while e.g. the interrupt service routine is processed.

## 3 How to control a TLE 6230 GP with a C16x microcontroller

All members of the Siemens C16x 16 bit microcontroller family which are dedicated for automotive and industrial applications like the C161, C164 and C167 are equipped with the fully SPI compatible SSC (Synchronous Serial Channel). This peripheral can be configured in a very flexible way. The data width can be choosen from 2 bits to 16 bits. The clock control allows the adaption of clock polarity and clock phase to the specific application demands. Communication can be achieved with baudrates up to 5 MBaud (@ 20 MHz CPU clock). The SSC peripheral of the Siemens C16x microcontroller family fits perfectly for the smart multiple Low-Side Switches TLE 62x0 GP.
No additional software effort is necessary for 8 and 16 bit data transfers. Once the data transmission is started, the 8 or 16 bit are transferred autonomiously by the SSC.

The initialization of the SSC for proper communication with the TLE 6230 GP can be found in the attached software examples.

## 4 Conclusion

State of the art embedded control applications require powerfull microcontroller architectures as well as intelligent power devices. Sytems based on a TLE 62x0 GP and a C500 or C16x microcontroller allow powerfull and cost effective designs. With its rich set of peripherals for PWM generation, Siemens micrcocontrollers support the directly controlable output stages of the TLE 62x0 GP family. The SPI allows comfortable data exchange between microcontroller and multiple Low-Side Switch. Communication can be established either with 8 bit or with 16 bit microcontrollers. Therefore, the octal Low-Side Switch TLE 6230 GP and the hex Low-Side Switch TLE 6240 GP, with its 16 bit SPI, do not necessarily require a 16 bit microcontroller and can be also controlled by an 8 bit microcontroller.